Low Power Dynamic Logic Circuit with Leakage Reduction Technique

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ABSTRACT
In this paper a technique is proposed to reduce the leakage power of domino logic. In this proposed circuit pseudo dynamic buffer is used to reduce the power dissipation due to the precharge pulse propagation and leakage control transistor is used to reduce the leakage power. The leakage control transistors increase the resistance of the path from supply voltage to ground. As a result the leakage current is reduced. The cadence spectre tool at 180nm technology is used for simulation. The proposed logic is compared with the existing logic design. It is observed from the simulation that the power delay product and leakage current is reduced up to 32% and 10% respectively as compared to pseudo dynamic buffer based domino logic.

General Terms
Pseudo dynamic buffer based domino logic, LECTOR technique

Keywords
Low power domino logic, leakage current, CAD tool

1. INTRODUCTION
Low power and high speed logic design circuits[1,2] is getting more attention in consideration of product manufacturing. As power reduction is more important in comparison to any other constraint, presently dynamic logic is widely used. With respect to complementary static circuits in case of dynamic logic circuits the transistor count is reduced to almost half. But the cascading problem is the main issue in the dynamic logic. Due to this problem domino logic has been preferred. As compared to the dynamic logic circuit the domino logic circuits are more power efficient and comparatively faster. In Domino logic circuit a static inverter is present after the dynamic logic. The operation of the domino logic circuit is regulated by a clock signal [3]. Parasitic capacitance is used to store the output of the dynamic logic circuit and then passes it to the output stage of the domino circuit. Although the domino logic circuit has the advantage of higher speed and smaller area[8], a remarkable power is wasted because of these periodic precharge phases associated with the process. Moreover, the precharge pulses set up extra noise in the gate and when these pulses are propagated through the static buffer gives rise to surplus consumption of power [4]. True single phase clock(TSPC) based dynamic logic circuit[5] is used to avoid the noise introduced during precharge phase. But this is having a disadvantage that it uses an additional clock transistor in the output stage static inverter. Due to this extra clock transistor more power is consumed during precharge phase. A dynamic logic design using pseudo dynamic buffer(PDB) has been proposed[6]. In case of PDB based domino logic, the precharge pulse is not allowed to be propagated to the domino gate and stopped at the first stage. As a result of this effect, in the precharge phase the typical consumption of power in the buffer is significantly saved. In comparison to TSPC based dynamic logic in PDB based domino logic the no of clock transistor is reduced from 3 to 2. Hence the load capacitance lowers and the power consumption of this scheme is significantly less. In the above logic design the focus is on the power dissipation due to precharge pulse propagation. But the leakage power does not reduced in the above logic design. With advancement of technology high leakage current becomes a key factor in power dissipation of the circuit. Hence to reduce the leakage power leakage control transistors are used in between the precharge network and evaluation network. Due to effective stacking of transistor the resistance in the path is increased and hence leakage current is reduced.This paper is organized as follows. Section 2 describes briefly all the previous works. Section 3 presents in detail the proposed PDB based domino logic using lector technique. Section 4 deals with the computer simulation and power comparison with the PDB logic circuit. The conclusion is made in Section 5.

2. PREVIOUS WORK
2.1 Conventional Domino Logic
Figure 1(A) represents the conventional domino logic which consist of a dynamic pull down network followed by a static inverter. Generally dynamic logic uses n type network. Figure 1(B) depicts the domino logic implementation of a buffer. This gate is operated under two distinct phases namely, precharge phase when the clock(CLK) is low and evaluation phase when the clock is high. In precharge phase the clock is low, hence the NMOS transistor Q_2 is turned OFF and the PMOS transistor Q_1 is ON. So irrespective of the input combination the dynamic node S is charged to $V_{DD.}$ Hence output node Y drops down to zero. During evaluation phase the CLK is high hence NMOS transistor Q_2 is on. If its input combination is high the dynamic node S is connected to ground and it will discharge to zero[7]. If input combination is low then the logic at node S is kept high regardless of operating phase.

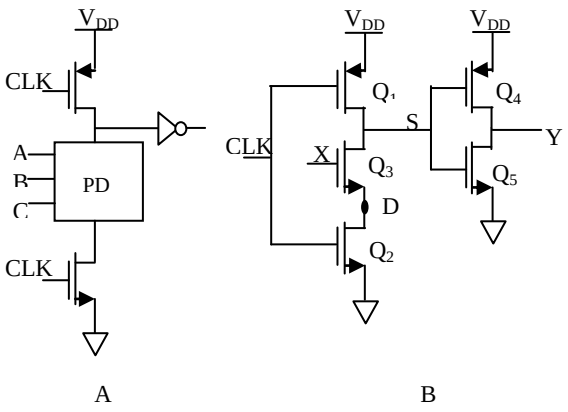

Figure 1: (A) Conventional buffer using the domino logic circuit (B) example of implementation of buffer .

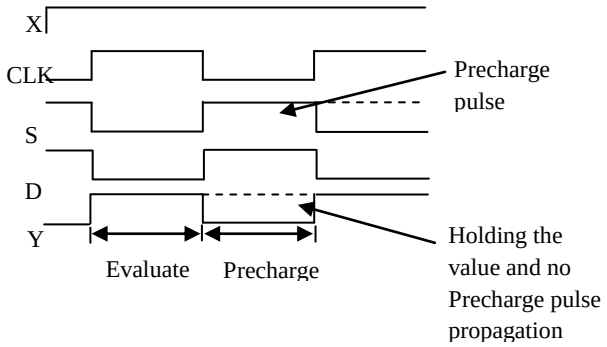

Figure 2: Timing diagram of the conventional domino buffer circuit, when X is '1'

A significant increase in power is observed when the precharge pulse is propagated from the dynamic node S to the next stage which is a static buffer and also during the precharge phase the output is not stable. Cascading is also limited. To overcome this problem a no of logics are proposed [6,7].

2.2 PDB Based Domino Logic

To avoid the drawback of conventional domino logic and TSPC based domino logic, the dynamic logic design using pseudo dynamic buffer has been done. Here an example of PDB based buffer [6] is taken as shown in the Figure 3.

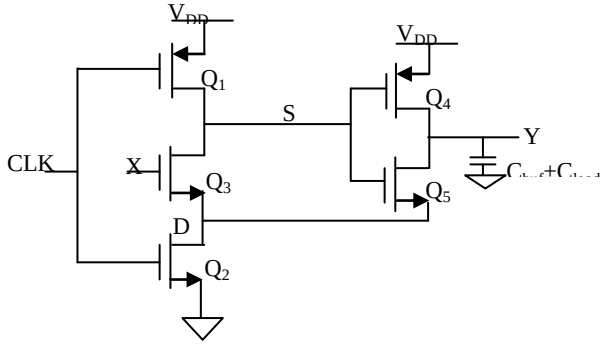

Figure 3: PDB based domino logic circuit

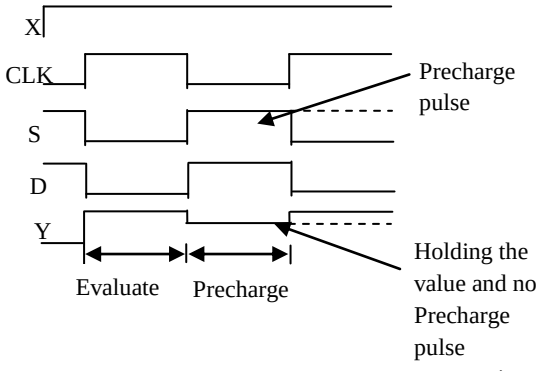

Figure 4: Timing diagram of the PDB based domino logic circuit.

In this PDB logic the source of the transistor Q_5 is not connected to GND. Rather it is connected to the node D. Hence during precharge phase when the node S is high, Y restores its previous value as the clock transistor Q_2 is OFF. Hence the dynamic node S cannot propagate to output node during precharge pulse. While the input X is low S remains high and the output drops down to zero regardless of the operating phase. In case of high input , the operation of the circuit in precharge and evaluation phase is as follows:During the evaluation phase, the CLK is high so the NMOS transistor Q_2 is turned on. Hence the dynamic node S is discharged to GND through node D. So the output goes high. During the precharge phase, the CLK becomes low, so the PMOS transistor Q_2 turned ON. Hence the dynamic node S becomes high. The NMOS transistor Q_2 is turned OFF, hence the output becomes high as it cannot be discharged to GND.

3. PROPOSED PDB BASED DOMINO LOGIC USING LECTOR TECHNIQUE

In case PDB based domino logic the dynamic power decreases. but the static power is not reduced. By using leakage control transistor technique[9], the static power reduction is enhanced. In this technique the leakage power can be reduced by the effective stacking of transistor between the precharge network and evaluation network . It is based on the study [10] that the state with one OFF transistor is more leaky than that of more than one transistor OFF from supply voltage to ground.

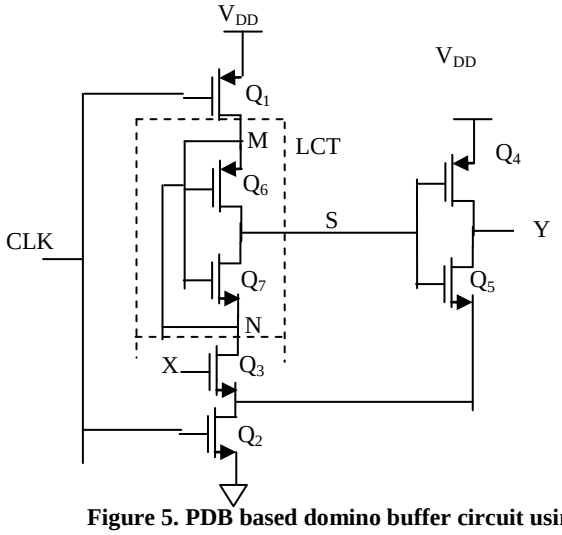

Figure 5. PDB based domino buffer circuit using leakage control transistor.

Figure 5 shows the implementation of a buffer using PDB based domino logic using LECTOR technique. In this technique between precharge network and evaluation network two leakage control transistor Q_6 and Q_7 is inserted . Gate of the two transistors are connected to the source of each other and drain of both transistors are connected to the input of the static inverter.In precharge phase, as CLK is low, Q1 transistor is ON. As node N has not the sufficient voltage to turn off Q_6, it will remain in near cutoff state. Similarly during the evaluation phase voltage at node M is not sufficient to turn off the transistor Q7, it will remain in its near cut off state. Hence resistance between supply voltage to ground increases, hence leakage current reduces. In Figure 6 an 1-bit full adder using PDB based domino logic with LECTOR technique is shown.

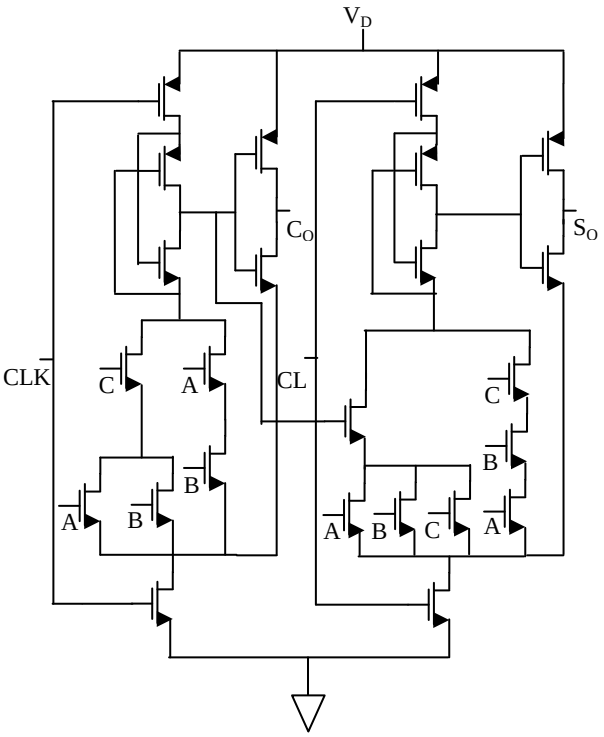

Figure 6: 1 bit full adder using PDB based domino logic with leakage control transistor

4. SIMULATION RESULT

The performance of the proposed circuit is evaluated using 180nm CMOS technology. To show the power reduction of the proposed circuit cadence spectre simulator for 180nm standard CMOS technology is used.

Table 1: Power consumption and delay comparison of different type of logic design

Logic function	Power (PDB) (µW)	Power (LCT) (µW)	Delay (PDB) (µW)	Delay (LCT) (µW)	PDP (PDB) $x10^{-15}$ W-S	PDP (LCT) $x10^{-15}$ W-S
AB	35.22	33.92	168.5	122.2	5.93	4.14
ABC	34.33	33.43	199.3	159.5	6.84	5.31
A+B	47.72	42.93	107.2	80.36	5.11	3.44
A+B+C	47.75	42.96	111.6	92.82	5.32	3.98
A+B+C+D	47.75	42.97	118.6	104.7	5.66	4.49
AB+CD	47.67	42.87	240.4	194.3	11.45	8.32

From Table 1 we observed that the power delay product of PDB based domino logic using LECTOR technique is significantly less as compared to PDB based logic Without LECTOR technique.

Table 2. Leakage power comparison of different logic function

Logic Function	Power (PDB) (µW)	Power (LCT) (µW)	Power Saving (%)
AB	26.46	23.79	10.09
ABC	26.42	23.74	10.14
A+B	13.26	11.93	10.03
A+B+C	8.843	7.958	10.00
A+B+C+D	6.633	5.96	10.14
AB+CD	26.46	23.79	10.09

Table 2 shows that, for all the logic functions the leakage power of PDB based domino logic using LECTOR technique, is reduced as compared to the PDB based domino logic without using LECTOR technique.

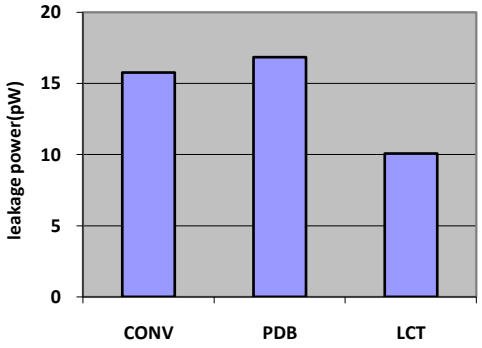

Figure 7: Leakage Power comparison between conventional domino logic, PDB domino logic and LCT based PDB logic at 500MHz clock frequency for 1 bit Full adder.

The above figure shows that in case of PDB based domino logic using LECTOR technique there is 36.11% and 40.21%

leakage power saving as compared to conventional domino logic and PDB based domino logic for a 1 bit full adder.

5. CONCLUSION

Different logic style is used to reduce the power dissipation of domino logic due to propagation of precharge pulse. This paper proposed a technique to reduce the active power consumption and leakage current as compared to other logic design. In the proposed domino logic the use of both PDB logic and lector technique improves the reduction in the power consumption and leakage current. The simulation result shows that power delay product and leakage current can be reduced up to 32% and 10% as compared to PDB logic design.

6. REFERENCES

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