

Hybrid Model of Multilevel Inverter With Selected Harmonic Elimination

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ABSTRACT

Multi-level inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. In this paper, the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cell with separate dc sources. In this paper, we proposed a new multi-level inverter topology based on a H-Bridge with number of switches connected in series with dc link as per the number of levels. The output voltage of the proposed topology is quite closer to quasi sinusoidal waveform compared with a typical single phase inverter. The proposed multilevel inverter is applicable to power conditioning system for renewable energy sources, and it also be used as a building block of cascaded multilevel inverter for high voltage. In case of conventional H-bridge type or NPC type multilevel inverter, 12 controllable switches are used to obtain a 7 level output voltage. But the proposed multilevel inverter requires only 7 switches. The efficiency can be improved with the reduction of the switching loss. The multilevel inverter is composed of an H-Bridge inverter and the active switches are connected in series with the DC link as per the requirement. For the 7-level output, seven numbers of switches and two numbers of diode are used. Three different DC source are required for the multi-level inverter. For a low or medium power application, we can use MOSFET or IGBT as power semiconductor switches.

Keywords

Multi-level inverter; Total Harmonic Distortion; Cascade multi-level inverter.

1. INTRODUCTION

The concept of multi-level converters has been introduced since 1975 [1]. The term multilevel began with the three-level converters [2-3]. Subsequently, several multilevel converter topologies have been developed [4-15]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources. The commutation of the power switches aggregate these multiple DC sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also

can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced [16-17].

Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage. Therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [18].

Input current: Multilevel converters can draw input current with low distortion.

Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

2. PROPOSED MODEL FOR 7-LEVEL MULTILEVEL INVERTER

Besides the multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed [19-22]; in this proposed MLI there is no capacitor used. Separate DC source is used for the topology as the number of separate DC source is used in cascaded multilevel inverter. This topology is slightly different than the inverter discussed in previous chapter. Though there is no capacitor is used, so the capacitor voltage unbalancing does not occur. Table-1 gives the comparison of proposed 7-level inverter with H-Bridge inverter and NPC type MLI.

Table 1 Comparison of different MLI

Devices	Active Devices	Passive Devices	Conduction Devices	Switching Devices
H-Bridge MLI	12	0	6	4
NPC type MLI	12	8	8	4
Proposed MLI	7	2	3	2

Hence, we conclude that in Table-1, as the numbers of switches are reduced means the cost of the inverter get reduces. And also the switching loss of the power semiconductor devices reduces.

A. Operating mode in inverter

The output voltage of the proposed multilevel inverter has 7-levels ($3V_{DC}$, $2V_{DC}$, V_{DC} , 0 , $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$) according to the switching condition. In 7-level PWM inverter, the instantaneous magnitude of reference signal (V_{ref}) is compared with the amplitude (V_c) of the carrier signal. The output voltage level of switching condition of MLI is given in Table-2.

Table 2 Switching condition of MLI

Output Voltage	Switching Condition						
	S1	S2	S3	S4	T1	T2	T3
$3V_{dc}$	1	0	0	1	0	0	1
$2V_{dc}$	1	0	0	1	0	1	0
V_{dc}	1	0	0	1	1	0	0
0	1	0	0	1	0	0	0
$-V_{dc}$	0	1	1	0	1	0	0
$-2V_{dc}$	0	1	1	0	0	1	0
$-3V_{dc}$	0	1	1	0	0	0	1

3. FORMULATION FOR 7-LEVEL MLI

The cascade multilevel inverter consists of a series of H-Bridge (single-phase full-bridge) inverter units. As stated above, the general function of the multilevel inverter is to synthesize a desired staircase voltage from several separate DC sources (SDCSs) such as solar cells, fuel cells, ultra capacitors, etc. The output waveform of a 7-level MLI is shown in Fig. 1.

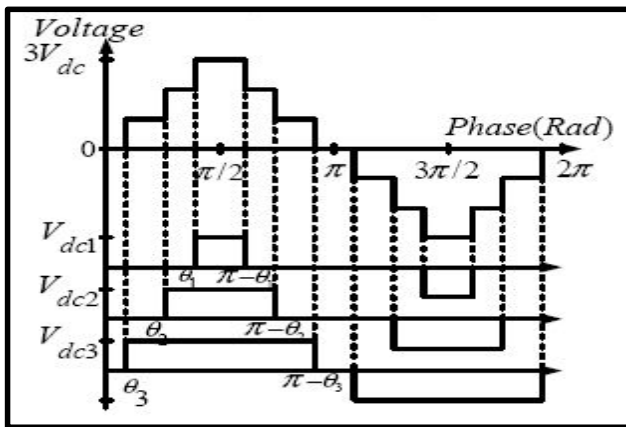


Fig.1. Output waveform of a 7-level MLI

The Fourier series expansion for the above stair case wave form is given in equation (1)

$$V_{an}(\omega t) = \sum_{n=1,5,7}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)) \sin(n\omega t) \quad (1)$$

where 'n' represents the order of the harmonics in the output waveform. The fundamental voltage is obtained from the calculated switching angles $\theta_1, \theta_2, \theta_3$ from equation (1). It is required to find the switching angles in the range of 0 to $\pi/2$ considering 5th and 7th order phase voltage to zero. For a seven level cascaded multilevel inverter, the fundamental voltage in terms of switching angles is given in equation (2).

$$V_1 = \frac{4V_{dc}}{\pi} (\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)) \quad (2)$$

The modulation index is defined as the ratio of fundamental voltage (V_1) to the maximum obtainable fundamental voltage (V_{1max}). The maximum fundamental voltage is obtained when all the switching angles are zero and the V_{1max} is given as (3)

$$V_{1max} = 3 * \left(\frac{4V_{dc}}{\pi} \right) \quad (3)$$

Then the modulation index (M) is given as in equation (4)

$$M = \frac{V_1}{3 * \left(\frac{4V_{dc}}{\pi} \right)} \quad (4)$$

The 7-level cascaded inverter requires three H-Bridges. The nonlinear equations which are used to finding the switching angles and desired fundamental voltage of 7-level inverter are equations (5), (6) and (7).

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = M\pi/4 \quad (5)$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) = 0 \quad (6)$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \quad (7)$$

These are the nonlinear transcendental equations for eliminating lower order harmonics such as 5th and 7th order and get desired fundamental voltage. For the given values of M (from 0 to 1), it is required to get complete and all possible solutions of these equations for determining the switching angles and lower THD. The THD equation for voltage is as follows:

$$THD = \left[\frac{1}{V_1^2} \sum_{n=5}^{\infty} V_n^2 \right]^{0.5} * 100 \quad (8)$$

Aim of the analysis is to eliminate 5th and 7th order harmonics, but THD can be optimized up to 49th order or above. As the inverter level increases according to that equation is added to above equations (5), (6) and (7). For a 11-level inverter, two more equations has to be considered for eliminating 5th, 7th, 11th and 13th order harmonics.

4. USE OF GENETIC ALGORITHM

Genetic Algorithm (GA) is well suited for solving non-linear problems and in most cases they can find the global optimum solution with a high probability. GA algorithm is based on the principle of natural genetics and natural selection.

Procedure:

- Select some switching angle randomly.
- Calculate the generation index and population index.
- If $0 < \alpha_1 < \alpha_2 < \dots < \alpha_m < \pi/2$, then go to next step, otherwise repeat above.
- Compute the objective function $F(\alpha)$.
- Find the best of individuals.
- Using crossover and mutation find the new set of values.
- If the solution is converge, then stop and find the switching angles otherwise repeat for the next generation.

5. SIMULATION AND RESULTS

For simulation of a 7-level MLI three DC sources are used. In this paper three 100V DC sources are selected. In this simulation 0.06 is taken as one period and phase delay is taken as 0.02 (switching angle 1), 0.04 (switching angle 2) and 0.06 (switching angle 3). S1 and S2 operate always in positive half cycle with switch T1, T2 and T3 in operation and S3 and S4 operates in negative half cycle with T1, T2 and T3 switched ON with a periodic interval. The output voltage, output current waveform, thyristor pulse rate, and frequency spectrum of line to line voltage shown in Fig.2, Fig.3, Fig.4, and Fig.5 respectively.

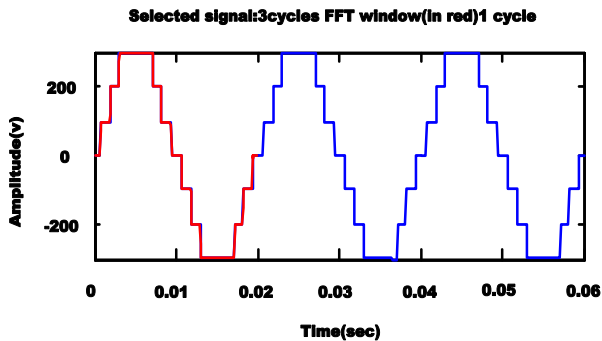


Fig. 2 Output voltage waveform

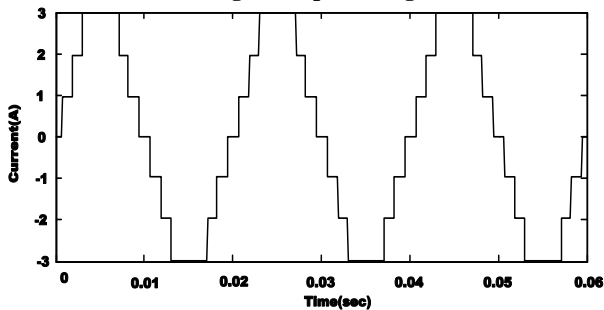


Fig. 3 Output current waveform

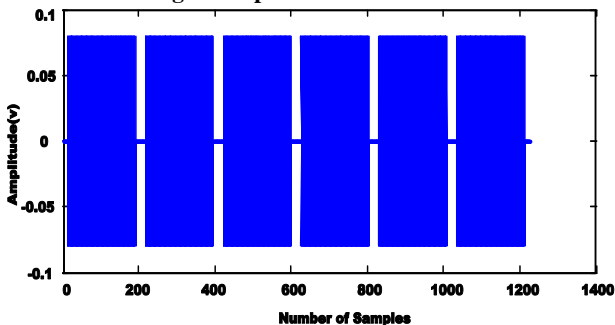


Fig.4 Thyristor pulse rate waveform

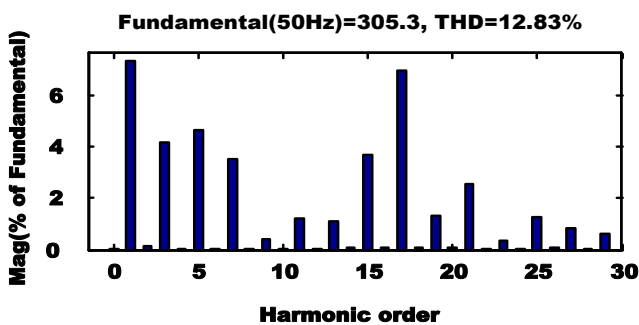


Fig. 5 Frequency spectrum for Output Line-Line Voltage

6. CONCLUSION

A simulation model for the hybrid multilevel inverter is developed in MATLAB. The inverter output is a seven level phase voltage. This paper present a main circuit model in MATLAB and simulation results analyzed fully. In this paper the number of switches used to get the seven-level output voltage is lesser in comparison with other conventional multilevel inverter [20]. Switching loss of the proposed model is reduced by 50% in comparison to the cascaded multilevel inverter as less number of switches in the circuit makes it simple, reliable and low cost. Total harmonic distortion in the proposed model is reduced by 4.16% as compared to the existing model. The voltages produced in the output of the inverter are seven levels with a low voltage distortion. With increase in level of multilevel inverter, THD reduces. And also voltage distortion due to dead time effect doesn't occur.

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