Effect of Driver Width Variations on Propagation Delay of Driver-Interconnect-Load System

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ABSTRACT
The performance of VLSI/ULSI chip is becoming less predictable as device dimensions shrinks below the sub-100-nm scale. Process variation is considered to be a major concern in the design of circuits including interconnect pipelines in current deep submicron regime. Process variation results in uncertainties of circuit performances such as propagation delay. The reduced predictability can be attributed to poor control of the physical features of devices and interconnects during the manufacturing process. Variations in these quantities maps to variations in the electrical behavior of circuits. The channel width of MOSFET varies due to changes in drain/source thickness; substrate, polysilicon and implant impurity level; and surface charge. This paper provides a comprehensive analysis of the effect of channel width variation on the propagation delay through driver-interconnect-load (DIL) system. The impact of process induced driver width variations on propagation delay of the circuit is discussed for three different technologies i.e. 130nm, 70nm and 45nm. The comparison of results between these three technologies shows that as device size shrinks, the process variation issues becomes dominant during design cycle and subsequently increases the uncertainty of the delays.

General Terms
Interconnects, delay, signal, VLSI.

Keywords
Process variation, parasitic, propagation delay, driver width, load, technology node.

1. INTRODUCTION
The semiconductor industry has been fueled by enhancements in integrated circuit (IC) density and performance, resulting in information revolution for over four decades and is expected to continue in future. The periodic improvement in density (as per Moore's Law) and performance has been mainly achieved through aggressive device scaling and/or increase in chip size. As far as MOS transistor scaling is concerned, device performance improves as gate length, gate dielectric thickness, and junction depth are scaled. In sharp contrast to this, scaled chip wiring (interconnect) suffers from increased resistance due to decrease in conductor cross-sectional area and may also suffer from increased capacitance if metal height is not reduced with conductor spacing.

Variability in modern nanometer sized circuits has not scaled down in proportion to the scaling down of their feature sizes. Manufacturing process variations (e.g. driver width, effective channel length), environmental variations (e.g., supply voltage, temperature), and device fatigue phenomenon contribute to uncertainties. Uncertainty due to parametric variations deeply impacts the timing characteristics of a circuit and makes timing verification extremely difficult. This necessitates the consideration of the parametric variations in timing analysis for accurate timing estimation.

The performance of a high-speed chip is highly dependent on the interconnects, which connect different macro cells within a VLSI/ULSI chip. With ever-growing length of interconnects and clock frequency on a chip, the effects of interconnects cannot be restricted to *RC* models [1-3]. The importance of on-chip inductance is continuously increasing with faster on-chip rise times, wider wires, and the introduction of new materials for low resistance interconnects. It has become well accepted that interconnect delay dominates gate delay in current deep sub micrometer VLSI circuits [2, 3]. With the continuous scaling of technology and increased die area, this behavior is expected to continue.

The function of interconnects or wiring systems is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on the chip. To escape prohibitively large delays, designers scale down global wire dimensions more sluggishly than the transistor dimensions [2, 3]. As technology advances, interconnects have turned out to be more and more important than the transistor resource, and it is essential to use global interconnects optimally. For high-density high-speed submicron-geometry chips, it is mostly the interconnection rather than the device performance that determines the chip performance. As operating frequencies continue to spiral upward, parasitic inductive effects must also be considered. Thus, interconnect parasitic play an increasing role in overall chip performance as feature size scales.

Distribution of the clock and signal functions is accomplished on three types of wiring (local, intermediate, and global). An interconnect depending on its length, can be classified as local, semi-global and global [2, 3]. Local wiring, consisting of very thin lines, connects gates and transistors within an execution unit or a functional block (such as embedded logic, cache memory, or address adder) on the chip. Local wires usually span a few gates and occupy first and sometimes second metal layers in a multi-level system. The length of a local interconnect wire approximately scales with scaling of technology, as the increased packing density of the devices make it possible to similarly reduce the wire lengths. Intermediate wiring provides clock and signal distribution within a functional block with typical lengths up to 3–4 mm. Intermediate wires are wider and taller than local wires to provide lower resistance signal/clock paths. Global wiring provides clock and signal distribution between the functional blocks, and it delivers power/ground to

all functions on a chip. Global wires, which occupy the top one or two layers, are longer than 4mm and can be as long as half of the chip perimeter. The length of global interconnect wires grow proportionally to the die size.

In current DSM technology, a major challenge of variability has been faced by semiconductor industry. In addition, digital circuits show an increased sensitivity to process variations due to low-power and low voltage operation requirement, which may fail to meet timing constraints. The feature sizes are going to be reduced with increased variability. Obviously, there are other technological opportunities for aggressive scaling when more variability can be tolerated. This will lead to better and cheaper products (provided the quantities are large enough). Designers have to make the resulting variability which is sufficiently harmless by using suitable architectures and topologies. The challenge of Electronic Design Automation (EDA) is to provide accurate and efficient procedures to enable designers to understand the effect of pertinent process variability on their design. Increasing process variations can affect electrical parameters of interconnects (e.g. capacitances) and further influence circuit performance and functionality. Due to the process variation, interconnect technology parameters (ITP) are varying substantially. For the sake of simplicity, researchers consider variations in metal thickness, metal width and interlayer dielectric thickness. The typical distribution of interconnect technology parameters can be observed for permittivity, inter level dielectric thickness, metal height and metal width. The variation is especially large in the ILD (Inter Level Dielectric) thickness and metal line width. Their variations have a definite impact to the total line capacitance and interline coupling capacitance and result in variation of the signal delay.

The propagation delay induced by word lines, bit lines, clock lines, and bus lines in memory or logic VLSI will remain the key concerns while designing the interconnects. The performance of VLSI/ULSI chip is becoming less predictable as device dimensions shrink below the sub-100-nm scale [4-6]. The reduced predictability is due to poor control of the physical features of devices and interconnects during the manufacturing process. Variations in these quantities result in variations in the electrical behavior of circuits. These variations have interdie and intradie components, as well as layout pattern dependencies. The device material variations in geometry (t_{ox}, L_{eff}, W), and variations in doping levels and profiles have a direct impact on the behavior of a MOSFET. Variations in the line width affect the resistance and the interlayer capacitance. Variations in the interwire spacing may cause a significant degradation in the signal integrity. Layout pattern dependent variations within the interlayer oxide and the chip multiprocessing process also have a significant impact on the interconnect parasitic. The dissimilar sources of variations in the IC fabrication process lead to both random and systematic effects on circuit performance. All of these make it increasingly difficult to accurately predict the performance of a circuit at the design stage, which ultimately translates to a parametric yield loss. The recent trends in VLSI chip exhibit significant variations within a chip and between chips, due to the high complexity of design and the presence of large number of correlated parameters. Therefore, fast and efficient methods are required to compute an accurate statistical description of the response.

Process variations are not completely random. It can be divided into deterministic part and nondeterministic part [6, 7]. Depending on the spatial scales of the variation, the non-systematic variation has two categories of (i) Die-to-Die or Inter-die or Global Variation and (ii) Within-Die or Intra-die or Local Variation. Die-to-die (or inter-die or global) variations affect all transistors within a die in the same way and have identical effect. For example, gate length variation of all the devices on the same chip being larger or smaller than the nominal value. The die-to-die variations result in shift in the process from lot-to-lot, wafer to wafer, reticle to reticle on each gate in the chip. On the other hand, within-die (or intra-die or local) variations affect each device within the same die differently. For example, some devices on a die have smaller gate length whereas other devices on the same die have a larger gate length. The within-die variations can be further classified as spatially correlated and random variations. Spatially correlated variations are the kind of within-die variations which exhibit similar characteristic for devices in small neighborhood in the die than those placed far apart. However, random or independent variations are kind of within-die variations which are statistically independent from other device variations. As an illustration, RDF and LER are two major random variations. With the continuous process scaling, the contributions of random component of variation is increasing.

Random variations are intrinsic fluctuations in process parameters such as dopant fluctuations from wafer to wafer, lot to lot. On the other hand, systematic variations depend on the layout pattern and are therefore predictable for the systematic part, the variations need to be experimentally modeled and calibrated, in order to either compensate hiring the design phase or captured in the analysis phase. These effects, which include optical proximity correction (OPC), residual error and chemical mechanical planarization (CMP) dishing [8, 9], have a substantial but deterministic impact on the critical dimension (CD) of a transistor gate or the width and thickness of an interconnect wire. By accounting for systematic part of process variation in timing analysis, uncertainty can be reduced, thereby achieving closer bound for circuit performance. With the shrinking feature size in VLSI technology, the impact of process variation is increasingly felt. To address the effect, great amount of research has been done recently, such as the clock skew analysis under process variation [4-10], statistical performance analysis [9, 10], worst case performance analysis [11, 12], parametric yield estimation [12, 13], impact analysis on micro architecture [12, 13] and delay fault [14, 15] test under process variation [14-17]. As the technology reaches deep submicron or nanometer regime, the errors due to process variations becomes prominent [17-19]. Driver width of a MOSFET varies due to (1) Changes in oxide thickness; (2) Substrate, polysilicon and implant impurity level; (3) Surface charge. This paper analyzes the effect of channel width variation of MOSFET due to process variation on the propagation delay of Driver-Interconnect-Load (DIL) system as shown in Fig. 1. The propagation delay variations through DIL system are observed due to process variations in driver individually for different technologies *i.e.* 130nm, 70nm and 45nm.

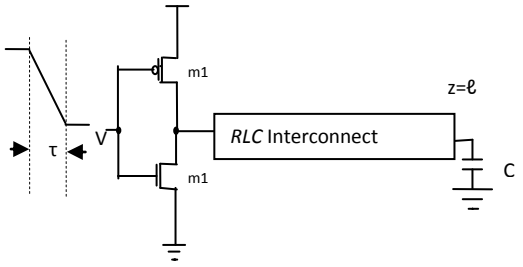

Fig 1: Driver Interconnect Load (DIL) System [21].

This paper highlights about Monte Carlo analysis in section 2. Thereafter, section 3 describes effect of driver width variation on delay of driver-interconnect-load system. Finally, a brief summary is drawn in section 4.

2. MONTE CARLO ANALYSIS

The analysis carried out in this work takes into account a Driver-Interconnect-Load (DIL) system as shown in Fig. 1. The driver is an inverter gate driving the interconnect. The propagation delay of a DIL system is dependent on various physical parameters which are prone to process variation. In this analysis, the driver is subjected to process variations in reference to driver width for three different technologies of 130nm, 70nm and 45nm. To obtain statistical information on how much the characteristics of a circuit can be expected to scatter over the process, Monte Carlo analysis is applied. Monte Carlo analysis performs numerous simulations with different boundary conditions. It chooses randomly different process parameters within the worst case deviations from the nominal conditions for each run and allows statistical interpretation of the results. In addition to the process parameter variations, mismatch can be taken into account as well, providing a more sophisticated estimation of the overall stability of the performance with respect to variations in the processing steps. In most cases the parameters on which the assumptions for the mismatch are based are worst case parameters. A proper layout and choice of devices can significantly improve scatter due to mismatch. In order to obtain reasonable statistical results, a large number of simulations are needed, leading to quite long simulation times.

3. VARIATION OF DRIVER WIDTH ON DELAY OF DIL SYSTEM

Monte Carlo simulations are run for driver width variations in 130nm, 70nm and 45nm fabrication technology. Fig. 2 shows the SPICE input and output voltage for a variation of 20% in driver width in NMOS and PMOS transistors [22] in 130nm technology. It is observed that the output varies significantly due to the process variation parameter. Table 1 accounts for the percentage variation in NMOS and PMOS driver width; delay due to driver and interconnect line; and percentage variation in delay of driver and line. It is observed that the variation in delay ranges from -2.39% to 4.60% for 130nm technology [20]. Similarly, Monte Carlo simulations are run for driver width variations in 70nm fabrication technology also.

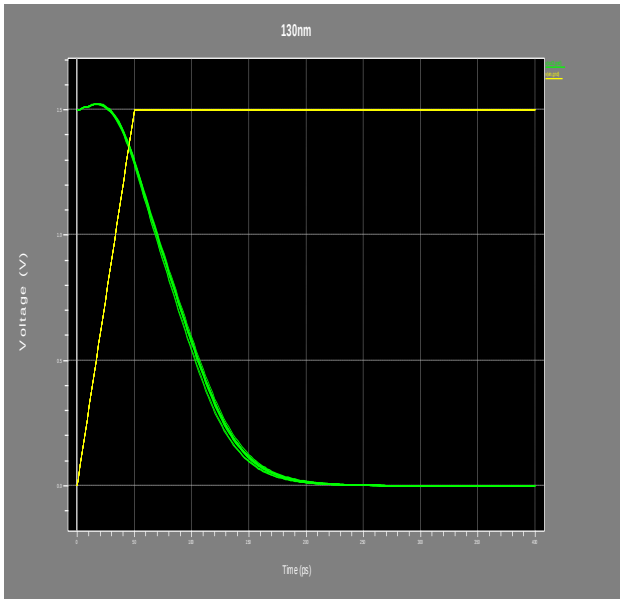

Fig 2: SPICE input and output waveform through DIL for 130nm technology driver.

Table 1. Variation in delay due to change in driver width of NMOS & PMOS for 130nm fabrication technology [21]

Variation in *Wn* (%)	Variation in *Wp* (%)	Driver and Line Delay (ps)	Variation in Delay of Driver and line (%)
-34.15	2.39	59.88	-2.39
-26.11	-5.68	60.36	-2.23
-4.06	-3.89	61.60	-0.47
-0.48	41.53	61.64	-0.62
0.00	0.00	61.82	0.00
4.33	1.99	62.08	0.61
6.21	-19.00	62.28	1.30
8.81	-10.14	62.40	1.54
10.54	-31.83	62.61	2.31
12.72	9.22	62.56	1.87
26.69	7.98	63.43	4.60

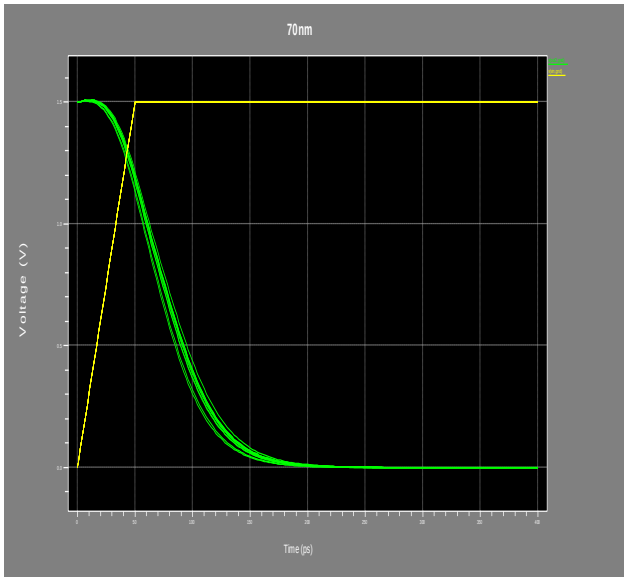

Fig 3: SPICE input and output waveform through DIL for 70nm technology driver.

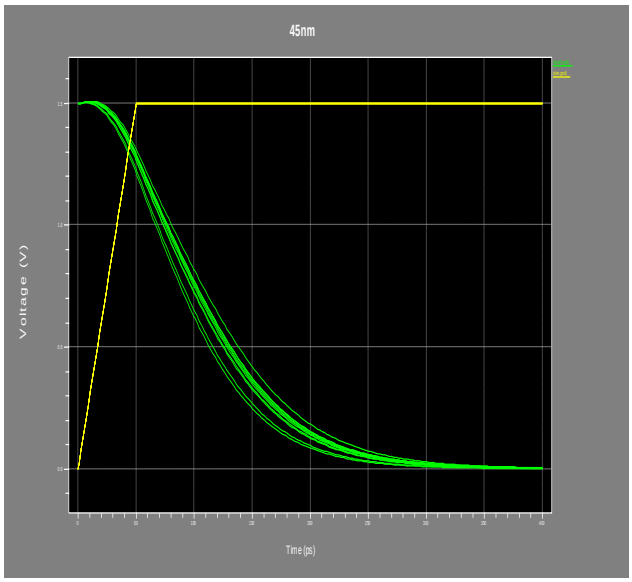

Fig 4: SPICE input and output waveform through DIL for 45nm technology driver.

Table 2. Variation in delay due to change in driver width of NMOS & PMOS for 70nm fabrication technology [21]

Variation in *Wn* (%)	Variation in *Wp* (%)	Driver and Line Delay (ps)	Variation in Delay of Driver and line (%)
-34.15	2.39	44.907	-9.13
-26.11	-5.68	45.974	-6.97
-4.06	-3.89	48.879	-1.10
-0.48	41.53	49.051	0.75
0.00	0.00	49.421	0
4.33	1.99	50.014	1.20
6.21	-19.00	50.456	2.09
8.81	-10.14	50.738	2.66
10.54	-31.83	51.186	3.57
12.72	9.22	51.137	3.47
26.69	7.98	53.124	7.49

Table 3. Variation in delay due to change in driver width of NMOS & PMOS for 45nm fabrication technology [21]

Variation in *Wn* (%)	Variation in *Wp* (%)	Driver and Line Delay (ps)	Variation in Delay of Driver and line (%)
-34.15	2.39	63.055	-13.90
-26.11	-5.68	65.425	-10.60
-4.06	-3.89	71.976	-1.70
-0.48	41.53	72.613	-0.83
0.00	0.00	73.22	0
4.33	1.99	74.656	1.96
6.21	-19.00	75.603	3.25
8.81	-10.14	76.337	4.26
10.54	-31.83	77.263	5.52
12.72	9.22	77.414	5.73
26.69	7.98	82.393	12.5

Fig. 3 shows the SPICE input and output voltage variations for variation in driver width for NMOS and PMOS transistors of the driver in 70nm technology. It is observed that the output varies appreciably higher than the results observed for 130nm technology due to the process variation parameter.

In this paper, Fig. 4 demonstrates the Monte Carlo SPICE simulation input and output voltage variations due to variation in driver width of NMOS and PMOS transistors of the driver in 45nm technology. It is observed that the output varies drastically due to the process variation parameter in 45nm technology compared to 130nm and 70nm technologies.

Table 2 accounts for the percentage variation in NMOS and PMOS driver width; delay due to driver and interconnect line; and percentage variation in delay of driver and line. It is observed that the variation in delay ranges from -9.13% to 7.49% for 70nm technology [20].

Table 3 accounts for the percentage variation in NMOS and PMOS driver width; delay due to driver and interconnect line; and percentage variation in delay of driver and line. It is observed that the variation in delay ranges from -13.9% to 12.5% for 45nm technology.

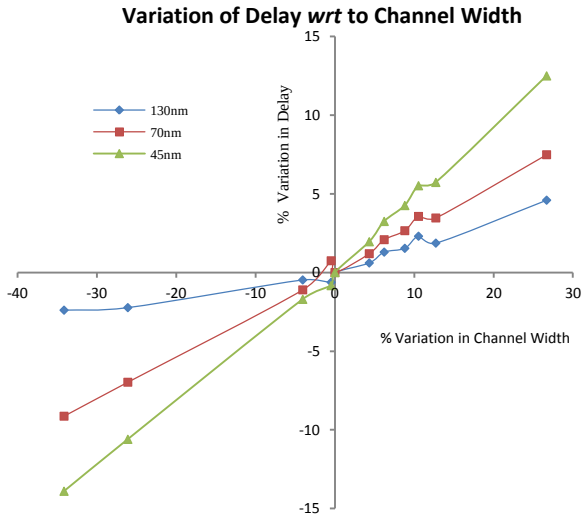

Fig 5: Comparison of percentage change in delay due to variations in driver width for 130nm, 70nm and 45nm technologies.

The comparison between three technologies shows that as device size shrinks, the process variation becomes dominant and subsequently gives rise in variation of delays. Fig. 5 demonstrates this claim by comparing the percentage change in delay due to variations in driver width for 130nm, 70nm and 45nm technologies. It is observed that as feature reduces the variation in delay performance increases due to change in driver width. Thus these simulation results reveals that process variation has large effect on the driver delay due to variation in driver width.

4. CONCLUSIONS

Process variation represents a major challenge to design system-on-chip using nanometer technologies. In this paper, we have evaluated process variation effects on the delay of Driver-interconnect-load system due to driver width variations. Variations in the driver and interconnect geometry of nanoscale chips deciphers to variations in their performance. The resulting diminished accuracy estimates the performance at design stage can lead to a significant reduction in the parametric yield. Thus, determining an accurate statistical description of the DIL response is critical for designers. The random or systematic part of variations plays an important role in deviating electrical parameter. In the presence of significant variations of device model parameters, variations in performance parameter such as delay are severely affected. The comparison between three technologies shows that as device size shrinks process variation becomes a dominant factor and subsequently raises variation in delays.

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