Implementation of LFSR Counter using CMOS Chip Technology

Nilesh P. Bobade
Assistant Professor, Dept. of Electronics Engineering
BDCE, Sevagram, wardha. M.S., India

Priti R.Meshram
BDCE, Sevagram, wardha

Payal A. Malame
BDCE, Sevagram, wardha

Pranali S. Vairagade
BDCE, Sevagram, Wardha

ABSTRACT
In chip manufacturing technology, the threshold of major evaluation, which shrinks chip in size and performance, is implemented in layout level which develops the low power consumption chip, using recent CMOS, Microwind layout tools. This paper compares 3 architectures in terms of the hardware implementation, power consumption and CMOS layout using Microwind CMOS layout tool. Thus it provides solution to a low power architecture implementation of Counter in CMOS VLSI. The Microwind program allows the designer to design and simulate an integrated circuit at physical description level. Such technology is highly applicable in the design approaches for the rural development.

Keywords
Rural development technology, Microwind chip technology, Layout level, LFSR, Pass transistor.

1 INTRODUCTION
The purpose of this research paper is to explain what a Linear Feedback Shift Register (LFSR) in CMOS chip technology. Due to advancements in large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of heat dissipation and power consumption have come into the picture. Research has been conducted to decrease the power supply voltage, switching frequency and capacitance of transistor [1] LFSR is used in a variety of applications such as Built-in-self test (BIST) [2]. Today LFSR's are present in nearly every coding scheme as they produce sequences with good statistical properties, and they can be easily analyzed. Moreover they have a low-cost realization in hardware. Counters such as Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks. They produce not only glitches, which increase power consumption but also complexity of design. The propagation delay of results of existing techniques is more which reduces speed & performance of system. Thus we are going to implement these counters with techniques using different technologies of CMOS. By studying different implementation techniques, we conclude to implement LFSR counters with pass transistor in cryptography. Unlike most everyday devices whose inputs and operations are effectively predefined, VLSI chips must be able to react to a constantly changing environment. For layout and simulation at deep submicron CMOS design tool Micro wind is used. Software implementations will be considered for further hardware implementation.

2. LINEAR FEEDBACK SHIFT REGISTER (LFSR)
An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit .LFSRs are frequently used as pseudorandom pattern generators to generate a random number of 1s and 0s. Each output of the LFSR is multiplexed with an ASIC input and, when the device is placed in the LFSR (test) mode, the random, high-toggle-rate patterns produced are extremely good for generating high-fault coverage. A LFSR can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip flops as shown in Figure.1. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, a LFSR with a well-chosen feedback function can produce a sequence of bits which appears random in nature & which has a very long cycle.

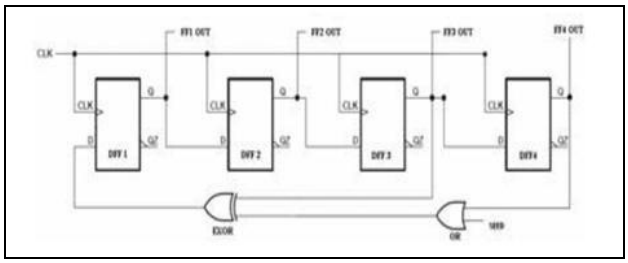

Fig.1: Block Diagram of LFSR

2.1. Working of LFSR
The list of bits position that affects the next state is called the tap sequence. In block diagram, the sequence is [4, 3].The outputs that influence the input are called taps. A maximal LFSR produces an n-sequence (i.e. cycles through all possible 2n-1 states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. The sequence of numbers generated by a LFSR can be considered a binary numeral system just as valid as Gray code or the natural binary

Table 1: PATTERN GENERATED BY LFSR

CLOCK PULSE	FF _OUT1	FF_OUT2	FF_OUT3	FF_OUT4
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	1	0	0	1
8	1	1	0	0
9	0	1	1	0
10	1	0	1	1
11	0	1	0	1
12	1	0	1	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	1	1	1

The tap sequence of an LFSR can be represented as a polynomial mod 2. This means that the coefficients of the polynomial must be 1's or 0's. This is called the feedback polynomial or characteristic polynomial. For example: if the taps are at the 3rd, 4th, bits the resulting LFSR polynomial is $X^4+ x^3 +1$.The '1' in the polynomial does not correspond to a tap. The powers of the terms represent the tapped bits, counting from the left. If (and only if) this polynomial is a primitive, then the LFSR is maximal. The LFSR will only be maximal if the number of taps is even. The tap values in a maximal LFSR will be relatively prime There can be more than one maximal tap sequence for a given LFSR length. Its output for the various condition of input is expressed in Table I.

2.2 Design Aspects

We have designed CMOS layout of LFSR Counter .The logic hardware contains D Flip Flop, 2-input OR gate, 2 input XOR gate and inverters. The most important component of our LFSR Counter Design is D Flip Flop. We have designed D-flip flop by using following different components: NAND Gates, Transmission gates and inverter and Pass transistors.

2.3 Design of D Flip Flop

The latches and flip flops are the basic building blocks of sequential circuits. In ASIC design environments, latches and flip flops are typically predefined cells specified by the ASIC vendor. The D Flip Flop is negative edge triggered. The D Flip Flop combines a pair of D latches (Master and slave). The edge triggered D Flip Flop has a setup and hold-up time window during which the D inputs must not change. The negative edge triggered D Flip Flop simply inverts the clock input, so that all the action takes place on falling edge of CLK. By designing D Flip Flop, we compare the Power Consumption; from this we decide the most efficient D Flip Flop implementation.

3. DESIGN OF D FLIP FLOP USING NAND GATE

The basic construction of the Master Slave D Flip Flop is shown in Fig.2

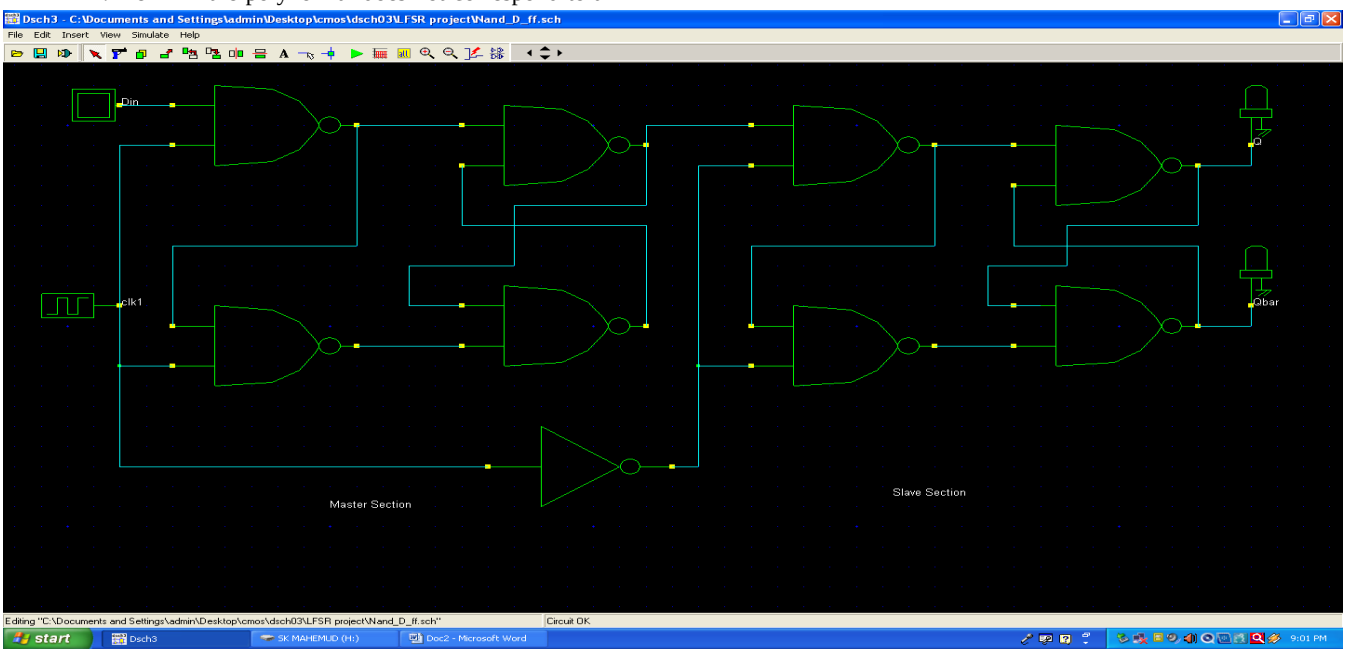

Fig.2: Master Slave D Flip Flop using NAND Gate

4. DESIGN OF D FLIP FLOP USING TRANSMISSION GATE

From Fig.3, at the negative edge of the CLK (clock), transistors T1 and T4 are ON and transistors T2 and T3 are OFF. During this time the slave maintains a loop through two inverters I3, I4 and T4. Thus the previous triggered value from Din is stored in slave. At the same time master latches next state but as T3 is OFF it is not passed to slave. At the positive clock edge T2 and T3 are turned ON and new latched value passes to slave through the loop of two inverters I1, I2 and T2. When we want to reset the circuit, both the master and slave loops are pulled down to ground.

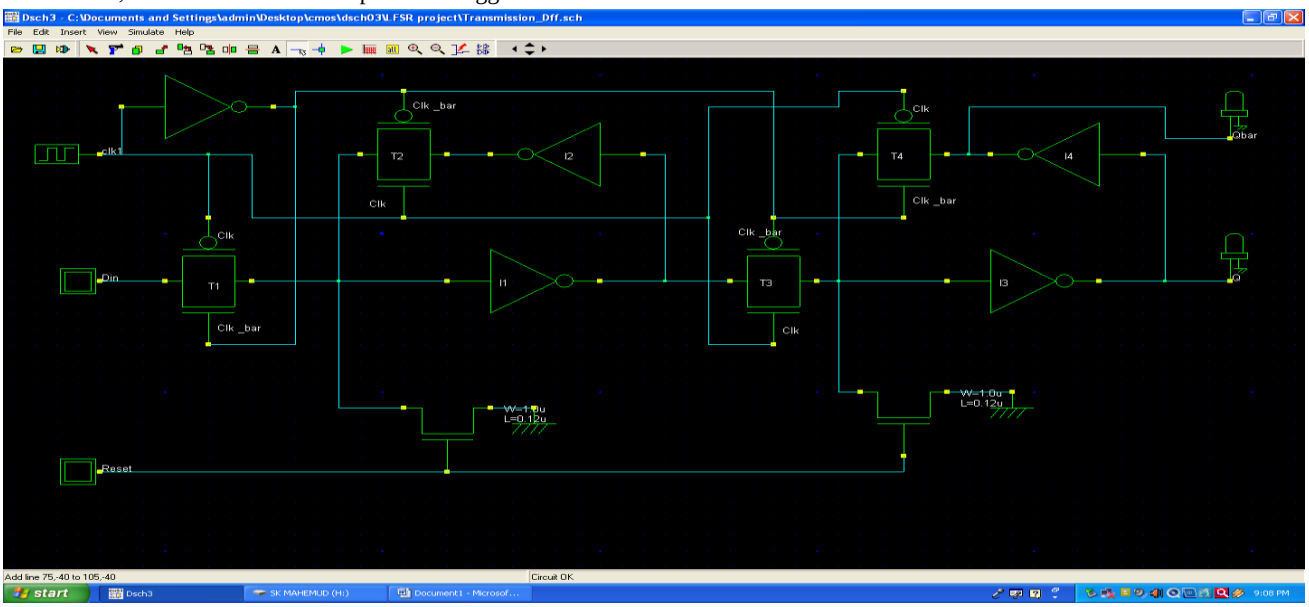

Fig.3: Master Slave D Flip Flop using Transmission Gate

5. DESIGN OF D FLIP FLOP USING PASS TRANSISTOR

The most compact implementation of edge trigger latch is based on inverters and passes transistors as shown in Figure.4. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when clock = 0. Other two chain inverters on the right hand acts in opposite way, and the reset function is obtained by direct ground connection of the master and slave memories, using NMOS devices.

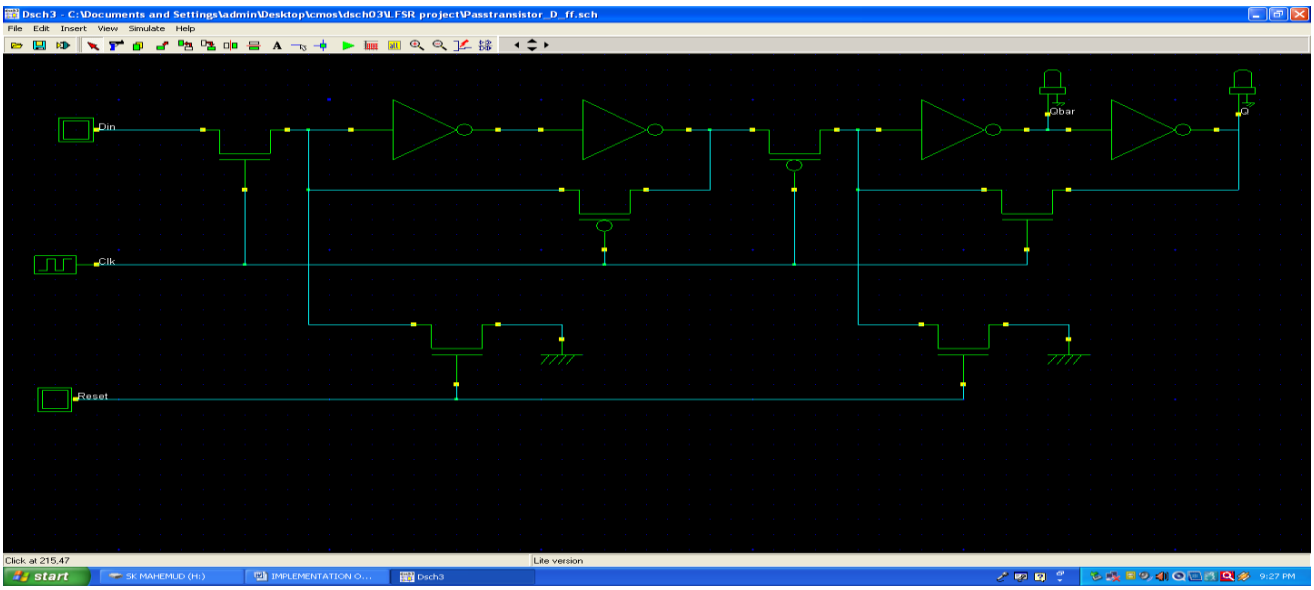

Fig.4: Master Slave D Flip Flop using Pass Transistor

6. LAYOUT OF D FLIP FLOP

Before implementing the whole circuit, a gate-level schematic in DSCH3 is generated. DSCH3 program is a logic editor and simulator used to validate the architecture of logical circuit, before microelectronics started. It provides user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows design and validation of complex logic structures. After successful simulation we implemented the above designs of D Flip Flop with different components using Microwind 3 CMOS layout tool for its ease of use and availability. The result of the implementation is detailed below.

6.1 D Flip Flop layout using NAND Gate

Layout of LFSR counter in which D Flip flop is implemented using NAND gates is as shown in Fig. 5.

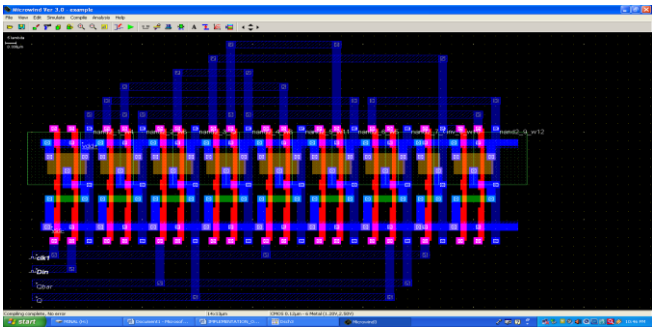

Fig.5: D Flip Flop layout using NAND Gate

6.2 D Flip Flop layout using TRANSMISSION Gate

Layout of LFSR counter in which D Flip flop is implemented using transmission gates is as shown Fig. 6.

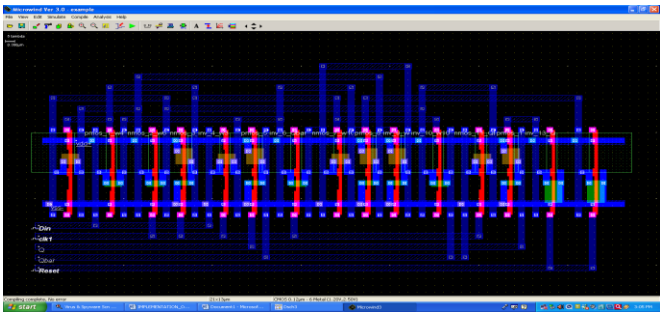

Fig.6: D Flip Flop layout using TRANSMISSION Gate

6.3 D Flip Flop layout using PASS Transistor

Layouts of LFSR counter in which D Flip Flop is implemented using transmission gates is as shown Fig. 7.

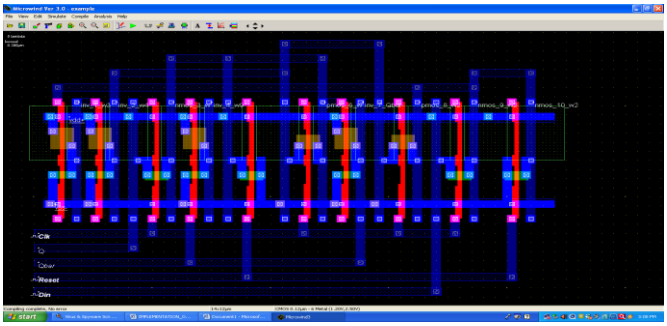

Fig.7. D Flip Flop layout using PASS Transistor

7. SIMULATION RESULT AND COMPARISON OF LFSR LAYOUT

In table we have compared layouts. The layouts are implemented in 120 nm technology. The varivous parameter because of different D Flip Flop is tabulated. CMOS layout of LFSR using pass transistors is as shown in fig.

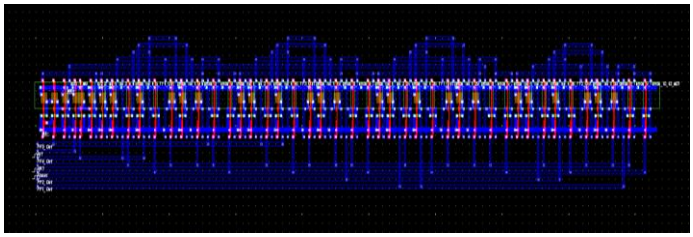

Fig.8: Layout of LFSR using pass transistors

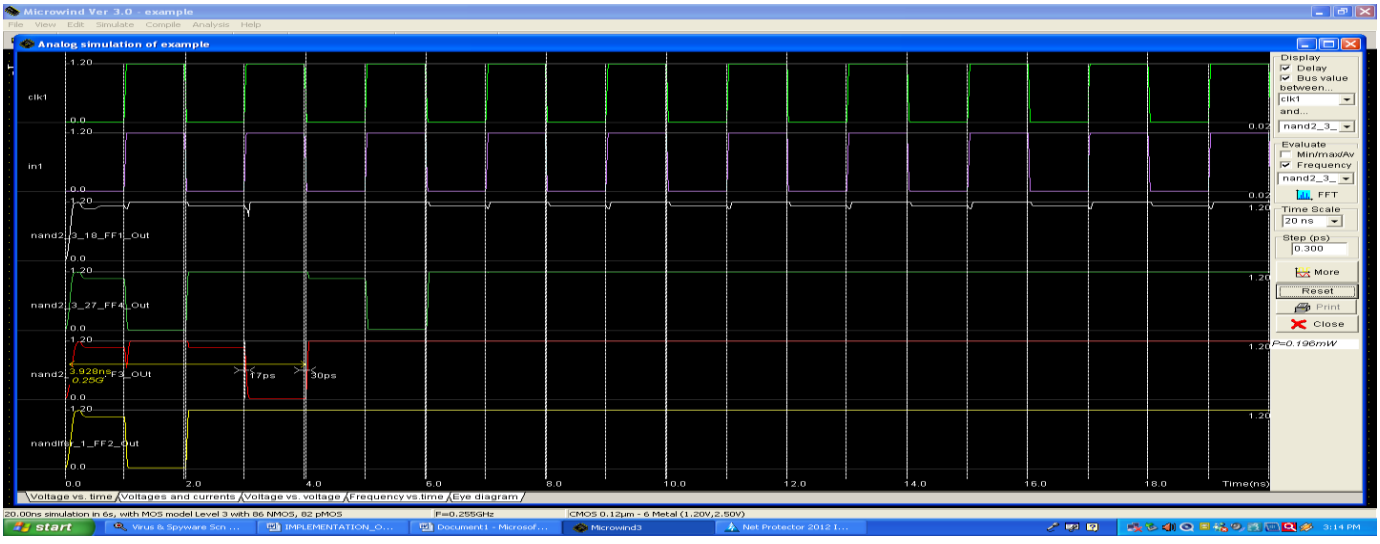

Fig.9: Simulation result of LFSR using NAND gate as component

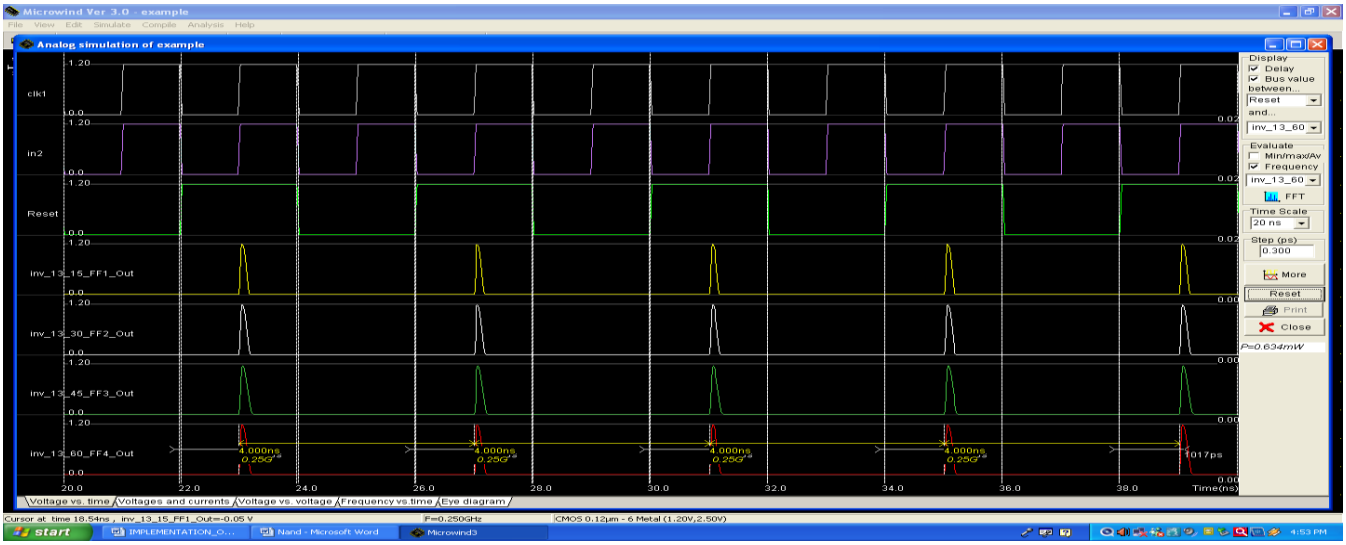

Fig.10: Simulation result of LFSR using Transmission Gate as component .

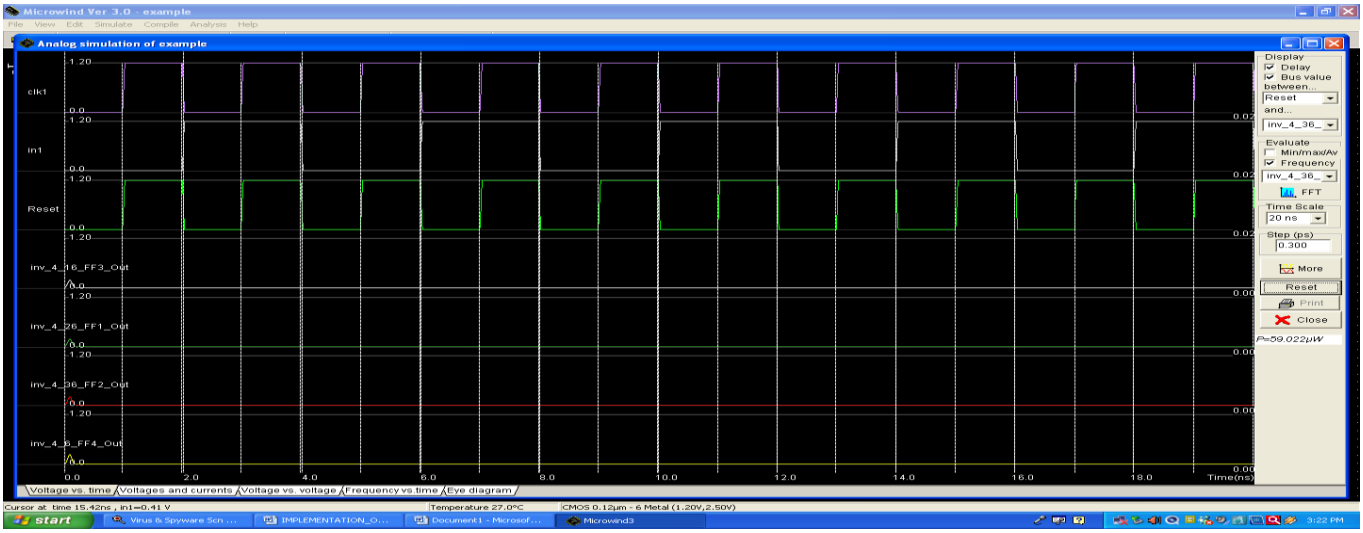

Fig.11: Simulation result of LFSR using Transmission Gate as component .

Table II: LFSR in 120 NM Technology

Components	No. of transistor	Power consumption (microwatt)	Max frequency (GHz)	Layout area (micro sq. meter)
NAND	**148**	**196**	**0.255**	**224.8**
Transmission Gate	**92**	**625**	**0.241**	**390.1**
Pass Transistor	**68**	**59.22**	**0.250**	**460**

8. CONCLUSION

This paper concludes that LFSR counter is best implemented using the pass transistors. In this the number of transistors required is minimum i.e. 19, power consumption is 59.22 micro watt , Max operating frequency is 0.241 GHz, layout size area is 460 micro sq. meter. Thus it is preferable over Gray counters in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & glitches. Thus LFSR implemented in CMOS chip technology, is the best illustration of VLSI. Further, such technology is highly utilized in the applications related to development of rural area.

9. REFERENCES

[1] N. A. Doshi, S. B. Dhobale, and S. R. Kakade," LFSR Counter Implementation in CMOS VLSI", World Academy of Science, Engineering and Technology 48 2008173

[2] Neil Weste, Harris and Banerjee, "CMOS VLSI design"

[3] Etienne Sicard and Sonia Delmas Bendhia ,"Basic CMOS Cell Design".

[4] Sung-MO Kang and Yusuf Leblebici,"CMOS Digital Integrated Circuits-Analysis and design".

[5] John F. Wakerly.K,"Digital Design-Principles and Practices".

[6] Neil Weste and Karmran, "Principles &Applications of CMOS Logic".

[7] James L. Massey,"On the Shift register Synthesis & BCH Decoding", IEEE Trans. Inform. Theory, vol. IT-15, n. 1, pp. 122-127, Jan 1969.

[8] "LFSR Layout Advance VLSI Design", Dept of Elect Engg.University of Houston.

[9] Arshdeep Singh, Oscar Servin, Edward Lee, Lutfi Bustami: A Project report of 4017 CMOS LED CHASERCOUNTER.

[10] A White Paper on "Linear Feedback Shift Registers and Cyclic Codes in SAGE Timothy Brian Brock. World Academy of Science, Engineering and Technology 48 2008172".

[11] Krishnendu Chakrabarty,Brian.Murray, and Vikram Iyengar:A white Paper on "Deterministic Built-in Test Pattern Generation for High-Performance Circuits Using Twisted- Ring Counters".

[12] Kazuo Yano, "Top down pass-Transistor Logic Design", IEEE Journal of solid-state circuits, vol-31,No-6, june 1996.

[13] Kazuo Yano,"A 3.8 CMOS 16 * 16 –b multiplier using complementary pass-transistor logic", IEEE Journal of solid-state circuits, vol-25,No-2,April 1990.

[14] Etienne Sicard ,"Micro wind User Manual".