A Novel Design of Low Power Adiabatic Inverter

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ABSTRACT
The growing market of mobile, battery-powered electronic systems demands the design of microelectronic circuits with low power dissipation. More generally, as density, size, and complexity of the chips continue to increase, the difficulty in providing proper cooling might either add significant cost or limit the functionality of the computing systems that make use of those integrated circuits. In this paper a new adiabatic inverter is proposed. Here the circuit of conventional positive feedback adiabatic (PFAL) inverter has been improved. The various improvement results are analyzed in Tanner EDA tool.

Keywords
Adiabatic, PFAL,VLSI, Recyclability.

1. INTRODUCTION
In the past years, several techniques, methodologies and tools for designing low-power circuits have been presented and proposed in the scientific literature. However, only a few of them have found their way in current design flows.

Green Computing is the study and practice of environmentally sustainable computing. The designing, manufacturing and using of computers, subsystems efficiently and effectively with minimal or no impact on the environment can be treated as the aim of green electronic computing. The goals of green computing are to reduce the use of hazardous materials, maximize energy efficiency and promote the recyclability.

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level[2]. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing various circuits. This is because all the important parameters governing power dissipation are strongly influenced by logic styles [3].

The logic style used in logic gates influences the speed, size, power dissipation, and the complexity level of a circuit. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes and intra- and inter-cell wiring capacitances. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. Power dissipation is determined by the switching activity and the node capacitances. All these characteristics may vary considerably from one logic style to another. The electronic devices dissipate heat energy to the environment .Hence the hotter ICs are a common concern for the environment as well. The dissipated energy contributes to the environment warming. The generalized power equation is stated as:$P=CV^2fa$. Hence power can be reduced classically by decreasing the capacitance involved in the path, scaling down the operating voltage, slowing down the operation of the circuit, reducing the activity factor of the chip. All these different approach needs different techniques for reducing power dissipation of the chip [4].

Adiabatic concept is one in which no heat is gained or lost by systems. The adiabatic concept is based upon the work of Landauer and Benett and is proving to be very fruitful in reducing the power levels[7]. These circuits can be broadly classified as semi or partial adiabatic and full or complete adiabatic circuits [8].

In this paper a new positive feedback inverter is introduced. The power dissipation and delay of the new logic are compared with conventional CMOS and other adiabatic inverters. NORgate and multiplexer are also implemented using PFAL and modified PFAL logic. Positive feedback adiabatic logic is a semi adiabatic approach which tries to increase the charging and discharging times maintaining the swing levels. It requires presence of complemented and un-complemented input. PFAL comes in dual rail logic family which requires availability of both the complementary and un-complementary inputs for the logic functions. The logic functions F and Fbar are implemented using NMOS networks alongside the two cross coupled inverts as latch known as sense amplifier which drives the two PMOS and two NMOS switches which ultimately prevents the output terminals from degradation of logic levels [8]. One of the logic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other function network provides a very high resistance in between the power clock and the other concerned output.

PFAL uses power clock instead of normal one as it is also used to energies logic networks. No extra dc power source is used and a time varying ac signal is used to actuate the circuit elements along with the clocking control. In PFAL a 4 phase clock is used. The four phases are namely ideal, evaluate, hold and recover stages. During evaluation phase the logic is evaluated as per the input vectors which is kept retained during the recover stage. But PFAL does not provide full recovery of charge and hence it is considered as partial recovery adiabatic logic family. Heat is dissipated during discharge cycle on the falling edge of the clock. Energy stored in capacitor does not need to be minimized, it is necessary to minimize energy wasted in the transistor network in order to achieve energy savings.

If the current is driven with a period T, the total power used in the circuit during a cycle can be proved as

$P=E/T=CV_{dd}^2/T$[8].

Where C is the value of load capacitor and V_{dd} is the power supply voltage.In adiabatic switching, we use lower frequency and constant current source to minimize power wastage.

In fig1 normal CMOS inverter with pull up and pull down network is shown.

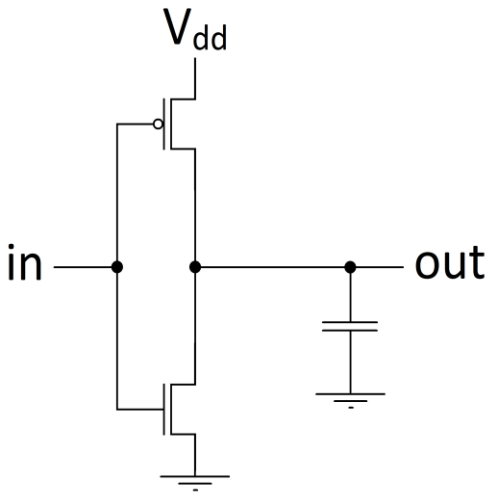

Fig 1.CMOS inverter

Pull up network brings the output capacitor voltage V_{dd} from zero by charging the capacitor voltage and pull down network brings the output capacitor voltage zero from V_{dd} by discharging the output capacitor voltage.

In normal or conventional charging constant voltage source is used to charge the load capacitance.

In fig2 the load capacitance is charged using constant voltage source.

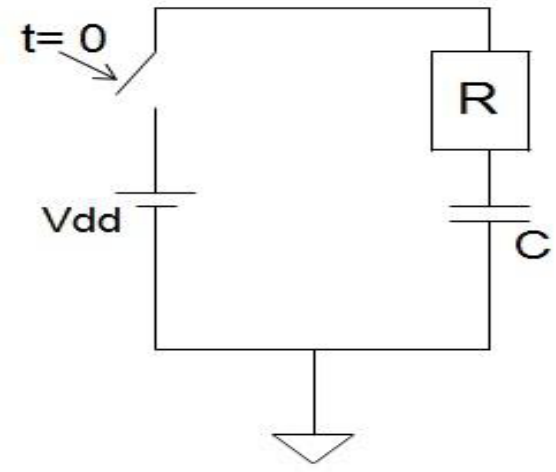

Fig 2.Conventinal charging

In adiabatic logic, load capacitance is charged by a constant current source instead of constant-voltage source as in the conventional circuit charging. A constant charging current corresponds to a linear ramp. Infig3 the circuit with constant current source, resistor and capacitor is shown. This circuit is used for adiabatic charging.

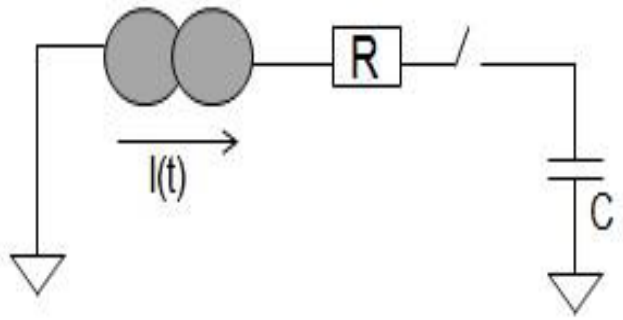

Fig 3.Adiabatic Charging

2. NEW ADIABATIC INVERTER

In this paper a new positive feedback adiabatic inverter is shown .The heart of all the PFAL logic is composed of a latch made by the two PMOS transistors M1-M2 and two NMOS transistors M3-M4.

In modified PFAL, the NMOS and PMOS of pull up and pull down networks are interchanged. Here power supply V_{DD} is used instead of power clock.

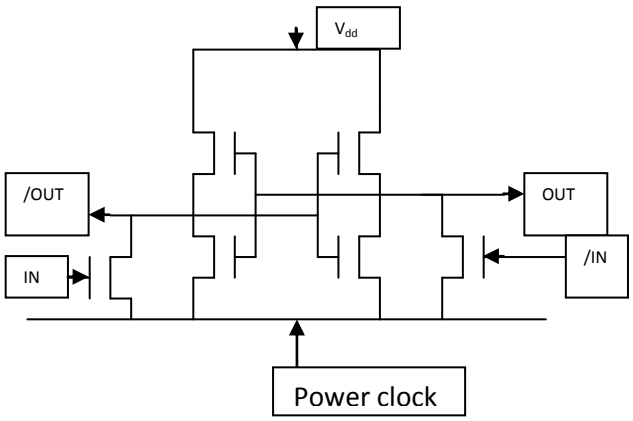

Fig 4.Modified PFAL inverter

The modified PFAL inverter uses a cross coupled latch connection to improve its efficiency.

3. SIMULATION RESULTS

The simulation is done by VLSI EDA Tool. Tanner SPICE is used for simulation.

Table1. Comparison of power dissipation between PFAL inverter and modified PFAL inverter

Inverter	Power dissipation at 200MHz
PFAL	9.75 µW
Modified PFAL	2.02 µW

In modified PFAL we have interchanged the NMOS and PMOS of pull up and pull down network. We connect power supply VDD instead of power clock. The Power saving is nearly76%. The modified PFAL inverter has very good low power characteristics. If various digital subsystems are built using this modified block more low power designs can be achieved.

Table2. Comparison of delay between PFAL inverter and modified PFAL inverter

Inverter	Delay(ns)
PFAL	1.82
Modified PFAL	0.98

Table3. Comparison of power dissipation between PFAL NOR gate and modified PFAL NOR gate

Circuit	Power dissipation at 50MHz
PFAL NOR	2.42 µW
modified PFAL NOR	0.507 µW

Table4. Comparison of power dissipation between PFAL MUX and modified PFAL MUX

Circuit	Power dissipation at 50MHz
PFAL 2:1 Mux	1.42 µW
Modified PFAL 2:1 Mux	0.407 µW

Table5. Comparison of power delay product of various adiabatic inverters

Inverter Circuit	PDP
2n2n2p	12.98
ECRL	10.43
PFAL	7.89
Modified PFAL	0.654

4. CONCLUSION

From the simulation results it is found that modified PFAL inverter has better performance than the normal PFAL inverter. The modified PFAL inverter has 70% less power dissipation over PFAL inverter. The delay characteristics is nearly 98% better in modified PFAL inverter. The modified PFAL universal gate (NOR) has 70% less power dissipation and modified PFAL 2:1MUX has 71% less power dissipation over normal PFAL circuits. Modified PFAL has better low power characteristics.

5. REFERENCES

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