Study and Design of Low Power Universal Differential Current Conveyor

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ABSTRACT
In this paper very low power CMOS universal differential difference current conveyor is designed. This is regarded as current mode circuits can be used for wireless communication. The gain, 3db bandwidth ,unity gain bandwidth, slew rate and phase margin at non inverting terminal was calculated as of 32.33dB, 781MHz, 24 GHz, 934V/ms and 47 degree. The gain, 3db bandwidth ,unity gain bandwidth, slew rate and phase margin at inverting terminal was calculated as of 30dB, 756MHz, 15.3 GHz, 934V/ms and 32.4 degree .The circuit was simulated using Cadence analog and digital design tools. The used technology is gpdk 45nm.

Keywords
Operational amplifiers (OP-AMPs), Current conveyor (CCII), Differential difference current conveyor (DDCC), Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS).

1. INTRODUCTION
Operational amplifier played unmatched significances in the world of analog electronics. It served as building block for designing of many types of equipment like filters and oscillators which are specified in literature. However, traditional OP-AMPs have some drawbacks like limited bandwidth, gain and slew-rate. So, to facing these difficulties in electronics worlds current-mode circuits came into existence which brought revolution in this area. In last few decades several new circuits were introduced and they gathered attention due to their wide dynamic range, greater linearity, larger signal bandwidth, simple circuitry and very-low power consumption. Among all these current mode circuits the active circuitry introduced by Sedra and Smith in 1970 [1] which was second generation current conveyor (CCII) marked there long term presence due to their high-performance in circuits analysis. Many circuits were realized with the help of CCII which depicts the era of these current-conveyors [2-4]. Though CCII had many advantages but the only drawback rose that it had only one input terminal, so it became unsuitable for some conditions when there was differential inputs and floating inputs. At this situation there was need of two CCIIs. So, the concept of differential difference current conveyor came into existence which combines the advantages CCII and differential difference amplifier (DDA).CCII encompasses the advantages as accuracy, bandwidth and high gain.DDA advantages are less number of components and capability to perform arithmetic operations. DDCC comprises of number of applications as square rooter, squarer, multiplier, current and voltage mode low pass filters and high pass filters [5].After a couple of few years many circuits were simulated and presented with DDCC as useful basic circuitry [6-10].In this paper we have simulated universal DDCC which is enhanced version of previous existing one consisting of two output terminals.

2. CIRCUIT DESIGN AND ANALYSIS
The DDCC stated in Fig.1 is regarded as universal because it contains 4 input terminal(P1,P2,P3,Q) and 2 output terminal(OUT+ and OUT-) where positive and negative sign fairly indicates the configuration of DDCC. The inverting part is termed as DDCC- and non inverting part is termed as DDCC+. It consists of two both terminals inverting as well as non- inverting which makes it universal.

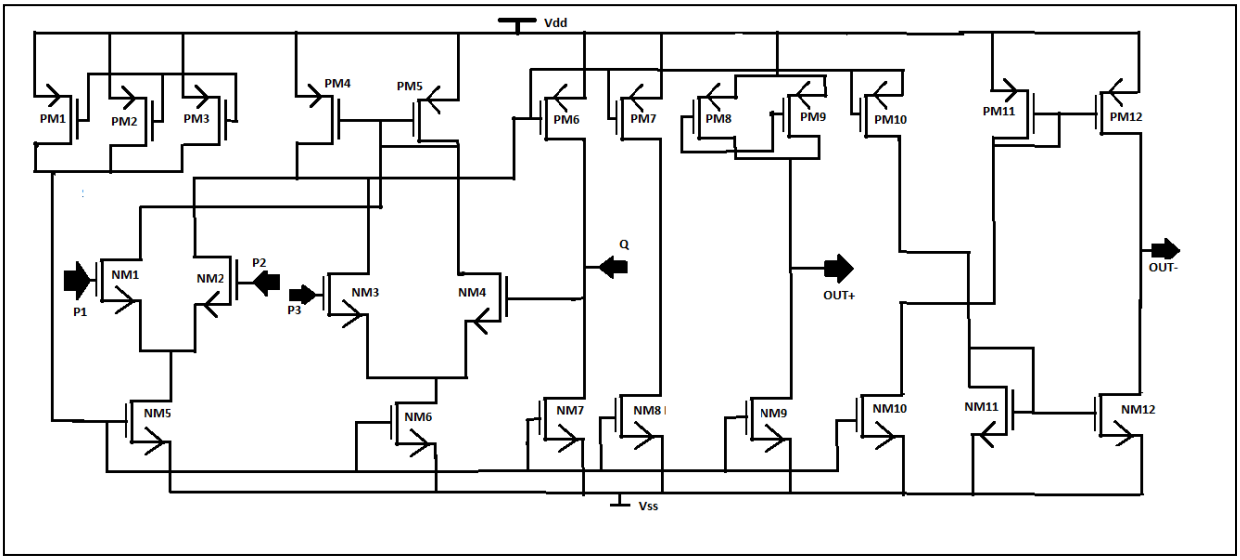

Fig. 1 Circuit Diagram of Universal DDCC

The circuit diagram of proposed CMOS universal DDCC circuit is stated in Fig. 1. The circuit consists of PMOS (PM1-PM12) and NMOS (NM1–NM12).The transistor PMOS (PM10-PM12) and transistor NMOS (NM10-NM12) is producing inverting output due to presence current mirror which produces negative current at OUT-.It is also provides the equal aspect ratio in both parallel transistor. The transistor NM1 and NM2 constitutes of two differential stages which realize the input transconductance. The presence of current mirror indicates similar current in parallel branch. It also provides the high gain stage and convert the differential current to single ended output current(PM6). The voltage at output terminal can be calculated by given equation

$$V_{OUT+}=X_0[(V_{P3}-V_{P1})-(V_{GNM4}-V_Q)] \quad (2)$$

Where, X_o represents the open loop gain of DDCC current conveyor based amplifier and V_{GNM4} represents gate voltage of NM4. Then we applied the negative feedback from output side of gain stage (node D) to input side (gate of MN4) [8]. The addition of inverting stage impacts the phase margin and makes circuit more stable. As we have used 45nm technology so the channel length is reduced to very much. It is also well known that cut off frequency of MOSFET transistor is depending on internal capacitance of transistor and the internal capacitances depends on the channel length as shown in following equations

$$f_T = \frac{g_m}{2\prod(C_{GS}+C_{DS})} \quad (3)$$

$$C_{GS} = C_{GD} = \frac{2}{3}wlc_{ox} \quad (4)$$

Where C_{GS} is gate to source capacitance, C_{DS} is drain to source capacitance C_{GD} is gate to drain capacitance, and f_T is cut off frequency of MOSFET. So, from equation (3) [11], as channel length get reduced the f_T will get increased. This shows a great impact on bandwidth of circuit. For the purpose of biasing we are used three MOSFETs which act as a current source instead of resister because it is advantageous when we are working for the purpose of layout and fabrication. In further stages of IC development resistors are avoided because of larger area and also complicacy in the circuit. The aspect (W/L) ratios of the MOSFETs at biasing stage can be calculated by given methods [12].

As, we know that transconductance (g_m)

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (5)$$

Similarly for transistor PM13

$$g_{mp13} = \frac{\partial}{\partial V_{GS}}[\frac{\mu_n c_{ox} w}{l}(V_{GS}-V_T)^2] \quad (6)$$

Since $$r_{on} = \frac{1}{g_{m13}} = \frac{l}{\mu_n c_{ox} w(V_{GS}-V_T)} \quad (7)$$

From the equation (7) it is seen that r_{on} is inversely proportional to transconductance and consequently become inversely proportional to aspect ratio *(w/l)*. Hence if aspect

ratio value is increased the value of the resistance is also decreased.

3. SIMULATION AND RESULTS

Theoretical analysis of proposed universal DDCC stated in Fig.1. was simulated and verified using Cadence analog and digital system design tools gpdk45nm technology. For simulation the used rail to rail supply voltage was ±1V.The gain, 3db bandwidth, unity gain bandwidth, slew rate and phase margin at non inverting terminal was calculated as of 32.33dB, 781MHz, 24 GHz, 934V/ms and 47 degree. The gain, 3db bandwidth ,unity gain bandwidth, slew rate and phase margin at inverting terminal was calculated as of 30dB, 756MHz, 15.3 GHz, 934V/ms and 32.4 degree .The transient response is stated in Fig.2 which depicts the inverting and non-inverting output. The AC Response of both inverting and non-inverting terminal is shown in fig.3. and fig.4. The simulation results and used supply voltage and technology are shown in Table 1.

Table 1. Performance analysis of proposed universal DDCC

Output Type	Non- inverting(O+)	Inverting(O-)
CMOS technology	45nm	45nm
Power Supply	$\pm 1V$	$\pm 1V$
3db Bandwidth	781 MHz	756 MHz
Unitygain bandwidth	24 GHz	15.3 GHz
Gain	32.33 dB	30 dB
Phase margin	47 deg	32.4 degree
Slew rate	934V/ms	934 V/ms

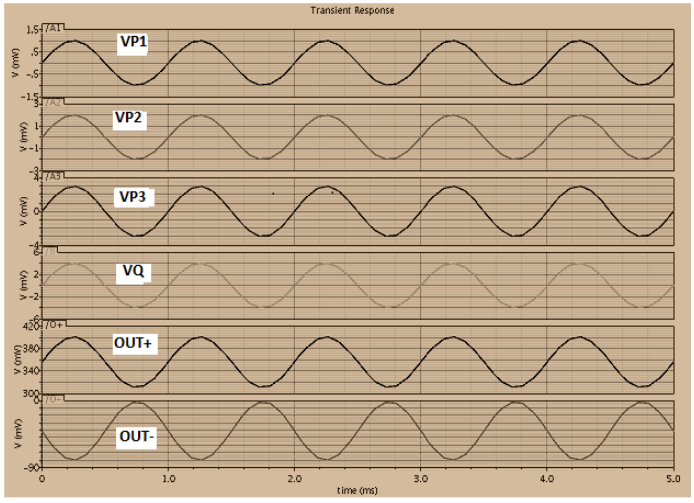

Fig.2.Transient response of proposed universal DDCC

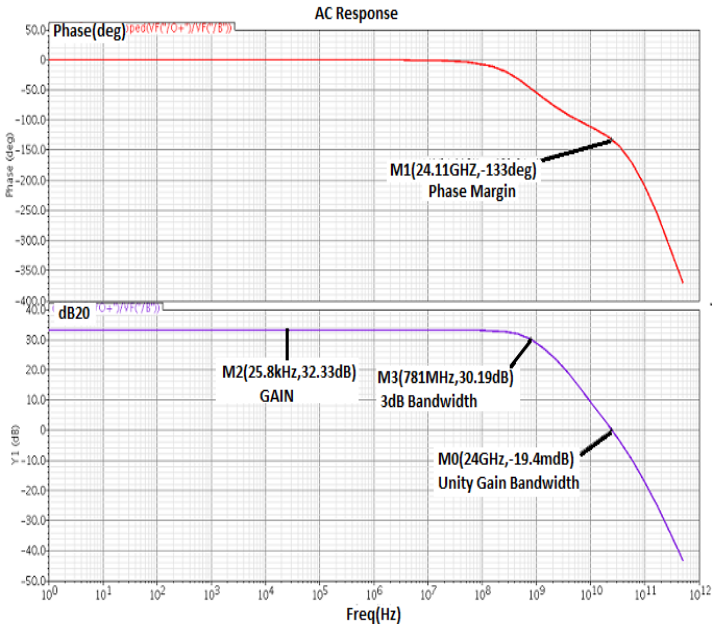

Fig.3. AC response of non-inverting terminal (OUT+) of proposed universal DDCC

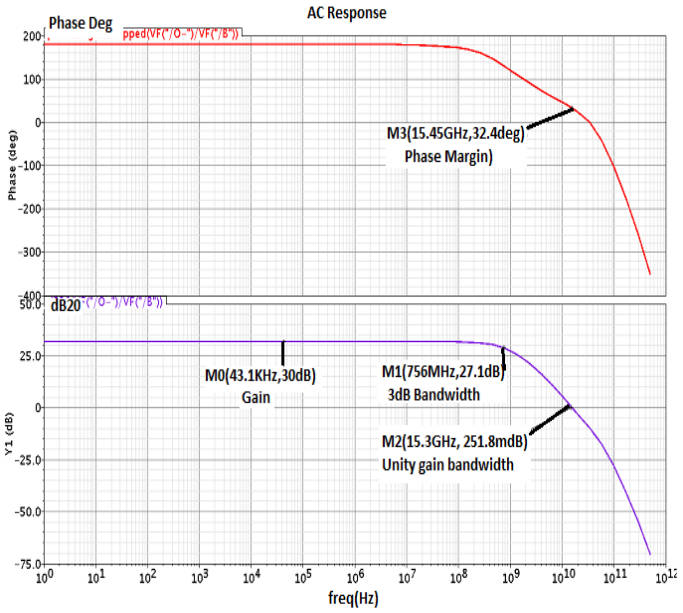

Fig.4. AC response of inverting terminal (OUT-) of proposed universal DDCC

4. CONCLUSION

In this universal DDCC was successfully simulated using Cadence analog and digital design tools. The technology used is gpdk 45nm technology. The designed DDCC is useful in designing of filter, oscillators and phase shifters. The used rail to rail power supply was ±1V. The gain, 3db bandwidth ,unity gain bandwidth, slew rate and phase margin at non inverting terminal was calculated as of 32.33dB, 781MHz, 24 GHz, 934V/ms and 47 degree. The gain, 3db bandwidth ,unity gain bandwidth, slew rate and phase margin at inverting terminal was calculated as of 30dB, 756MHz, 15.3 GHz, 934V/ms and 32.4degree. .

5. ACKNOWLEDGMENTS

We are thankful to Prof. P.K. Barhai, Vice-Chancellor, BIT Mesra and Prof. S.K. Ghorai, HOD ECE, BIT Mesra, for providing the infrastructure and encouragement. We are thankful to DST New Delhi and DRDL Hyderabad for funding for IC design tools like Cadence, Silvaco software to Dr. Vijay Nath, Principal Investigator of sanctioned project "Design of Ultra Low Power CMOS Cell for Temperature Sensor in VLSI".

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