Low Power Test Pattern Generator for System on Chip Architecture

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ABSTRACT
Low Power test pattern generator using a linear feedback shift register (LFSR), called LP-TGP is presented to reduce the average and peak power of a circuit during test. The correlation between two test patterns generated by LP-TPG is more than between the random patterns. The goal of having intermediate patterns is to reduce the transitional activities of primary inputs which reduces the switching activities inside the circuit under test and hence power consumption. An experimental result shows that proposed method gives 30.87% reduction in power during testing.

Keywords
built-in self-test; low power; single input pattern testing; switching activity.

1. INTRODUCTION
Today's system-on-chips (SoCs) design and test confront several problems, especially power dissipation. Generally, power dissipation of a system in test mode is more than in normal mode [1]. This is because a significant correlation exists between consecutive vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in the test mode. Reduced correlation between the consecutive test vectors increases the switching activity and eventually the power dissipation in the circuit. The second reason of increasing the power dissipation during test is because the test engineers may test cores in parallel to reduce the test application time. This extra power (average or peak) can cause problems such as instantaneous power surge that causes circuit damage, difficulty in performance verification and decreased overall product yield and cost. Low power test application has become important in today's VLSI design and test.

Built-In Self-Test (BIST) has emerged as a promising solution to the VLSI testing problems. BIST is a DFT methodology aimed at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as improved testability, at-speed testing and reduced need for automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates test patterns and a multiple input shift register (MISR) compacts test responses. Test vectors applied to a circuit under test at nominal operating frequency may have more average and/or peak power dissipation than those in normal mode. The reason is that the random nature of patterns reduces the correlation between the pseudorandom patterns generated by LFSR compared to normal functional vectors. It results in more switching and power dissipation in test mode.

However, there are some major drawbacks for this BIST whose architecture is based on the linear feedback shift register (LFSR). One is that the BIST circuit introduces more switching activities in the circuit under test during test than that during normal operation [3]. That can cause excessive power dissipation, and results in delay penalty into the design [4]. To lower the power in test mode, many techniques have been proposed to reduce the switching activities of test pattern. For LFSR based test pattern generator (TPG), Guiller proposed a modified clock scheme for liner feedback shift register (LFSR), so that only half of the D flip-flops works during each test period, thus only half of the test pattern can be switched [5].

Single input change sequence technique is a better low power approach which greatly decreases the transitions of inputs to reduce the internal switching activities. In [6], [7], the combination of LFSR and scan shift registers is used to generate random single input change sequences. In [4], a pseudo single input change sequence technique is proposed by adding an extra cyclic shift register and XOR gates, so that 2n -1 single input change test vectors can be inserted between two neighbour vectors generated by LFSR, n is the length of LFSR. Thus average power is reduced. The drawback of this methodology is that the test vectors' switching activities will still be very large if the test clock frequency is very high since the seed changes every 2n clock period.

In [2], the combination of LFSR and single input changing generator to generator random single input change sequence. Here the LFSR which is the combination of type-I LFSR and several X-OR gates. Here the main drawback is that the type-I LFSR produces only the correct quotient not the correct reminder for polynomial division [8].

In this paper we slightly modifies the type-I LFSR to type-II LFSR which generates more efficient single input change test patterns with single input changing generator (SICG), which includes an n-bit counter and n-bit grey encoder and 2n single input changing data are generated. Then the single input changing data is exclusive-ORed with the seed generated by the LFSR. For n-bit LFSR, the largest non-related random data is inserted between two neighbouring seeds, thus 2n * (2n-1) single input changing test vectors can be generated. In this method the seed generated by the modified LFSR will be changed every 2m (m<=n) clock period, so it is very suitable for BIST in very large scale sequential circuits especially SOC.

The rest of the paper is organized as follows. Section II gives an overview of test power analysis. Section III presents the proposed LP-TPG architecture. Section IV describes the experimental results and discussion. Section V summarizes the concluding remarks.

2. TEST POWER ANALYSIS

Power in electronic devices is defined as the conversion of electrical energy of power supply to heat. Equation (1) represents the power dissipation in electric circuits [9].

$$P=V.I \quad (1)$$

where:

V = Voltage (Joules/Coulomb or Volts)

I = Current (Coulombs/Sec or Amperes)

P = Power (Joules/Sec or Watts)

CMOS technology is the best choice for low-power designs because of its insignificant static power dissipation. However, simply selecting CMOS technology should not be considered as the only method for reducing power in ASIC/SOC devices. Since most of today's designs are based on CMOS technology, the first step toward power reduction is to understand the sources of power dissipation in such devices. Power consumption sources in digital CMOS circuits are divided into three main categories:

- Static power dissipation
- Short-circuit power dissipation
- Dynamic power dissipation

Equation (2) illustrates the relationship between these three parameters.

$$P_{Average}=P_{Static}+P_{Dynamic}+P_{Short\ circuit} \quad (2)$$

CMOS devices have very low-static power dissipation and most of the energy in them is used to charge and discharge load capacitances. By comparison, the short-circuit and static powers are usually of smaller magnitude than the dynamic power, and they can be ignored. Therefore, dynamic power is the principal source of power dissipation in CMOS devices. The following sections explain each of these power dissipation sources in detail.

A. Static Power Dissipation

Static power dissipation occurs when the logic-gate output is stable; thus it is frequency independent. Equation (3) represents the static power components.

$$P_{Static}=V_{DD} . I_{leakage} \quad (3)$$

Leakage current is caused by sub-threshold-transistor operations and is determined by device technology. This type of current is responsible for power dissipation when a CMOS device is inactive and its value is insignificant (less than 1 percent) when the device is active. Therefore, the large amount of leakage current, or static power, accordingly is an indication of a serious design problem, such as static inputs that do not turn a gate on or off properly. Static power dissipation in CMOS devices is usually negligible, because the amount of leakage current can be decreased significantly by choosing appropriate device technologies.

B. Short-Circuit Power Dissipation

Short-circuit power dissipation occurs when current flows from power supply (VDD) to ground (GND) during switching. The value of short-circuit dissipation depends on the amount of short-circuit current flowing to GND and it accounts for almost 10 percent of CMOS power consumption. Equation (4) represents the short-circuit power dissipation.

$$P_{Short\ Circuit} = V_{DD} . I_{Short\ Circuit} \quad (4)$$

Short-circuit current decreases when a large capacitive load is seen by the output of a gate and is at its maximum value when there is no capacitive load.

C. Dynamic Power Dissipation

Dynamic power is the dominant source of power dissipation in CMOS devices and accounts for approximately 90 percent of overall CMOS power consumption. It occurs during the switching of logic gates, and as a result, this type of power dissipation is frequency dependent. Dynamic power is therefore the average power required to perform all the switching events across the circuit. Equation (5) defines various parameters of dynamic power dissipation.

$$P_{Dynamic} = \frac{1}{2} . \beta . C . V_{DD}^2 . F \quad (5)$$

where:

β = Switching Activity per Node

C = Switched Capacitance

F = Frequency (switching events per second)

V_{DD} = Supply Voltage

From the above equation it is evident that dynamic power can be reduced by lowering the supply voltage, switched capacitance, switching activity per node, or frequency of signal transitions from 0 to 1 or vice versa. It is also apparent from Equation that the most effective and simple way of reducing dynamic power dissipation is by lowering the supply voltage (if the option of choosing lower voltage is available for a device). This is due to the squared effect of VDD. The other three terms in the above equation influence the overall power dissipation linearly.

The switching activity β determines the amount of switching that occurs in each node. Lowering this parameter decreases the useless transitions. β can be estimated statistically or captured from simulation traces (for example in Verilog, a.vcd file). Frequency represents the switching events per second. Since dynamic power is frequency dependent, frequency reduction is a key concept in power optimization. Clocks are the major contributors to the frequency component of Equation 5. However, other signals such as bus interconnects signals contribute to high-frequency activity and should be lowered to optimize power. Switched capacitance (C) can be either estimated based upon statistical models or measured from an actual layout database. Switched capacitance can be lowered by using shorter interconnect wires and smaller devices.

3. PROPOSED LP-TPG ARCHITECTURE

LFSR is widely used as test pattern generator because of its small circuit area and excellent random characteristics. Modified LFSR is used as the seed generator in this paper. As shown in Figure 1, the proposed architecture [2] which is called Low Power TPG consists of a seed generator (SG), an n-bit counter, a gray encoder and an exclusive-OR array. The n-bit counter and gray encoder generate single input changing patterns.

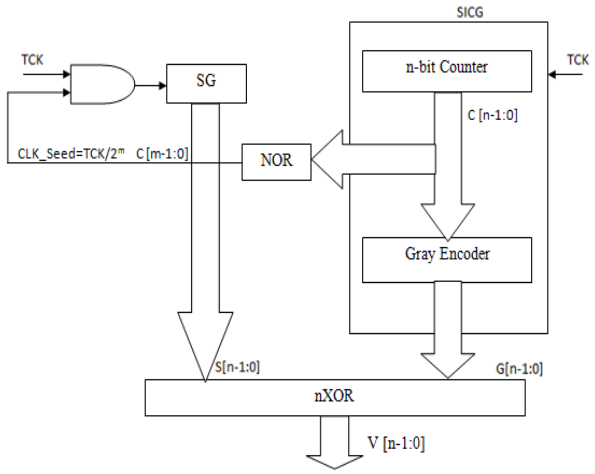

Figure 1.Structure of Low Power Test Pattern Generator

According to proposed structure of LP-TPG C[n-1:0] is the counter output and G[n-1:0] is the gray encoder output. The counter and SG are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates 2n continuous binary data periodically. The output of NOR operation of C[m-1:0] will be the clock control signal of SG where m<=n. It can be found obviously that SG will generate the next seed only when C[m-1:0] are all '0' and NOR output changes to '1'. The period of the single input changing sequences will be 2m.

Gray encoder in Fig. 1 is used to encode the counters output C[n-1:0] so that two successive values of its output G[n-1:0] will differ in only one bit. Gray encoder can be implemented by following equations.

G[0] = C[0] XOR C[1]
G[1] = C[1] XOR C[2]
G[2] = C[2] XOR C[3]
…….
G[n-2] = C[n-2] XOR C[n-1]
G[n-1] = C[n-1]

The seed generating circuit SG is a modified LFSR which is the combination of a Type-II LFSR and several XOR gates. The theory in [12] stated that the conventional LFSR's outputs can't be taken as the seed directly, because some seeds may share the same vectors. So the seed generator circuit should make sure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. The final test patterns are implemented as following equations.

V[0] = S[0] XOR G[0]
V[1] = S[1] XOR G[1]
V[2] = S[2] XOR G[2]
…
V[n-1] = S[n-1] XOR G[n-1]

The SG's clock will be TCK/2m due to the control signal. As SICG's cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too.

TABLE I

AN EXAMPLE OF GRAY ENCODER OUTPUT (N=4)

C[3:0]	G[3:0]
C0=0000	G0=0000
C1=0001	G1=0001
C2=0010	G2=0011
C3=0011	G3=0010
C4=0100	G4=0110
C5=0101	G5=0111
C6=0110	G6=0101
C7=0111	G7=0100
C8=1000	G8=1100
C9=1001	G9=1101
C10=1010	G10=1111
C11=1011	G11=1110
C12=1100	G12=1010
C13=1101	G13=1011
C14=1110	G14=1001
C15=1111	G15=1000

Table I is an example of counter and gray encoder's output when n=4 and m=3. The seed does not change in a cycle when C[2:0] ="000", and it will only switch to another vector when C[2:0] ="000". It can be found that all values of G[3:0] are single input changing patterns.

Table II is an example of 4 bit single input changing sequence with the seed S0 "0000" and with the seed S1 "0101" when n=4 and m=3. The period of the single input changing sequences will be 8. 4-bit gray encoder output sequence in Table I is {0000, 0001, 0011, 0010, 0110, 0111… 1000}. The chosen seeds S0 and S1 are {0000} and {0101}. S0 will be exclusive-ORed with sequence {0000, 0001, 0011 … 0100} and generates the SICG single input changing sequence {0000, 0001, 0011, 0110, 0111, 0101, 0100}, S1 will be exclusive-ORed with sequence {1100, 1101, 1111 …1000} and generates the SICG single input changing sequence {1001, 1000, 1010, 1011, 1111, 1110, 1100, 1101}. As an example, two well chosen seeds guarantee two single input changing sequences are unique.

TABLE II

AN EXAMPLE OF 4 BIT SINGLE INPUT CHANGE SEQUENCE (N=4, M=3)

S0=0000	S1=0101
V0=0000	V8=1001
V1=0001	V9=1000
V2=0011	V10=1010
V3=0010	V11=1011
V4=0110	V12=1111
V5=0111	V13=1110
V6=0101	V14=1100
V7=0100	V15=1101

Figure 2 is the circuit structure of single input changing generator (SICG), which consists of an n-bit counter and a gray code encoder.

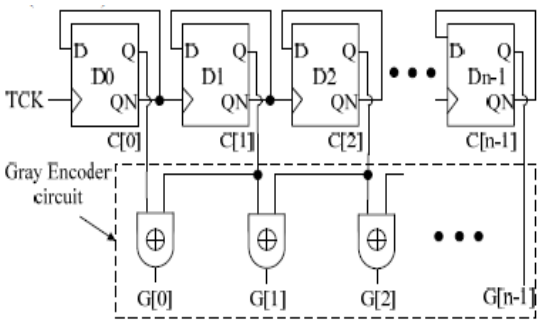

Figure 2.Single input change generator circuit (SICG)

The n-bit counter consists of n D flip-flops and the gray encoder consists of n-1 exclusive-OR gates. So the hardware overhead can be controlled under reasonable scope and the power consumption can be greatly reduced while the fault coverage is guaranteed. It is applicable for large scale circuits especially for SoC.

4. EXPERIMENTAL RESULTS

To validate the effectiveness of the proposed approach we select traditional LFSR technique for comparison, simulation and synthesis were carried out with Cadence SimVision and Cadence RTL Compiler GPDK 180nm CMOS library is used.

In our experimentation we used the polynomial x8+x6+x5+x+1 for both LFSR and LP-TPG. The test patterns are generated using an LFSR written in venilog program. As we used 8-bit LFSR it counts upto (28-1) i.e. 255 no. of stages. Figure 3 and 4 shows the simulation result of 8-bit Type-II LFSR and LP-TPG respectively.

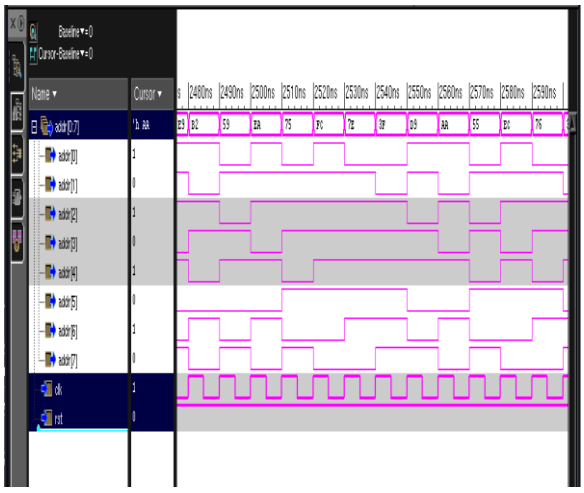

Figure 3. Simulation result of 8-bit Type-II LFSR

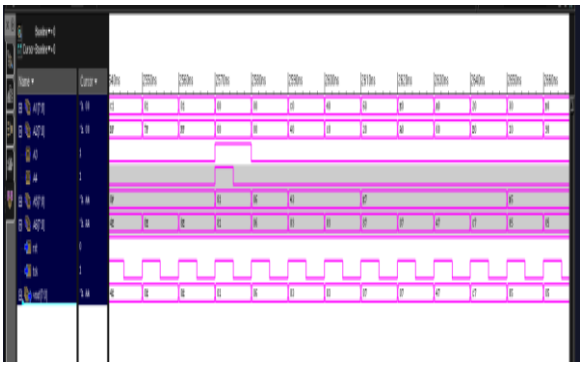

Figure 4. Simulation result of LP-TPG

Figure 5 and figure 6 shows synthesis report (power) of 8-bit Type II LFSR and LP-TPG respectively.

```
========================================
Generated by: Encounter(R) RTL Compiler
RC9.1.203 - v09.10-s242_1
Generated on: Apr 08 2012  03:28:12 PM
Module:lfsr1
Technology library:
scmetro_cmos10lp_rvt_ss_1p08v_125c 1.0
Operating conditions:   ss_1p08v_125c
(balanced tree)
Wireload mode:  enclosed
Area mode: timing library
========================================


                Leakage   Dynamic   Total
Instance Cells Power(nW) Power(nW) Power(nW)
----------------------------------------
lfsr1        8    45.427 50632.855 50678.282
```

Figure 5. Synthesis report of 8-bit Type-II LFSR

```
============================================
  Generated by: Encounter(R) RTL Compiler
RC9.1.203 - v09.10-s242_1
  Generated on: Apr 09 2012  02:39:17 PM
  Module:   tpg
  Technology library:
scmetro_cmos10lp_rvt_ss_1p08v_125c 1.0
  Operating conditions:   ss_1p08v_125c
(balanced tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================

               Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
--------------------------------------------
tpg         42   158.120 34874.419 35032.540
  G1        22    79.283  9099.985  9179.268
    DFF0     1     6.404  6068.011  6074.415
    DFF7     1     6.235   357.634   363.869
    DFF2     1     6.195   328.923   335.119
    DFF6     1     6.192   325.599   331.791
    DFF3     1     6.160   361.834   367.994
    DFF5     1     6.151   363.753   369.903
    DFF4     1     6.133   437.473   443.606
    DFF1     1     6.121   371.916   378.037
  G4         8    43.575 20907.128 20950.703
  G5         8    27.808   309.524   337.332
  G2         3     5.991   192.433   198.424
  G3         1     1.463  3315.589  3317.053
```

Figure 6. Synthesis report of LP-TPG

Table III shows the comparison of experimental results of the test power consumption with the proposed method.

TABLE III
POWER CONSUMPTION COMPARISON

Circuit	Dynamic Power(nw)	Total Power(nw)
LFSR	50632.855	50678.282
LP-TPG	34874.419	35032.540
IMPROVEMENT (%)	31.12	30.87

In Table III the columns refers to the test power consumption with conventional Type-II LFSR circuit. It can be found that the LFSR circuit consumes 50.67 mw (50687.282nw) test power where as the LP-TPG circuit consumes 35.032mw (35032.54nw) test power with 30.87% improvement of power consumption during testing.

5. Conclusions

An efficient low power test pattern generator (LP-TPG) method had been proposed to reduce the test power and uses a modified pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus pseudo-random signal input changing sequences are generated, which greatly minimize circuit switching activities and test power. The experimental result shows 30.87% reduction in test power. LP-TPG also reduces the instantaneous power violation compared to conventional LFSR.

6. Acknowledgment

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7. References

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