Design of Reversible Code Converters for Quantum Computer based Systems

Manjula Gandhi S Assistant Professor (SG), Dept. of MCA, Coimbatore Institute of Technology, Coimbatore, India J Devishree Assistant Professor (SG), Dept. of EEE, Coimbatore Institute of Technology, Coimbatore, India

ABSTRACT

Reversible logic is one of the latest technologies having promising applications in Quantum Computing. Reversible code converters are a class of reversible circuits that are used to convert one type of code in to another. Code conversion is a widely used process in digital systems for reasons such as enhancing security of data, reducing the complexity of arithmetic operations and thereby reducing the hardware required. This paper presents the design of reversible code converters such as converting Binary to BCD code, BCD to excess-3 code, Binary to Gray code and BCD to Gray code. Circuits have been designed and synthesized using QCViewer. The circuits are evaluated in terms of number of qubits, ancilla inputs, garbage outputs and quantum cost.

General Terms

Quantum gates

Keywords

Code converters, Quantum Computer, Quantum Gates, Qubit, Reversible logic

1. INTRODUCTION

Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is there is a oneto-one mapping between the input and output vectors. For example, a single reversible circuit for converting a BCD to excess-3 code can convert a BCD to excess-3 code and an excess-3 code to BCD code whereas in digital systems one would need two different circuits for such a conversion [3].

R.Landauer [9] showed, the amount of energy (heat) dissipated for every irreversible bit operation is given by kTln2, where k is the Boltzmann's constant (1.3807*10 $^{23}\mathrm{JK}^{-1})$ and T is the operating temperature. At room temperature (300 K), kTln₂ is approximately 2.8 *10⁻²¹J, which is small but not negligible. He also showed that only the logically irreversible steps in a computation carry an unavoidable energy penalty. If one could compute entirely with reversible operations, there would be no lower limit on energy consumption. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [4], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. One of the emerging applications of reversible logic is in quantum computers [11]. A Quantum computer consists of quantum logic gates. The quantum logic gates perform elementary unitary operation on qubits [17]. In quantum computing, qubit represents the elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible in nature and hence quantum computers must be built from reversible logical components [5].

In Digital systems, there are wide varieties of binary codes such as binary coded decimal (BCD), excess-3 code, and Gray code and so on. Many times, it is required to convert one code to another. The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems. It is some time necessary to use the output of one system as the input to the other. The conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus a code converter is a circuit that makes the two systems compatible even though each uses the different code.

In this paper, the irreversible circuits for code converters in digital systems are converted into reversible circuits. Reversible circuits for converting Binary to BCD, BCD to excess 3 code, Binary to Gray and BCD to Gray are designed and synthesized using QCViewer [1]. Rest of the paper is organized as follow: Section 2 provides the necessary background on reversible logic along with the examples of popular quantum gates. Section 3 contains the Literature Survey. Reversible code converters are discussed in section 4. Result analysis of the proposed circuits is presented in section 5 and Conclusions in section 6.

2. BASIC DEFINITIONS OF REVERSIBLE LOGIC

In this section, basic definitions and ideas related to reversible logic are presented.

Definition 2.1

A Reversible gate is a k-input, k-output circuit that produces a unique output pattern for each possible input pattern. Reversible gates [12] are circuits in which the number of outputs is equal to the number of inputs and there is one to one correspondence between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa.

Definition 2.2

Unwanted or unused output of a reversible gate is known as Garbage output. More formally, the outputs, which are needed only to maintain reversibility, are called garbage outputs.

Definition 2.3

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number

of primitive reversible logic gates required to realize the circuit.

Now we define some popular reversible gates formally, those that are needed in our research, with appropriate figures, examples and their cost.

Definition 2.4

The basic and simplest Reversible gate is conventional NOT gate and is a 1*1 gate. The block diagram is given in Figure 1. The quantum cost of Reversible NOT gate is 1.

Fig 1: Reversible NOT gate

Definition 2.5

The block diagram for 2 * 2 Feynman gate, also known as Controlled NOT gate. This gate is one through because it passes one of its inputs. Every linear reversible function can be built by using only 2 * 2 Feynman gate and inverters. Since this is a 2 * 2 gate, the quantum cost is 1. The quantum circuit of Feynman gate is shown in Figure 2. The reasons to use this gate in reversible circuits are:

(i) Make the copy of an input (by putting any of the input a constant 0);

(ii) To invert an input bit (by putting any of the input a constant 1).

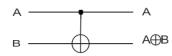


Fig 2: Quantum equivalent of Feynman gate

Definition 2.6

The input vector, I_V and output vector, O_V for 3*3 Toffoli gate [19]is defined as follows: Iv=(A,B,C) and $Ov=(P=A,Q=B,R=AB \oplus B)$. Toffoli gate plays an important role in the reversible logic synthesis. It is also used in the design of any Boolean function and hence it can be considered as a universal reversible gate. Figure 3shows the quantum realization of two qubit Toffoli gate, whose cost is 5. The quantum cost of three qubit Toffoli gate is 13.

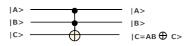


Fig 3: Toffoli Gate

3. LITERATURE SURVEY

Alexis De Vos [2] has shown that Conventional logic gates (e.g. AND gates) cannot be used for building a reversible computer. Both small building blocks and a more complex circuit in MOS technology have been presented. Rekha James et al., [14] proposed an implementation of Binary Coded Decimal adder in Reversible logic, which is basis of ALU for reversible CPU. Yvan Van Rentergem and Alexis De Vos [18] presented four designs for Reversible full-adder circuits and the implementation of these logic circuits into electronic circuitry based on CMOS technology and pass-transistor design. Majid Mohammadi et al., [10] proposed a synthesis method to realize a Reversible Binary Coded Decimal adder/subtractor circuit. Rangaraju et al. [16] have proposed a reversible eight-bit parallel Binary Adder/Subtractor with three designs. In all the three design approaches, the full Adder and Subtractor is realized in a single unit. The performance analysis is verified using number of reversible gates, Garbage input/outputs and Quantum cost and showed that their Design III is efficient. Krishnaveni et al., [8] have proposed a new reversible parallel adder/subtractor using 4*4 DKG gate, which can work as a reversible full adder and a full subtractor. Bhagyalakshmi et al., [6] have proposed a reversible design of a multiplier using DPG and BVF gate. Prashant et al. [13] presented a brief idea to build adder circuits using reversible gates like peres gate and TSG gate. Ravish, et al. proposed a reversible low power decoder [15]; circuits have been designed and synthesized using Revkit. Himanshu Thapliyal [7] has contributed more on Reversible circuits.Himanshi Thapliyal proposed a 3*3 Reversible TKS gate with two of its ouputs working as 2:1 multiplexer. The gate is used to design a reversible half adder and further used to design multiplexer based reversible full adder.

4. PROPOSED CIRCUITS

There are a wide variety of codes such as Binary-codeddecimal (BCD), Excess-3, Gray, etc. It is sometimes necessary to use the output of one system as the input to another. A conversion circuit should be inserted between the two systems if each uses different codes for the same information. Thus, a code converter is a circuit that makes the two systems compatible even though each uses a different binary code [3]. This particular section deals with various reversible code converters.

4.1 Binary to BCD Code

The quantum reversible circuit is presented in Figure 4. Total number of qubits is 17. The binary number which is passed as an input is set in qubits 1,2,4,6 and the output BCD number is measured in qubits 1, 10, 13, 14, 17. The input 1011 is passed in Qubits 1,2,4,6 respectively, and the output 11001 is measured in qubits 1, 10, 13, 14, 17. The input file contains 1>|0>|1>|1>|0>|1>|0>|0>|0>|0>|1>|0>|0>|1>|0>|0>|1>|1> and the measured output is duput is the provided output is the statement of the provided output is the statement of the provided output is the provided output is the statement of the provided output is the provided outp

|1>|0>|1>|0>|1>|0>|1>|0>|1>|0>|1>|0>|0>|0>|0>|0>|0>|1>|0>|1>.

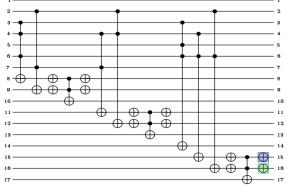


Fig 4: Reversible Circuit - Binary to BCD

4.2 Binary to Gray Code

 |1>|0>|1>|0>|1>|0>|1>.

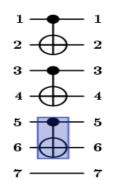


Fig 5: Reversible circuit - Binary to Gray

4.3 BCD to Excess-3 Code

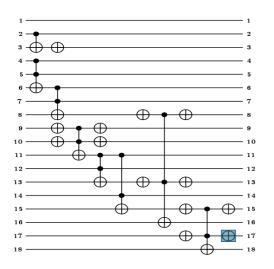


Fig 6: Reversible circuit - BCD to excess-3

4.4 BCD to Gray Code

Quantum reversible circuit is presented in Figure 7. The BCD code which is passed as an input is set in qubits 1, 2, 3, 6 and the output gray code is measured in qubits 2, 4, 7, 8. The reversible circuit in figure 7 has been designed and checked for all possible inputs. The input 1001 is passed in qubits 1, 2, 3, 6, and the output 1011 is measured in qubits 2, 4, 7, 8. The input file contains |1>|0>|0>|0>|1>|1>|1>|1> and the measured output is |1>|1>|0>|0>|0>|1>|1>|1>.

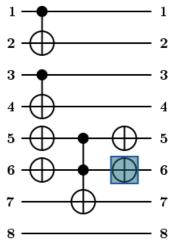


Fig 7: Reversible circuit - BCD to Gray

5. RESULTS

The quantum cost for the various reversible existing gates is given in Table 1. The quantum cost for the proposed reversible code conversion circuits is shown in Table 2 along with the number of NOT gates, number of CNOT gates and number of two (2Q) qubit and three qubit (3Q) toffoli gates used.

Table 1. Quantum gate cost

S.No	Gate	Cost
1	NOT gate	1
2	CNOT/Feynman gate	1
3	CCNOT/Toffoli gate	5
4	3 qubit Toffoli gate	13

Table 2. Quantum cost for proposed circuits

Reversible circuits	NOT gates	CNOT gates	CCNOT gates (2Q and 3Q)	Quantum Cost
Binary to BCD	12	0	8 and 2	78
Binary to Gray	0	3	0 and 0	3
BCD to Excess – 3 code	13	1	7 and 0	49
BCD to Gray	4	2	1 and 0	11

6. CONCLUSIONS AND FUTURE WORK

In this paper, reversible logic syntheses were carried out for various code converters. The designs have been developed for ease of reversible logic implementation. These circuits can be an important part of some other larger and more complex reversible circuits. Today, these circuits are useful in low-power digital electronics. Tomorrow, these may be useful in quantum computers. The quantum reversible circuits were synthesized using QCViewer [1]. In future, the proposed circuits can be implemented using optimized quantum gates and hence quantum cost can be reduced.

7. REFERENCES

- [1] Alex Parent and Jacob Parker, May 2012, QCviewer0.8, http://qcirc.iqc.uwaterloo.ca
- [2] De Vos, A. 2010. Reversible computer hardware. Electronic Notes in Theoretical Computer Science, 253(6), 17-22.
- [3] Godse, P.A , Godse, 2007, Digital Electronics, Technical Publications Pune.
- [4] Bennett, C. H. 1973. Logical reversibility of computation. IBM journal of Research and Development, 17(6), 525-532..
- [5] Bennett, C. H. 1988. Notes on the history of reversible computation. IBM Journal of Research and Development, 32(1), 16-23.
- [6] Bhagyalakshmi, H. R., & Venkatesha, M. K. 2010. An improved design of a multiplier using reversible logic gates. International journal of engineering science and technology, 2(8), 3838-3845.
- Thapliyal, H., & Srinivas, M. B. 2005, August. Novel design and reversible logic synthesis of multiplexer based full adder and multipliers. In Circuits and Systems, 2005. 48th Midwest Symposium on (pp. 1593-1596). IEEE.
- [8] Krishnaveni, D., & Geetha Priya, M. 2010. A Novel Design of Reversible Serial and Parallel Adder/Subtractor. International Journal of Engineering Science and Technology, 3, 2280-2288.

- [9] Landauer. R, 1961, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191.
- [10] Mohammadi, M., Eshghi, M., Haghparast, M., & Bahrololoom, A. (2008). Design and optimization of reversible BCD adder/subtractor circuit for quantum and nanotechnology based systems. World Applied Sciences Journal, 4(6), 787-792..
- [11] Nielsen, M. A., & Chuang, I. L. 2010. Quantum computation and quantum information. Cambridge university press.
- [12] Perkowski, M. 2000. Reversible Computation for Beginners. Lecture Series.
- [13] Yelekar R. P, Shiwande. S S, 2011, Introduction to Reversible Logic gates and its Application, 2nd National Conference on Information and Communication Technology, pp 5-9.
- [14] James, R. K., Shahana, T. K., Jacob, K. P., & Sasi, S. 2007, November. A new look at reversible logic implementation of decimal adder. In System-on-Chip, 2007 International Symposium on (pp. 1-4). IEEE.
- [15] Chinmaye, R., & Kn, M. 2012. Design, Optimization and Synthesis of Efficient Reversible Logic Binary Decoder. International Journal of Computer Applications, 46(6), 45-51.
- [16] Rangaraju, H. G., Venugopal, U., Muralidhara, K. N., & Raja, K. B. 2010. Low Power Reversible Parallel Binary Adder/Subtractor. arXiv preprint arXiv:1009.6218.
- [17] Sahni. V, 2007, "Quantum Computing", Tata McGraw-Hill, New Delhi, India.
- [18] Van Rentergem, Y., & De Vos, A. 2005. Optimal design of a reversible full adder. International Journal of Unconventional Computing, 1(4), 339.