Roadmap to the Modeling Approach and Design of RFCMOS Devices

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ABSTRACT
Requirements of RF CMOS device and its related design issues to operate at high frequencies are discussed. Problems faced by current CMOS models and its lack of accuracy in capturing high frequency are focused. To improve model accuracy, Vendor modeling approach is discussed to model frequency dependent parameters like substrate resistance, gate resistance and noise signals. In this connection, few design techniques of RF CMOS device to improve frequency dependent parameters are discussed. Limits possessed on CMOS scaling and an insight into the next generation CMOS devices have been overviewed.

General Terms
CMOS modeling at RF regime

Keywords
RF CMOS modeling, substrate and gate resistance modeling, design techniques of RF CMOS, Scaling, Multiple Gate MOSFET

1.INTRODUCTION
Personal computers and multimedia equipments demand high throughput and broad band wireless communications. The thirst for designing RF circuits to push the devices to operate at high frequency keeps growing. The physical realization of RF IC (Radio Frequency Integrated Circuit) design using CMOS devices offers several advantages including low cost, high integration, high noise immunity, low static power consumption and easy access to the technology[1]. But CMOS devices suffer from heavy substrate loss which has led to the development of GaAs and InP based devices. But still CMOS devices are preferred due to wide scaling possibilites which makes the device suitable for high frequency application by increasing trasistion frequency, f_t.

1.1 Requirements of RF CMOS Device
The primary requirement of RF CMOS device is that it should have lower channel length(L) and wider channel width(W). These make the device current to increase (1) which further increases f_t (2) and Unity power gain frequency, f_{max} (3). The drain current in saturation neglecting channel length modulation is given by

$I_D = k'(W/L)(V_G - V_t)^2$ ----------(1)

$f_t \alpha (1/L^2)$ ----------(2)

where k' = process transconductance (A/V^2);
V_G =Gate Voltage (V);V_t = Threshold Voltage (V);

$f_{max} \alpha (R_{out}/R_G)^{1/2}$ ----------(3)

Therefore it is evident from equation (2) and (3) that f_{max} can be improved by increasing Rout , the output resistance of the device with respect to the substrate and by decreasing the gate resistance (R_G) of CMOS device[2].

1.1.1 Increase the output resistance
High R_{out} means increasing the substrate resistance from source to bulk and from drain to bulk. Normally reverse biased junction capacitance C_{sb} & C_{db} ensures that there is a high resistance between active region and bulk.

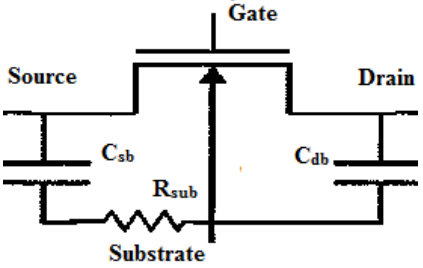

Fig. 1 Reverse biased junction Capacitance of MOSFET

1.1.2 Decrease the gate resistance
Lower gate resistance drives the MOSFET in high frequency operation and also it offers low delay to the input side of the MOSFET. Considering these, the paper discusses the problem faced in designing RF IC design and its related issues.

2. RF IC DESIGN
Each and every component of RF IC circuit has to be optimized to fit into RF frequency regime because in RF and millimeter frequency range, each section of semiconductor has distributed parasitic. This is the main difference between RF IC design and Digital IC design. This especially holds for active devices like CMOS transistor as they are the core device involved in amplification.

2.1 Issues in RF CMOS Device Modeling
Circuit engineers rely on circuit simulators for verification of their design before going to fabrication. Circuit simulators, in turn depend on device models to generate and construct circuits. This paper discuss mainly on the latest issues related to MOSFET models that are commonly used in circuit simulators.

It is found that always there is some sort of discrepancy exists in between the simulated output and the fabricated one (which is called the measured data). The reason for this discrepancy is that the core models used in the circuit simulator describe the behavior of devices operated in DC and low frequency regime. In real time, devices exhibit additional parasitic in all its terminals say, source, drain, gate and substrate resistances, capacitances and inductance effect due to high frequency

signal given to it. These effect are not captured by the available MOS models [3]. Also each section of the device has to be treated as transmission line models at RF regime which are again frequency dependent.

A few popular MOSFET models which lag behind the description of high frequency parasitics are listed in the Table 1.

2.2 Vendor Modeling Approach

Recent device models are based on semi empirical analytical modeling. This consists of a set of equations that are solved

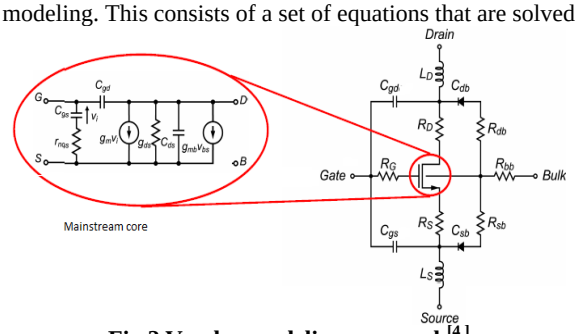

Fig.2 Vendor modeling approach[4]

by assigning the parameters. The model parameters are those values that are determined by experimental results. Parameters like process transconductance, body bias coefficient etc., are obtained from experimental results whereas high frequency related parasitic are not determined or computed in the model file. This is the lacking aspects in current model files and if they are used in simulation of RF circuit design then the simulated results would deviate from the measured results due to the inaccuracy of model files. So, many researchers worked on determining the gate and substrate resistance and it paved way to Vendor modeling approach[4].

Based on customer's (here Circuit designer) demand, certain vendors started working on the exploration of high frequency parasitics and included them in the core model. Fig.2 pictures clearly differentiate the mainstream core with its related parasitics. Following this vendor modeling approach, one could increase the accuracy of the existing devise models.

2.3 Substrate Resistance Modeling

Among the parasitic listed, substrate resistance and gate resistance are important as they determine the upper operating frequency of a device, given by equation (2) and (3). As these resistances are frequency dependent, device models should mandatorily update these resistances for its accuracy.

A small signal MOSFET model can be depicted as shown in Fig.3. Treating as two port network, y-parameters are derived as follows.

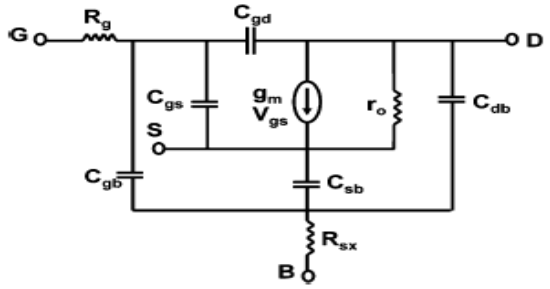

Fig.3 The small signal equivalent circuit of CMOS device

The substrate resistance [5] can be calculated using

$$R_{sx} = \frac{Real(y_{22})}{(img(y_{22}+y_{12}))^2} \qquad \text{----------(4)}$$

Equation (4) indicates clearly that substrate resistance depends on frequency and it adversely affect the device performance if the device is subjected to RF frequency signal and millimeter wave signal. The current models do not capture this degradation. Similarly the gate resistance do get change due to increase in signal frequency.

Paper [6] indicates that modern ICs suffer from resistive and capacitive couplings of interconnects with the substrate causing noise. This work is focused on modeling the distributed effects of a large interconnect parallel to substrate using the 3D boundary element method. This approach has a drawback that it is difficult to find noise injection areas and/or noise picking areas.

Another approach describes a physically based model for substrate resistance [7]. Because of the multifingered layout, the device sees multiple unequal paths through the substrate to the ground. The resulting network is computationally complex, so the authors have proposed to reduce this to few lumped resistances. That is, the path through the substrate is divided into two; one through the active area and the other is under the shallow trench isolation (STI).

Next, the design of scalable model of substrate resistance components for RF MOSFETs using bar type body contact set in horizontal direction to gate poly is attempted[8]. The model equations for substrate resistances based on number of fingers (N_f) for bar type body contacts are derived. The designed model is scalable not only for L, N_f and W_f but also for various layout dimensions, such as body-contact to active region distance and gate poly to gate poly distance.

Next the impact of substrate contact ring shape and its placement on the substrate are studied in [5]. Structures of varying shape of gate finger, substrate ring and the variation of substrate ring position relative to the device are fabricated and measured data of substrate resistance, f_t and f_{max} are obtained pertaining to 45 nm CMOS devices.

2.4 Gate Resistance Modeling

It is found in the literature that R_G also influences the performance of RF CMOS device. A physics-based effective gate resistance model [9] representing the non-quasi-static (NQS) effect and the distributed gate electrode resistance using 2-D simulations and extracted values are verified with experimental (measured) data. In addition, the effect of the gate resistance on the device noise behaviour has been studied.

Another approach deals with the characterisation of gate resistance of MOSFETs for various geometries [10] working at various bias conditions at high frequency (HF). Variation in the gate resistance with channel length and/or per finger width upto a critical dimension of L_f or W_f is presented. The results were based on measurements.

2.5 Modeling of Noise Sources

It is known that thermal noise prominently dominates in RF CMOS devices. So studies reveals that the drain channel noise, gate resistance noise and induced gate current noise are the common thermally generated noise sources that are to be

computed[2] and included in the small signal equivalent circuit representation.

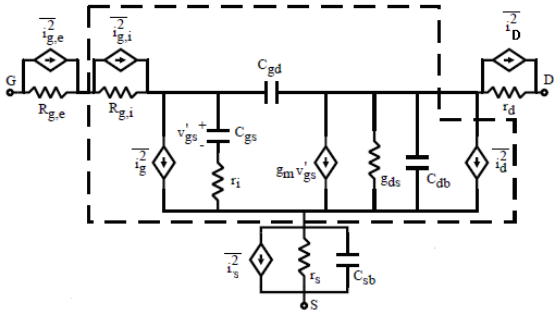

Fig.4 A complete small signal representation of RF CMOS device [2]

The noise sources occur in RF CMOS devices are thermal in origin. The generalised expression of noise source that are generated at the terminals of CMOS device is given by

$$\overline{i_x^2}=\frac{4kT}{R_x}\Delta f \qquad \text{---------- (5)}$$

where R_x =resistances at the terminals of MOS(Gate, Source to substrate resistance and Drain respectively)

K = Boltzmann's constant;
T=Temperature in Kelvin;
Δf = Bandwidth;

Generally the resistance at device terminal is divided into internal part (intrinsic or core part) and the external part(terminal resistance). Since the gate is wider, its resistances are subdivided into internal part(due to the distributed resistance at the gate) and the external part(terminal resistance) as shown in Fig.4.

Next prominent noise sources is the drain channel noise which is given by :

$$\overline{i_d^2}=4kT\gamma g_{do}\Delta f \qquad \text{----------(6)}$$

where g_{do}=Conductance of the channel at zero V_{DS}.The drain channel noise depends on the conductance of the channel.

And the next source is induced gate noise which is given by ;

$$\overline{i_g^2}=4kT\beta g_{do} r_i \omega C_{gs}\Delta f \qquad \text{----------(7)}$$

γ,β =Bias dependent parameter;
r_i =Channel charging resistance;
C_{gs} = Gate to Source capacitance

This is the noise current from the channel charging resistance and the distributed carriers in the channel that are capacitively coupled into gate through the gate capacitance.

The above equations[5]-[7] shows that the small signal noise parameters varies with temperature and frequency dependent resistance.

The above studies reveal that the substrate resistance, gate resistance and noise models have been carried out as a lumped element representation. Also the results are verified using measurement based data obtained after fabrication. If they are properly modeled including its distributed effects and included into the small signal representation, then the accuracy of resultant model increases.

3. FEW TECHNIQUES FOR THE DESIGN OF RF CMOS

CMOS technology is the most common technology whose concepts and fabrication steps are well analysed. It consists of a set of layers which defines a transistor. The procedural steps are understandable and hence its effect on the device performance can be predicted in advance. This type of modeling a device with respect to its associated fabrication modeling steps is called as '*Simulation- based modeling*' whereas if a device is fabricated and its parameters are measured by conducting suitable experiments using measuring equipment is called as '*Measurement-based modeling'*.

Simulation-based modeling is simple and cost effective, anyone who has better understanding on device fabrication can follow Simulation-based modeling. This is technology independent, application independent and applicable to any RF circuit. Whereas measurement based modeling approach is expensive as measuring equipments are costlier and it is technology based and application based. But in terms of accuracy of parameter, measurement-based modeling scheme offers reliable data, but restricts the flexibility in modeling.

3.1 Cancellation of Miller's Capacitance

Based on simulation based modeling, paper [11] suggest that layout of transistors connected in differential pair is adjusted so that the negative Miller capacitance is created thus cancelling the Miller's effect. This paper also suggests that metallization Capacitances can be extracted in layout level.

3.2 Multifinger Gate Structure

Since RF CMOS devices demands wider channel width, this increases the resistance of gate material which in turn increases the time delay. This can be mitigated by multifinger gate structures where the gate is splitted into number of fingers and these results in reduction of effective gate resistance[12].

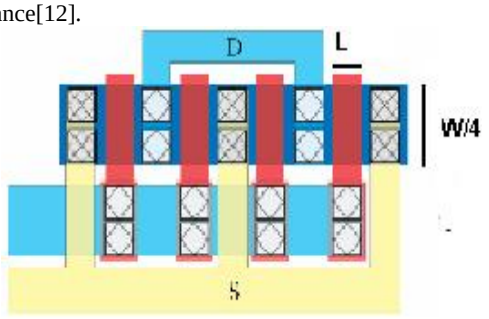

Fig.5 Multifinger gate structure

Four finger gate structure shown in Fig.5 depicts that the total width of transistor is divided by 4 whereas the length of the transistor remains the same. This reduces the effective gate resistance by 8.

Table 1: A short comparison of various device models

Parameter	**BSIM3**	**MOS Model 9**	**BSIM4**	**MOS Model 11**
Source and drain series resistance	RS & RD are included in IDC so, inaccuracy at HF			
Non-Quasi static model	NQS @ HF	No	NQS @ HF (with r_i)	NQS added using channel segmentation
Short channel effect	Includes SCE	No	Includes SCE(including tunneling)	Includes SCE
Gate and substrate resistance	No	No	included	included

3.3 Increasing the Output Resistance of RF CMOS Device

The output resistance of RF CMOS device can be improved by adjusting the doping profile and channel length. If the doping concentration decreases this may increase the space charge region of reverse biased p-n junction diode of active to bulk region. So C_{sb} or C_{db} decreases therby its reactance increases (resistance to leakage path).

But chances for increasing the channel charging resistance, r_i. This resistance is responsible for the delay in formation of charge layer in the channel and this is due to the effect of non-quasi static behaviour of MOSFET.

The next design issue is increasing the channel may decrease the channel length modulation effect which in turn increase the output resistance. But this forms the contradictory to requirement of RF CMOS device which needs shorter channel length for high frequency operation.

The above studies strongly recommend that layout of CMOS device can be altered to reduce the gate resistance and could increase the output resistance thereby reducing the noise. So layout of a device has strong dependence on its performance [13]. Several works has been done to add calculated parasitic to the available model resulting in the composite model. Then this model is tested for its accuracy by using in Low Noise Amplifiers[14].

4. ISSUES IN DEVCIE SCALING

4.1 Device Scaling Limit

CMOS scaling has allowed the transistor dimensions to be reduced to less than 100nm. As the dimensions are shrunk, the drain and source region come closer to each other and their respective potentials interact thus reducing the ability of the gate terminal to control the current flow in the channel. In this connection, few non linear effects such as Drain Induced Barrier Lowering (DIBL), body transconductance, velocity saturation, hot carrier effects, sub threshold voltage slope swing, band to band tunneling, etc. occur thus degrading the device performance. This forms the limits of cmos device scaling.

In order to reduce these non linear effects, As we scale down the channel length, oxide thickness (tox) can be reduced and corresponding substrate doping can be increased. These are done to ensure a perfect gate control over the channel. But reduction of oxide thickness causes significant gate current due to direct quantum tunneling. Similarly increase in the substrate doping causes reduction in carrier mobility and larger junction capacitance [15]-[17].Thus these factors limit further scaling of transistors.

4.2 Multigate Gate MOSFETs

One of the non-conventional solutions to overcome the non-linear effects due to scaling is the design of Multiple Gate structure, a new generation CMOS device. A prominent feature of the Multiple Gate MOSFETs is that they do not need heavy channel doping to reduce the non linear effects. Instead MG MOSFETs use thin body to mitigate the reverse biased p-n junction diodes formed between active and bulk region. Thus leakage paths are controlled and mobility degradation is also avoided. Various structures of Multiple Gate MOSFET have been proposed, such as Double Gate (DG), Surrounding Gate (SG), Triple Gate(TG), Triple Plus Gate(TPG) and Quadruple Gate(QG).

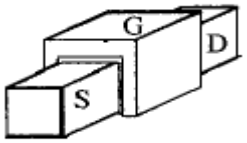

Fig. 6 Typical triple gate structure

Most of the research in constructing RF circuits and microcontrollers are on the line by IC manufacturing companies like AMD, Hitachi, IBM, Infineon Technologies, Intel Corporation, TSMC, University of California, Freescale Semiconductor etc., TPG draws attention and new products using TPG structure are yet to be released by INTEL [18].

5. CONCLUSION

It is understood from this study that the substrate and gate resistance determine the high frequency characterization of the RF CMOS device, say, ft and fmax. Based on the literature survey, a scalable substrate model and gate resistance models suitable for RF and millimetre wave frequency are required and they should be technology and application independent. Their distributed effects are yet to explored. Along with this, noise models are also should be included in the small signal parameters which vary with temperature and frequency dependent resistance. The

simulation-based modelling which is flexible and cost effective needs to be explored further to improve the model accuracy. Concepts of scaling RF CMOS device leads to the development of next generation CMOS devices, i.e., Multiple Gate Structured MOSFETs.

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