Modeling a Floating Gate EEPROM Device using Finite Element Analysis

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ABSTRACT
The present paper illustrates the modelling and simulation of an Electrically Erasable Programmable Read-Only-Memory (EEPROM) using COMSOL Multiphysics. The inbuilt stationary study computes the current voltage response of the device for both charged and uncharged cases of the floating gate. It is also illustrated herewith how time dependent studies on COMSOL Multiphysics are used to simulate the transient voltage pulses input at the control gate. It is also worth mentioning that EEPROM uses a FLOTOX (Floating Gate Tunnelling Oxide) device, which enables the pulses applied at the control gate to tunnel between the floating gate and the semiconductor material, thereby allowing storing or erasing a data. A write-erase cycle is performed, where the negative charges initially stored on the floating gate is subsequently removed by applying a high drain voltage and zero gate voltage. The model described here in the present paper is a single cell of an EEPROM, which has the capability to store only a single bit of data. As an extended version of this paper, many such cells can be connected together by using "enabling word lines" to simulate a large array of EEPROM. COMSOL Multiphysics provides us with a spice electrical circuit module which facilitates the connection of individual cells through nodes and terminals.

Index Terms
Electrically ErasableMemory (EEPROM), COMSOLMultiphysics,FLOTOX ((Floating Gate Tunnelling Oxide)

1. INTRODUCTION
The most relevant phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the flash memory market EEPROM devices are the building blocks of modern non-volatile. Moreover,

in the coming years, portable systems will consume more of these type of memories having either

high density and high writing throughput for data storage application or with fast random access for code execution in place. The strong consolidated know-how (with more than ten years of experience by many professionals), limitless inter flexibility, and the low cost make the Flash memory an immensely utilized, well consolidated and mature technology for most of the non-volatile memory applications. Nowadays, flash memories sales represent a lion's share of the overall semiconductor market. Even though different types of Flash cells/memories and architectures have been proposed, recently two of them are considered as industry standard: the common ground NOR Flash, because of its versatility it can address both the code as well as the data storage segments, and the NAND Flash which is optimized for the data storage market memory and is becoming an increasingly important storage medium for computers and mobile devices [1],[3],[4-8]. The current paper focus on the NOR type Flash memory or EEPROM, with the sole aim of learning the working mechanism of the device. Being electrically isolated, the FG acts as the storing for the cell device; charge injected in the FG is maintained there, allowing modulation of the "apparent" threshold voltage (i.e., seen from the CG) of the cell transistor. Obviously the quality of the dielectrics guarantees the non-volatility, while the thickness allows the possibility to program or erase the cell by electrical pulses/fields. Usually what happens is that, the gate dielectric (i.e., the one between the transistor channel and the FG) is an oxide in the range of 9–10 nm and is called "tunnel oxide" since FN electron tunneling occurs across it. Whereas, the dielectric that separates the FG from the CG is formed by a triple layer of oxide–nitride–oxide (ONO). The ONO thickness is in the range of 15–20 nm as compared to thickness of the oxide. ONO layer as inter-polysilicon dielectric has been introduced in order to improve the tunnel oxide quality. In fact, the use of thermal oxide polysilicon implies growth temperature higher than 1100 °C, impacting the underneath tunnel oxide [1],[2],[4], [7-10],[11],[12]. If the tunnel oxide and the ONO behave as ideal dielectrics, then once the charges are in the FG, the tunnel and ONO dielectrics form potential barriers. The neutral (or positively charged) state is associated with the logical state "1" and the negatively charged state, in accordance to electrons stored in the FG, is associated with the logical "0." Flash cells share the same gate, constitute the "word line (WL)", while those sharing same drain electrode constitute the "bit line (BL)". Such is the organization of cells and electrodes in flash memory arrays which is shown in figure 1.

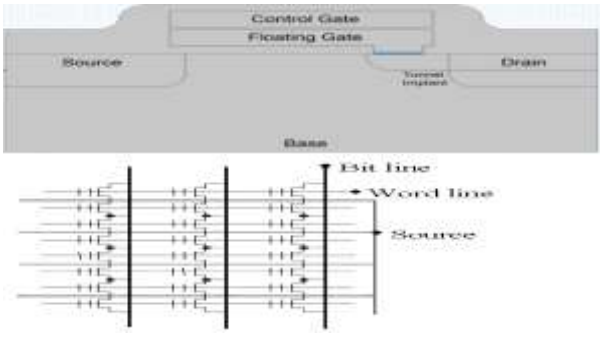

Figure 1. NOR flash array equivalent [6]

2. DESIGNING OF EEPROM CELL USING COMSOL MULTIPHYSICS

The basic structure of EEPROM is modelled using COMSOL Multiphysics and is shown in figure 2.

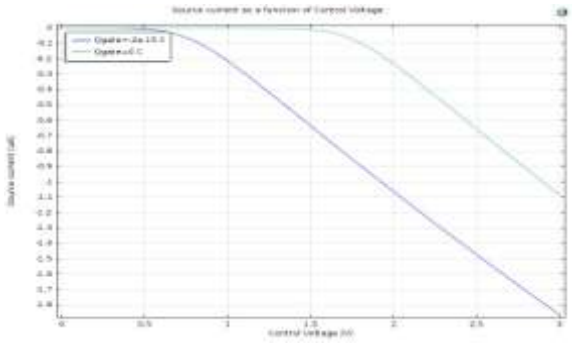

Figure 2. Designed model geometry showing key areas of the EEPROM. The tunnel barrier is highlighted in blue

The total length of the device is 1.8 μm with a channel length of 0.55 μm between the highly doped n-type regions. The source and drain contacts are 0.2 μm deep, with a shallower 0.1 μm deep tunnel implant protruding 0.25 μm from the drain region. The floating gate is separated from the channel by a 50 nm thick oxide layer, however directly above the tunnel implant the oxide thickness is only 8 nm. The 8 nm region serves a tunnel barrier between the MOSFET-like semiconductor device and the floating gate. When a voltage is applied to the control gate, the geometry of the floating gate serves to concentrate the resulting electric field in the region of the tunnel barrier. This can be seen in figure 4, which shows the electric field during the programming voltage pulse. Sufficiently large control voltages generate an electric field capable of causing electron tunneling across the tunnel barrier. To analyze the model three studies are done using the inbuilt function present in COMSOL Multiphysics.

2.1 Stationary, sweep V control for Qgate:

This study demonstrates the effect of varying the charge stored on the floating gate. Here, the source and base contacts are grounded, a fixed voltage of 10 mV is applied to the drain. For two different values of stored charge, 0 and $-2x10^{-15}$ C, the control gate voltage is swept from 0 to 3 V. The source current is plotted as a function of the control gate voltage for both values of stored charge.

2.2 Time dependent, program event: This study stores data

into the single bit EEPROM cell. The event can be described in brief, the control gate is maintained at a very high potential, while the drain current is maintained at a relatively lower potential. This in turn induces a very high electric field in the substrate near the tunnel barrier, the electrons moving from source to drain tunnels through the barrier and gets stored into the floating gate. The floating gate is negatively charged which corresponds to the charged state.

2.3 Time dependent, erase event: This particular study

empties or erases the charges stored in the floating gate by applying a subsequent zero voltage at the gate and a very high positive voltage at the drain terminal. This subsequent negative pulse causes these electrons to tunnel back out of the floating gate near to its initial condition; the erase state thus takes the "programmed state" as its initial condition.

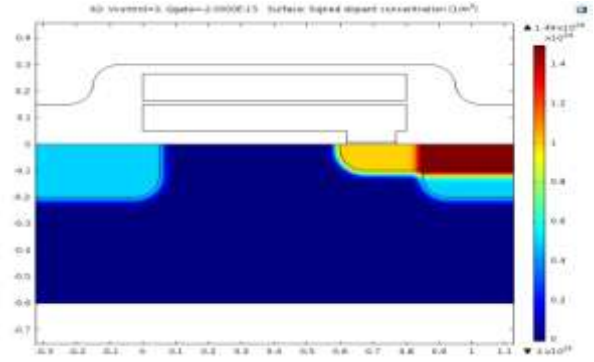

Figure 3. Surface plot showing electric field during the control voltage pulse used to program EEPROM device

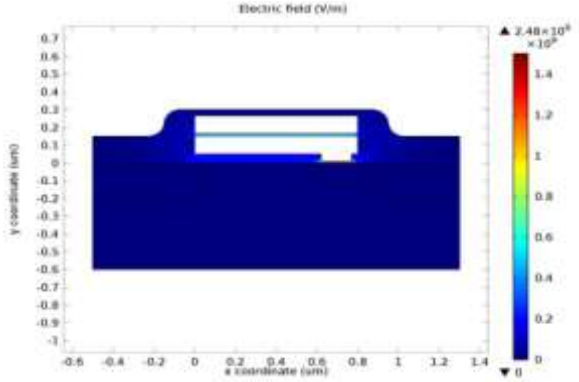

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Figure 4. Doping concentration across different EEPROM components for varied control gate voltage and charge

3. RESULTS AND DISCUSSION

Figure 4 shows the doping concentration in various areas of the EEPROM when Qgate is varied from 0 C to 15 C with a step of 2e C, and V control or control gate voltage is increased from 0 V to 3 V with a step of 0.1 V.

Figure 5 shows the current-voltage characteristics of the device for two different values of charge stored on the floating gate. As expected, the device behaves like a MOSFET, with no current flowing between the source and drain until a threshold "turn-on" control voltage is reached. This is because at the threshold voltage the electric field induces a thin inversion layer, in which the semiconductor changes from p-type to n-type, opening a conducting channel between the source and drain regions. As the control voltage increases past the threshold the width of the conducting channel increases, reducing the resistance between the source and drain contacts and allowing more current to flow for a given source-drain voltage. The stored charge changes the turn-on voltage, resulting in a different source-drain resistance for a given control voltage. By measuring the current at a given control and drain voltage it is thus possible to tell is charge is stored on the floating gate.

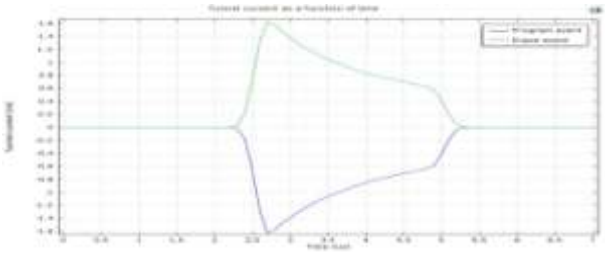

Figure 5.The green line shows the curve when the device is in the erased state. The blue line shows the curve when the device is in the programmed state

Figure 6 shows the tunnel current as a function of time throughout the program and erase events. During the program event electrons tunnel onto the floating gate, resulting in a conventional current with negative sign. When electrons tunnel back out of the floating gate during the erase event there is a positive current of equal magnitude to the program event.

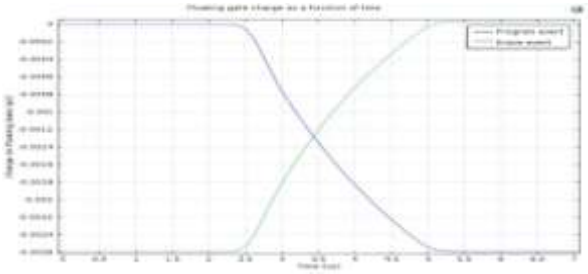

Figure 6: Charge on Floating Gate as a function of time for the program and erase events

Figure 6 shows the charge stored on the floating gate as a function of time throughout the program and erase Events. As the charge is due to electrons tunnelling through the tunnel barrier, the program event results in the accumulation of a negative charge on the floating gate and the erase event returns the charge to near zero.

4. CONCLUSION

Through this paper, a method of modelling EEPROM using COMSOL Multiphysics is highlighted The FLOTOX device type NOR array used in EEPROM have been designed and simulated in detail using the stationary sweep and the time dependent mode present in COMSOL software. Advanced features such as doping concentration, source current as a function of voltage, programming and erasing are described in detail. It is observed that tunnelling current plays an important role in both programming and erasing the cell without rupturing the thin oxide barrier.

5. REFERENCES

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