Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique

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ABSTRACT
This paper aims at reducing power and energy dissipation in Transmission Gate Logic (TGL) Multiplexer CMOS circuits comprise of reducing the power supply voltages, power supply current and delay with economical charge recovery logic. This paper designs an 8:1 Multiplexer with CMOS Transmission Gate Logic (TGL) using the Power Gating Technique, which reduces the leakage power and leakage current in active mode. Power Gating Technique uses Transmission Gate Logic (TGL) based an 8:1 multiplexer circuit which removes the degraded output. The PMOS and NMOS transistors are connected together for strong output level. Power gating technique achieves 36% reduction of leakage current and 43% reduction of leakage power in active mode, A the results of this paper are simulated on cadence virtuoso tool realized in 45nm technology with reduction of 4.021fW power, 7.381pA current and 0.7V supply voltage.

Keywords
Power Gating Technique, Transistor Gate Logic (TGL), Low Power, Leakage Circuit

1. INTRODUCTION
The paper makes an effort to increase prominence of transportable systems and wishes to limit power consumption which has light-emitting diode for speedy and innovative developments in low power VLSI design during the recent years. The developments include transportable device applications requiring low power consumption and high output because of their little chip size with large density of elements, redoubled complexity and high frequencies. An 8:1 Multiplexer may be the basic building block of the "switch logic". The Multiplexer circuit often wants to combine eight or a lot of digital signals onto one line, by inserting them there at totally different times. Technically, this can be referred to as time-division multiplexing. Multiplexers may also be used as programmable logic devices [1]. By specifying the logic arrangement within the input signals, a custom logic circuit is often created. The selector inputs then act as the logic inputs. This can be particularly helpful in things which price may be an issue and for modularity. So study on Multiplexer is inevitable [2] [3]. At the circuit design level, the key potential for power stake exists by suggesting the correct selection of a logic design for implementing combinative circuits. Exploration of low power logic designs within the analysis however has mainly focused on specific logic cell, namely Multiplexers, utilized in arithmetic circuits. At higher frequency the CMOS logic will operate continuously with low power consumption [4] [5]. The various methods are widely used for reducing power dissipation in circuits, reducing switching activities, supply voltages and load capacitances [6] [7]. Many leakage reduction techniques have area unit which cut back leakage power within the circuit to a significant level. Power Gating has become one amongst the foremost widely used circuit design techniques for reducing leakage current in power dissipation [8] [9]. This paper concentrates on reduction of leakage power that happens throughout the transition from the sleep mode to the active mode. This paper designs low power 8:1 Multiplexer using various CMOS designs like pass semiconductor device, transmission gate and Power Gating Technique. The Multiplexer has been realized with stacking power gating leakage reduction technique in 45 nanometer technology [10] [11].

2. 8:1 MULTIPLEXER
An 8:1 Multiplexer sends one of 2^n input lines to a single output line. A Multiplexer has eight sets of input X (0), X (1), X (2), X (3), X (4), X (5), X (6), X (7) and three select lines S (0), S (1) and S (2). The Multiplexer output in a single bit Y, which is one of the 2^n input data.

$$\boldsymbol{Y = X(0).\overline{S(0)}.\overline{S(1)}.\overline{S(2)} + X(1).S(0).\overline{S(1)}.\overline{S(2)} + X(2).\overline{S(0)}.S(1).\overline{S(2)} + X(3).S(0).S(1).\overline{S(2)} + X(4).\overline{S(0)}.\overline{S(1)}.S(2) + X(5).S(0).\overline{S(1)}.S(2) + X(6).\overline{S(2)}.S(1).S(0) + X(7).S(0).S(1).S(2)} \quad (1)$$

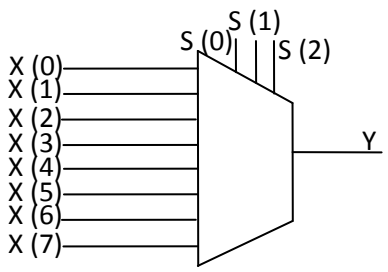
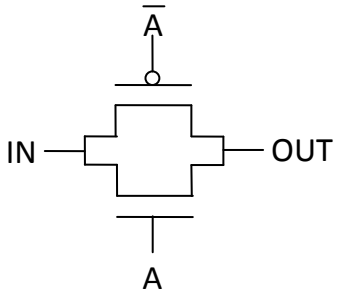


Fig 1: Conventional 8:1 MUX

2.1Transmission Gate Logic (TGL) Based 8:1 Multiplexer

The CMOS Transmission Gate uses Transmission Gate Logic to appreciate advanced logic functions employing a little range of complementary transistors. It solves the matter of low logic level using PMOS as well as NMOS [11].

Transmission gate has a switch with low resistance and capacitance having ratio less logic. Also, DC characteristic of this gate is independent of input levels. It is designed by connecting each source to source and drain to drain terminal of NMOS and PMOS transistors. Because the NMOS transistor is passing strong signal '0' and PMOS transistors passes strong signal '1' towards the output,



A

A	IN	OUT
H	H	H
H	L	L
L	X(don`t care)	Z(high impedance)

B

Fig 2: (A) Transmission Gate (B) Truth Table

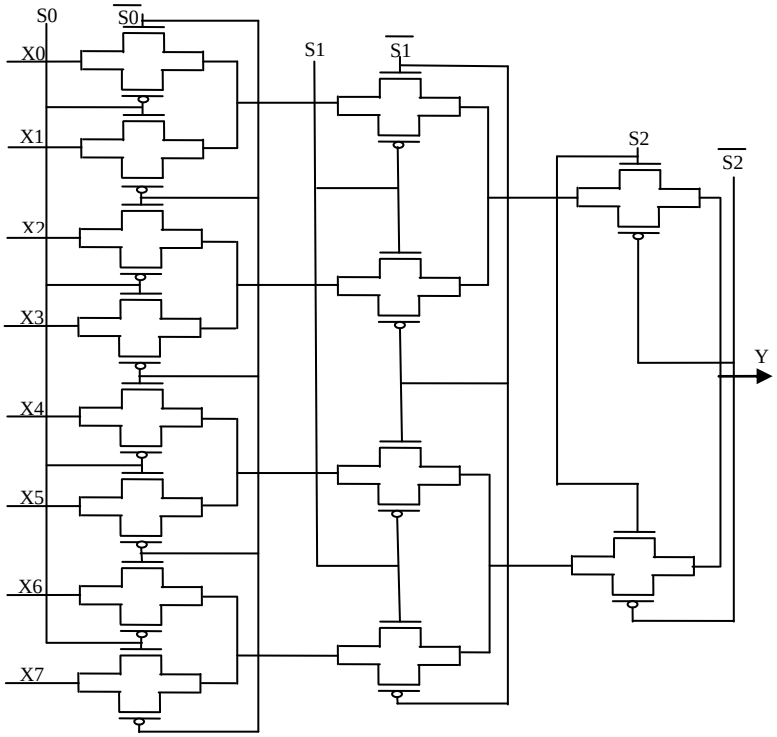


Fig 3: TGL base 8:1 MUX

each transistor is flipped on-off by the enable signals. The voltage on A node is a Logic one, the complementary Logic zero is applied to active-low A node. It permits each transistor to conduct and pass the signal from IN to OUT. Once the voltage on active-low node A is a Logic zero, the complementary Logic one is applied to node A turning each transistor OFF and forcing a high impedance condition on each IN and OUT node. The schematic diagram (Fig. 2) includes the absolute labels for IN and OUT, because the circuit will operate in a homogenous manner if that label were reversed. This design are provides true bidirectional property while not degrading input signal. The transmission gate symbol and the truth table are depicted in Fig. 2. [12] [13] [14].

2.2 8:1 Multiplexer with Power Gating Technique

The Power Gating Technique reduces the leakage in every circuit, by inserting the NMOS and PMOS to the circuitry [15]. Fig. 4 shows the Power Gating circuit. Power Gating Technique is the most popular one for reducing the leakage in the circuits. Because of the simplicity of implementation of the technique, Power Gating has been used to minimize leakage energy in circuits at the architectural level [16] [17]. The effectiveness of Power Gating requires the following;

- The switches for turning OFF and ON of the functional unit at circuit level.
- These switches controls the power gate at various parts of the circuit which act as handles at the system level thereby giving the system software or the compiler the ability to control them.

A sleep control mechanism is used for efficient power management. In the active mode, sleep is set to 'low' and sleep controlled transistor is turned ON. Since their resistance is small, the supply voltage VDD and VSS (GND) functions as real power line. In standby mode, sleep is set to 'high' and transistors are turned OFF, and leakage current is 'low'. In fact only one type of transistor is enough for the leakage control. Power Gating is a technique that can be easily implemented on 8:1 MUX circuits. Power Gating can reduce the leakage power, leakage current and delay. For PMOS and NMOS insertion, applied voltage on gate is 0v in active mode and virtual VDD line is connected to the supply VDD [18].

3. SIMULATION RESULT

In this section the result of Transmission Gate Logic (TGL) and Power Gating TGL type Multiplexer has been calculated. Fig.5 shows the Transient Response of 8:1 Multiplexer.

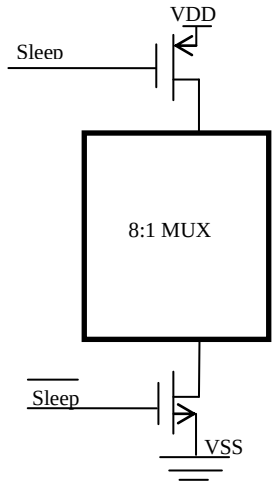


Fig 4: Power Gating 8:1 MUX

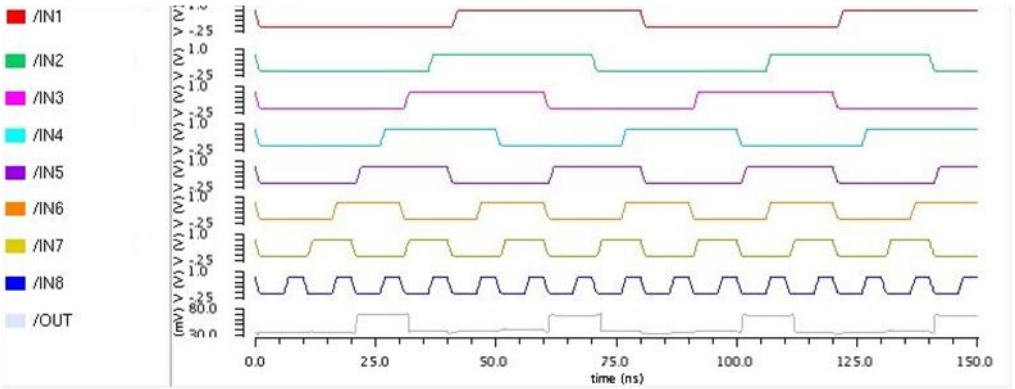


Fig 5: Input and Output of 8:1 MUX

3.1 Leakage Power

The leakage power of the circuit is measured during the standby mode. It explains how large percentage of power is wasted by the whole circuit during OFF state when there is no supply. The leakage power is product of leakage current and supply voltage [19]. The basic equation of leakage power is displayed in Eq. (2).

$$\mathbf{Pleak = I\ leak \times VDD} \quad \mathbf{(2)}$$

Where leak = leakage current, VDD = supply voltage.

3.2 Leakage Current

Leakage current of the MUX is estimated during the standby mode. To estimate the leakage current of the MUX, NMOS transistor is required to measure the leakage current that is connected at the pull down network below the whole circuit. The Sleep transistor is OFF for this technique whenever leakage current calculation is analyzed. Leakage current is derived and calculated through the equation given below [20].

$$\mathbf{I_{leak} = I_{sub-thr} + I_{gat-ox}} \quad \mathbf{(3)}$$

Where I sub-thr = sub-threshold leakage current, Igat-ox = gate-oxide leakage current

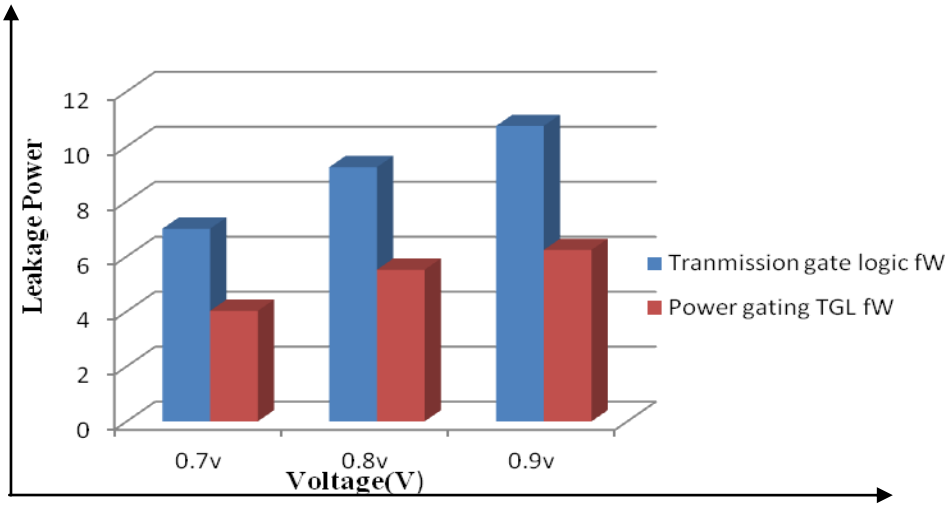


Fig 6: Leakage Power Comparison at Various Voltage Supplies

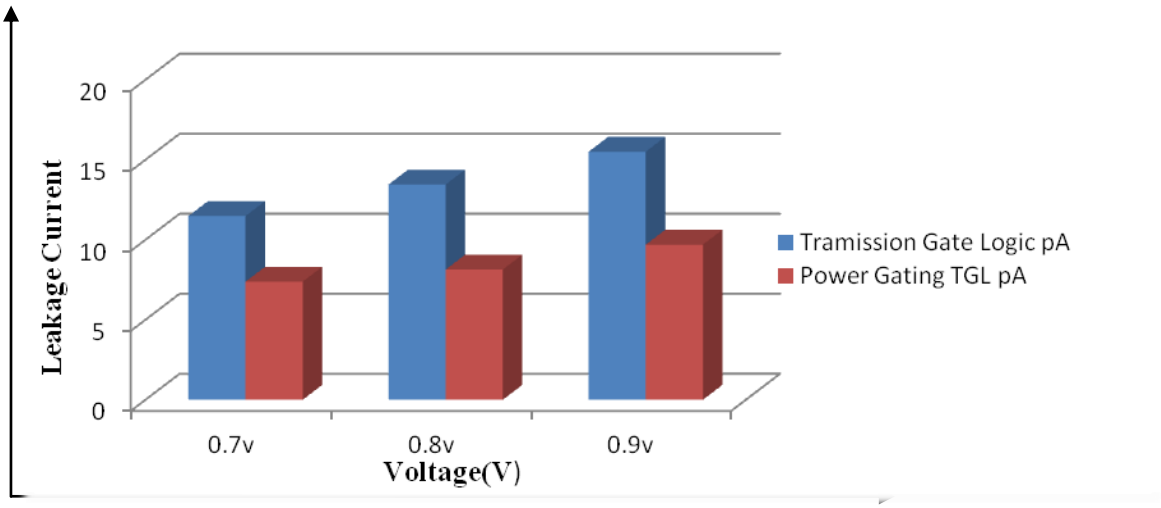


Fig 7: Leakage Current Comparison at Various Voltage supplies

$$\mathbf{I_{sub-threshold} = K_A W e^{\frac{-Vth}{nV\theta}}(1 - e^{\frac{-V}{V\theta}})} \quad \mathbf{(4)}$$

Where K_A and n are experimentally derived, W = gate width, Vth = threshold voltage, n = slope shape factor, VΘ = thermal voltage

$$\mathbf{I_{gat-ox} = K_B W(\frac{V}{Tox})^2 e^{\frac{\alpha Tox}{V}}} \quad \mathbf{(5)}$$

Where KB and α are experimentally derived, Tox = oxide thickness

The design of logic signal delay is found to be necessary in every circuit. For this design, we need to find out the values of resistor that can introduce the delay on the signal lines. Delay of the circuit has depended on the value of the resistor itself as well as the capacitive load of the circuit [21]. The propagation delay of the RC circuit can be calculated by the Elmore model delay formula as follows:-

$$\mathbf{tp = 0.69Req \times CL} \quad \mathbf{(6)}$$

4. COMPRESSION RESULTS

This section compares the result of Multiplexer Design.

Supply Voltage	Transmission Gate Logic (TGL)			Power Gating TGL		
	Delay (nS)	Leakage Current (pA)	Leakage Power (fW)	Delay (nS)	Leakage Current (pA)	Leakage Power (fW)
0.7	19.253	11.48	7.01	15.398	7.381	4.021
0.8	19.896	13.45	9.25	15.441	8.137	5.518
0.9	20.372	15.50	10.75	16.289	9.692	6.239

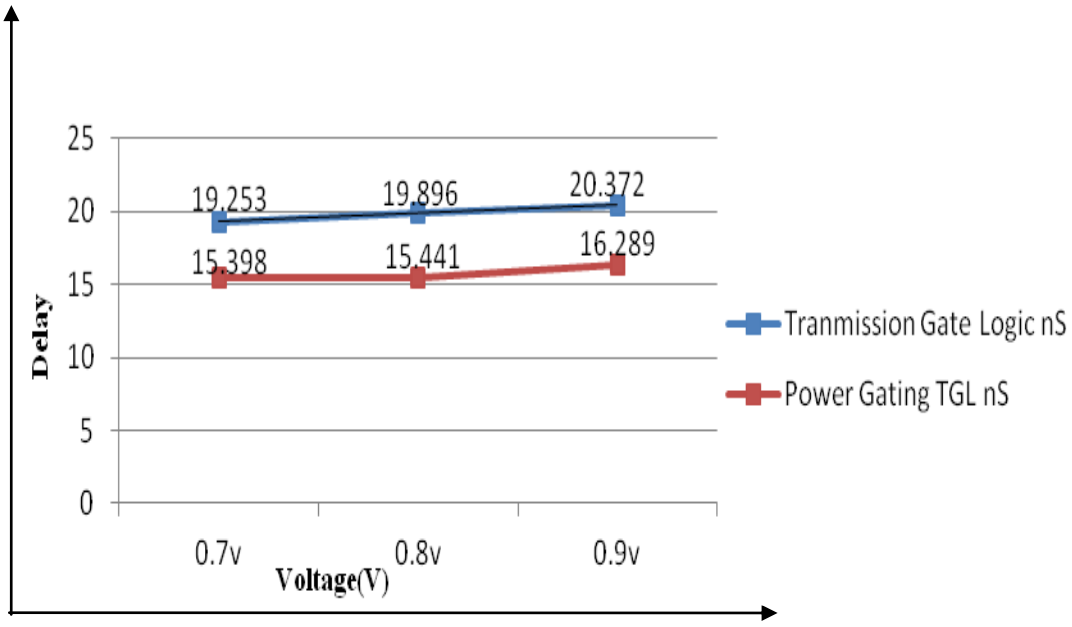


Fig 8: Delay Comparison at Various Voltage Supplies

5. CONCLUSION

This paper designs an 8:1 Multiplexer with Transmission Gate Logic using Power Gating Technique for reduction of leakage power and leakage current. The Transmission Gate Logic (TGL) using 28 transistors in the circuit is given in fig. 3. Reduction of power and current of Power Gating Technique is less as compared to Transmission Gate Logic (TGL). The result calculates in active mode with voltage variation. The 8:1 Multiplexer was designed using 45nm technology on cadence virtuoso tool. Using this tool the results have been calculated. Leakage power of 8:1 MUX Transmission Gate Logic (TGL) is 7.01fW and Power Gating Technique is 4.021fW. The leakage current of Transmission Gate Logic (TGL) is 11.48pA and Power Gating Technique is 7.381pA only.

6. ACKNOWLEDGMENTS

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