

Performance Analysis of High Speed Domino CMOS Logic Circuits

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ABSTRACT

As the demand of low power high performance arithmetic circuits multiplies, during this paper, we aim to introduce a style of latest MT-CMOS domino logic and FTL dynamic logic technique to style adder circuit. The MT-MOS transistors cut back the facility dissipation by minimizing sub threshold run current in the introduced domino logic circuits. The MT-NMOS semiconductor connected in discharging path of output electrical converter may be applied for pipeline structure to scale back the facility consumptions and increase fan-out. Dynamic logic vogue CMOS circuit is employed to enhance the speed and cut back the world of style by decreasing the device count. The introduced FTL dynamic logic circuit improves the performance by evaluating the computational blocks partially before its input signals are formalized and then rapidly perform a final evaluation as soon as the inputs arrive. This dynamic logic formation is like minded for an arithmetic circuit wherever the important path s created of an outsized cascade of inverting gates is created.

The mixture of MT-CMOS and dynamic logic circuit provides high fan-out, high change frequencies with each lower delay and dynamic power consumption. The simulation results of those projected low power high performance circuits provide 75% power reduction, three times redoubled high speed operation and active space reduction, whereas revealing lower sensitivity to power provide, temperature, electrical phenomenon load and method variations than the dynamic domino CMOS technologies.

Keywords

CMOS, Domino Logic, FTL (Feed through Logic), MT-CMOS, RCA

1. INTRODUCTION

In IC's, Dynamic logic (Clocked logic) was a style methodology digital logic in logic family that was standard in 1970s.

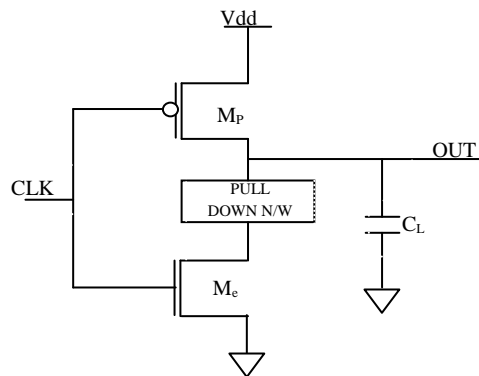


Fig.1: Dynamic CMOS Logic

It may be distinguished from static logic as it uses a clock signal in its implementation of combinative logic circuits. The utilization of clock signal in Dynamic logic is to gauge the combinative logic. The clock signal is additionally employed in consecutive circuits wherever it is used to synchronize the transitions in consecutive logic circuits [1].

Power utilization is a standout amongst the most significant imperatives in the planning of any dynamic logic circuit. Domino CMOS logic circuit family discovers a wide assortment of provisions in microchips, advanced indicator processors, and element memory because of their rapid and low gadget check. As it may be, there are unavoidable issues

that corrupt the clamor invulnerability of this family; the certain spillage current and the charge offering.

Added to the impediments, is the generally extensive force utilization, particularly if contrasted with the static corresponding CMOS logic crew [3]. To intensify the matter, these impairments are more material with the scaling of CMOS innovation starting with one era onto the next. In this section, the effect of CMOS innovation scaling on the execution of domino CMOS logic has been analyses. It is a CMOS-based development of element logic methods which were focused either around PMOS or NMOS transistors. To accelerate the circuits, this logic was produced.

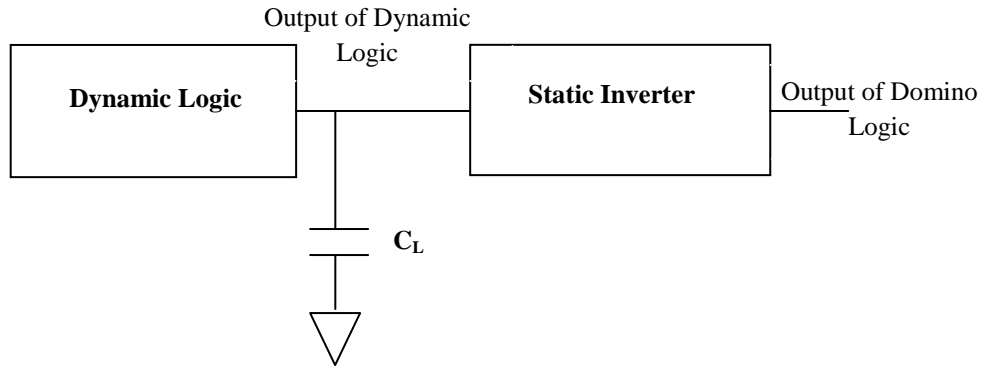


Fig.2: Block Diagram of Domino Logic

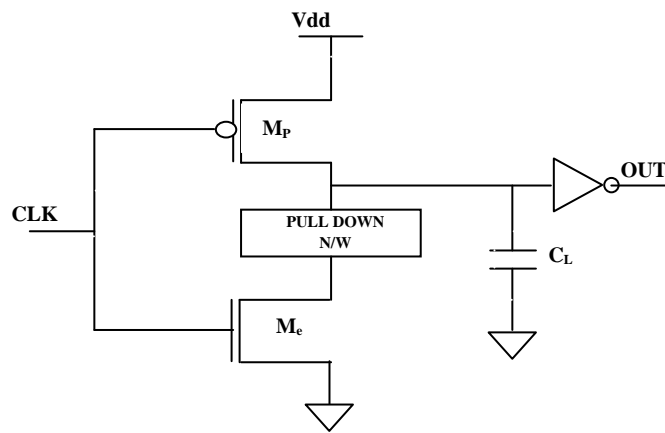


Fig.3: Basic Structure of Domino Logic Circuit

The demand of high performance CMOS VLSI processors with higher complication forces us to enhance the performance, area, efficiency and practicality of arithmetic logic circuits. Several efforts are targeted on the development of adder styles [4]. Since the utilization of carry look-ahead principle for high-speed arithmetic units, one in all, the challenges in VLSI processor style these days is structured for constructing CLA circuits, exactly for the 8-bit circuits while not limiting the purposeful flexibility. A coffee power high performance FTL circuit technique is projected in [5] for reducing power dissipation and decreasing propagation delay in domino logic. The low power FTL dynamic logic is achieved with the help of feed through dynamic CMOS logic structure [6]. Wang, Tsai [7] used the 8-bit CLA victimization- the dual-Vt domino logic blocks that are organized in a very PLA- like manner and synchronously triggered. It is enforced on chemical element to verify the facility reduction also because of the preservation of high speeds [8]. Proposed an 8-bit pipelined CLA victimization- the dual- Green Mountain State domino logic blocks to scale back the facility dissipation. Dual-Vt Domino Logic Circuits foreseen for reducing sub-threshold discharge current in domino logic circuits is projected in [9]. Sleep switch twin threshold voltage domino logic with reduced sub-threshold logic gate compound discharge current is projected and tried in [10]. The high speed arithmetic circuit obtained victimization FTL logic in [11]. Normally, domino CMOS logic is widely employed in high performance integrated circuits. It reduces the device count and chemical element space, and improves performance in comparison to the quality totally complementary static CMOS logic [12].

However, the chief disadvantage with the domino dynamic logic circuit is its excessive power dissipation owing to the change activity and the clock load. To upset the excessive power dissipation of the dynamic logic, the present style methodologies trade power for performance within the delay in the important sections of the circuit [13]. This can be achieved through a combination of dynamic and static circuit designs, use of twin provide voltages and dual-Vt transistors. Domino and dynamic logics are chiefly tormented by charge sharing and race issues [14]. To resolve these demerits, we tend to propose the new MT-CMOS dynamic logic circuit victimization multi-threshold MOS semiconductor device for reducing the facility dissipation and FTL logic for increasing the operative speed of arithmetic circuits [15]. The projected circuit is giving response to these issues and minimizing power wastages. During this paper, we tend to propose a coffee power high performance Ripple Carry Adder (RCA) logic structure employing a new MT-CMOS domino logic blocks [16].

2. PRINCIPLES OF OPERATION

The planned MT-CMOS Domino Logic Circuit as demonstrated fig.4 is employed for reducing sub-threshold outpouring current and power in domino logic circuits [17]. In MT-CMOS logic circuit, PMOS and NMOS transistors should be larger than the logic cells. This condition greatly depends on the parasitic capacitors gift within the semiconductor. Once the PMOS and NMOS semiconductor dimension is reduced, the parasitic capacitances become larger which tends to suppress the change of logic low and high to enhance the speed.

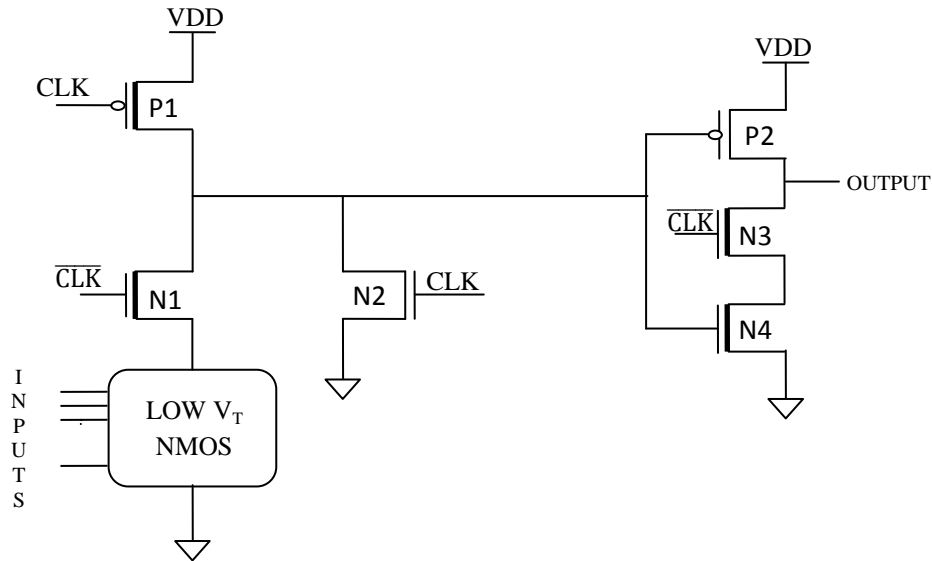


Fig.4: Proposed MT-CMOS Domino Logic

Within the standby (Sleep mode), i.e., at the high clock signal applied to the circuit, the MT-transistors are OFF, that lead the circuit for reduction of static power dissipation and elimination of sub-threshold current [18]. Within the analysis mode, the dynamic logic circuit improves the speed and reduces the overall space of MT-CMOS circuit.

When the CLK is high, the transistors P1, N1 are OFF. As a result of the multi threshold voltage of the transistors, the sub threshold leakages are restricted which supports to extend the speed. In the same time, low state electronic transistor N2 is ON to ground the outflow and junction currents gift in node A at sleep mode which cause to keep the output in logic high in node B. The output electrical converter is employed to revive the polarity and holding the output of logic circuit in sleep mode [19]. The clock controlled MT-NMOS electronic transistor N3 is utilized to keep the output as high throughout this sleep mode for the analysis method of second stage within the pipelined structure. This method is termed as pre-charging part. When the CLK is low, the transistors P1 and N1 are ON. This can be referred to as analysis part. Throughout this analysis part, the low state NMOS logic block is evaluated with efficiency to modify the node voltage V_A , nearly adequate to V_{dd} or ground. The low V_T logic circuit has reduced logic delay by 70% compared to high- V_T logic circuit. Hence it is quickly evaluated to provide the output. The projected logic circuit provides the pliability to style the logic circuit; therefore it will be used to style period domino logic with unvaried circuits [20].

The two stage MT-CMOS dynamic logic circuit as presented in fig.5 has the cascaded association of projected technique to construct pipeline structure. Here, each stage's are operates as an alternative in pre-charging part and analysis part, variedly. If the applied CLK is high, initial stage operates in pre-charging part and second stage operates in analysis part. The CLK signal applied MT-NMOS N3 is employed to hold the output of first stage in logic high during the pre-charging phase to judge the second stage. The second stage evaluates the low state NMOS logic block by the activation of the MT-Transistors P3 and N5. If the applied CLK is low, initial stage operates in analysis part and second stage operates in pre-charging part. The initial stage evaluates the low state NMOS logic block by the activation of the MT-Transistors P1 and N1. At an identical time, the second stage operates in pre-charging phase. The CLK signal applied to MT-NMOS N7 is used to hold the output of second stage in logic high during the pre-charging phase to evaluate the next stage. This alternate change of pre-charging and analysis of adjacent stages additionally aids to cut back the ability consumption of the circuit. Additionally, this dynamic domino logic operates swiftly to develop the output as compared to typical CMOS dynamic logic circuit.

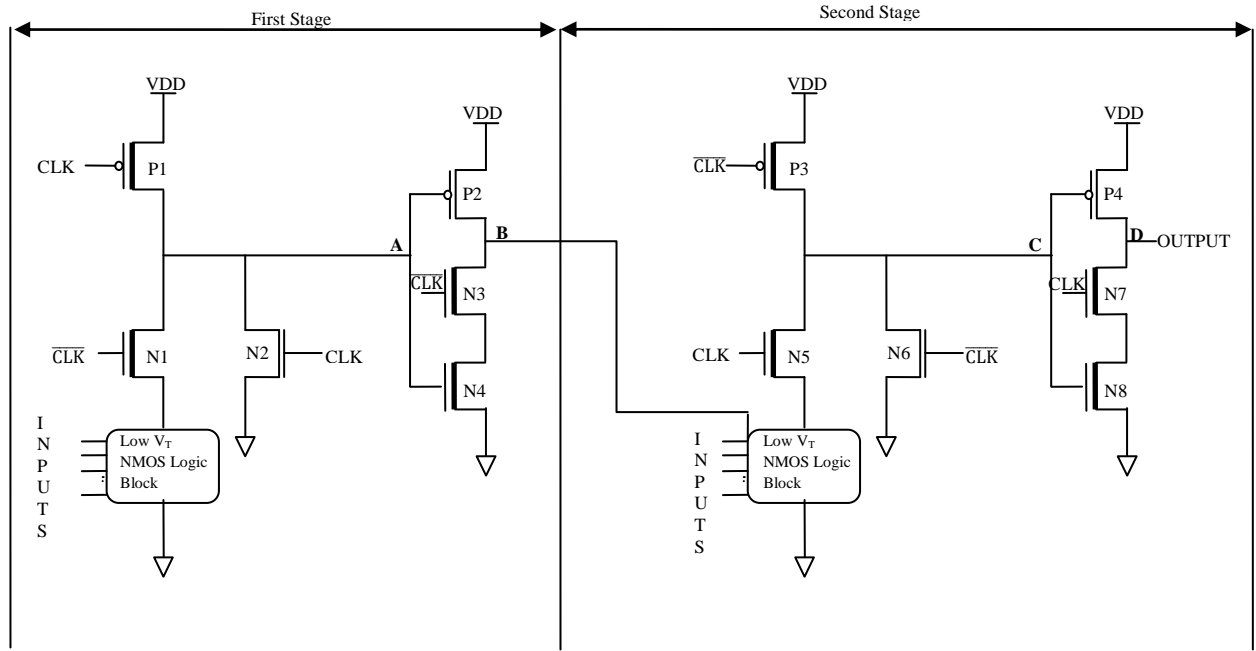


Fig.5: Cascaded Two stage MT-CMOS Dynamic Logic

3. RIPPLE CARRY ADDER

Here we present the design of RCAs based on the planned MT-CMOS dynamic logic as depicted in Fig.5. The structure of basic sum and carry cells used in the design of long word-length adder circuits are similar to the CMOS adder cell in [6]. Within the combined ripple carry adder conferred in Fig.6, the total ripple carry delay is reduced by optimizing the

Low VT NMOS ripple carry logic block. At the time of t , the sum is calculated using the previous carry output and present input values. Within the pipelined structure the carry output is propagated through the node to gauge the sum logic block.

The mathematical formation of sum and carry output is expressed as follows; at the time $t+1$ the sum uses carry to calculate

$$\text{CARRY} = AB + C_i(A + B) \quad (1)$$

$$\text{SUM} = \overline{\text{carry}} (A + B + C_i) + ABC_i \quad (2)$$

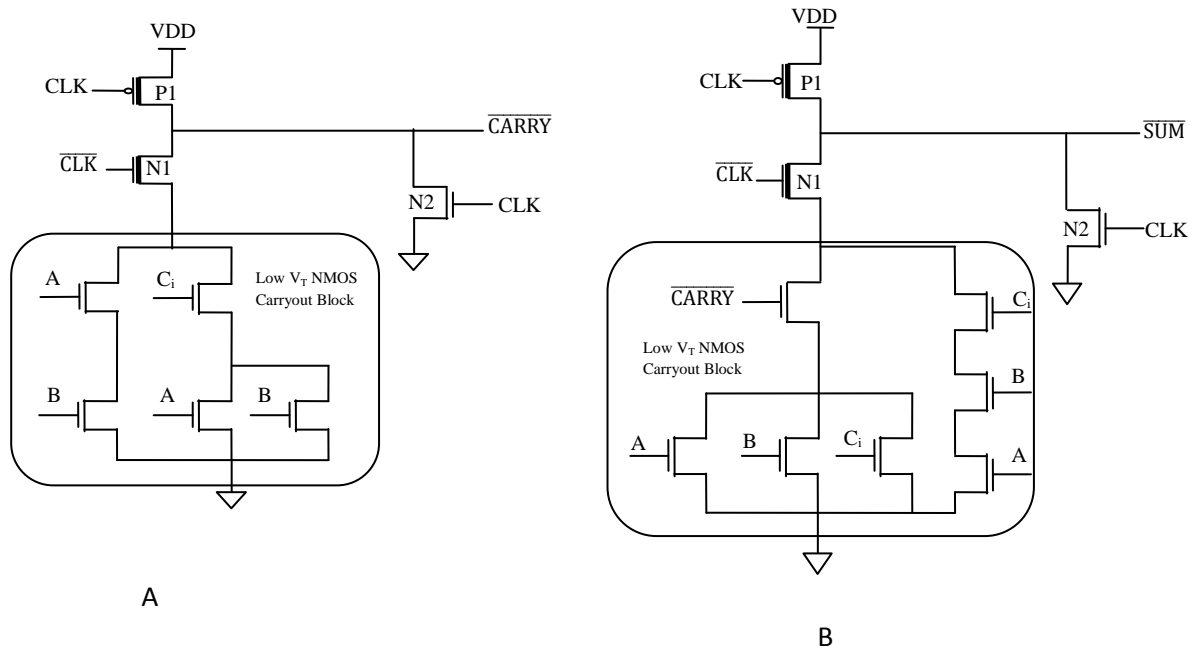


Fig.6: MT-CMOS Dynamic Logic for Ripple Carry Adder (A) Carry Block (B) Sum Block

4. SIMULATION AND RESULTS

4.1 Transition Response: Domino logic circuit is simulated at operating voltage 0.7 volts (45nm technology). Display in below fig. 7.

4.2 Power and Delay: The projected high performance and low power MT-CMOS, primarily, based on ripple carry adder technique increase the speed and reduce the common power consumption of the circuit. To verify this assertion, the simulations were conducted for the projected MT-CMOS dynamic logic and typical CMOS dynamic logic circuits [21-22]. A 45nm CMOS technology was used in Cadence virtuoso tool to work out the ability dissipation and operational delay of circuits. The ability and delay values also are verified exploring the following formulas. Transient power consumption can be calculated exploiting the equation:

C_{pd} = dynamic power-dissipation capacitance

Average propagation delay

$$t_{pd} = \frac{(t_{pdr} + t_{pdf})}{2} \quad (4)$$

Where t_{pdr} = rising propagation delay, from input to rising output crossing $V_{dd}/2$ and

t_{pdf} = falling propagation delay, from input to falling output crossing $V_{dd}/2$.

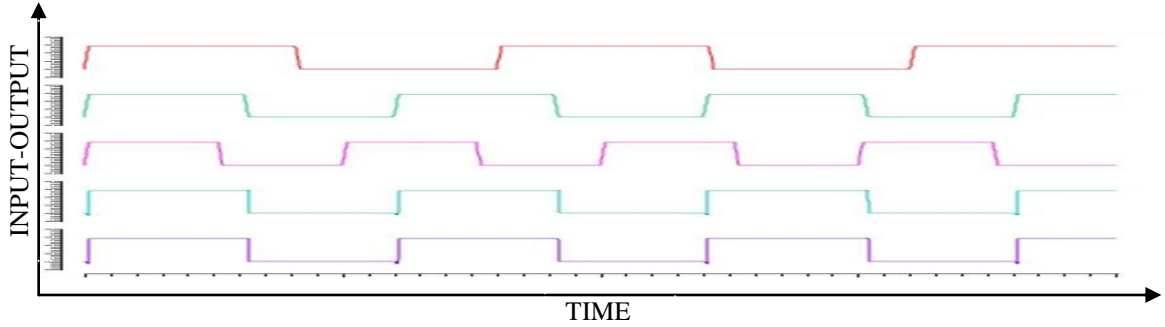


Fig. 7: Transition Response of Proposed MT-CMOS dynamic logic for Ripple carry adder

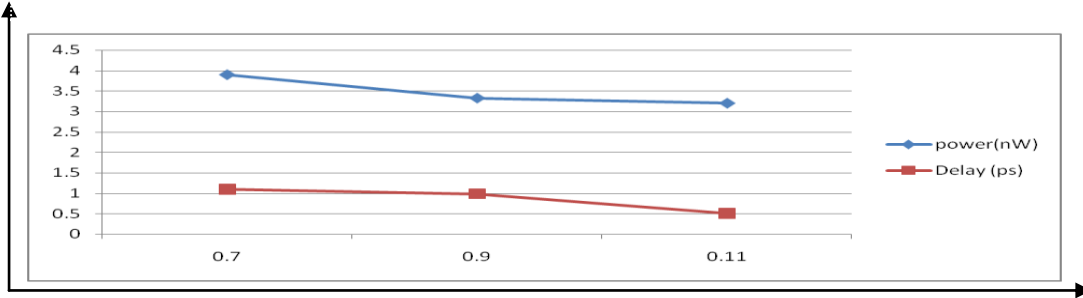


Fig.8: Voltage Variation Chart - Power and Delay

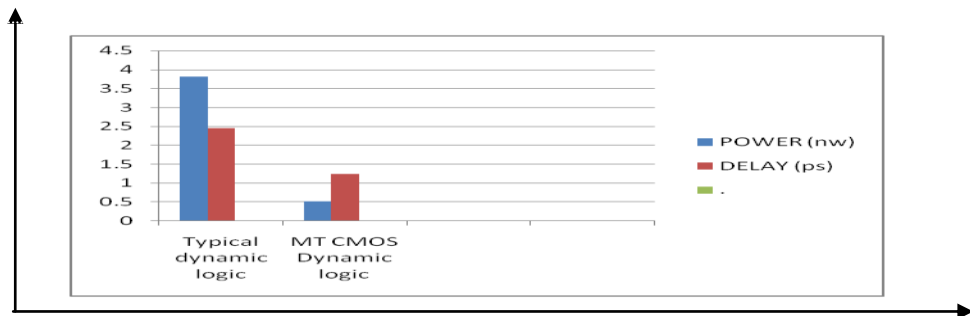


Fig. 9: Comparison Chart between MT CMOS Dynamic Logic and Typical Dynamic Logic

$$\text{Power}(P_t) = C_{pd} * V_{dd}^2 * F_i * N_{sw} \quad (3)$$

Where P_t = Transient power consumption;

V_{dd} = Supply voltage;

F_i = input signal frequency;

N_{sw} = number of bits switching;

5. CONCLUSION

In this paper, we have given an efficient method to reduce power and increase the speed of dynamic logic circuit to use in Adders exploitation FTL and MT-CMOS logic technique. Charge sharing problems related to dynamic and domino families also are removed within the projected structures. By avoiding these power wastages and MT-CMOS domino logic

technique reduces the entire power consumption of adder circuits. Experiments have shown that top speed and low power obtained by the projected model match with Cadence virtuoso tool simulation results all right. By the experimental verification, the projected RCA method reduced power more than (55%) and propagation time delay (around 20%). Simulated results show significant improvement in leak tolerance and acceptable speed for high speed applications. Therefore, the power consumption and space were shriveled simultaneously in our projected circuit.

6. ACKNOWLEDGMENTS

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