International Journal of Computer Applications (0975 8887)
Volume 99 - No. 19, August 2014

Realization of Combinational Multiplier using Quantum Cellular Automata

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ABSTRACT

Quantum dot cellular automata(QCA) shows promise as a post silicon CMOS,low power computational technology.Nevertheless,to generalize QCA for next generation digital devices,the ability to implement conventional programmable circuits based on NOR,AND and OR gates is necessary.We devise a new QCA structure,the QCA multiplier,employing the five quantum dot QCA cell.The structure can multiply two 4 bit binary number.Tihis work is motivated by the fact that implementing combinational multiplier using QCA will reduce its area and consequently its heat dissipation.The efficacy of our framework is that it uses QCA majority gates as its primitives.

Keywords:

QCA, CMOS, multiplier

1. INTRODUCTION

Complementary metal-oxide semiconductor technology(CMOS) has consistently provided the required scaling in VLSI circuits. However, such an aggressive approach has many problems. Some of these problems are high leakage current, high power density levels and high lithography costs. It is predicted that these problems will grow in magnitude exponentially as we move towards compaction of circuits within a small area. So a viable alternative has to be determined. One of the possible replacement can be QCA[2, 4, 6, 12, 16]. In QCA, logic states, rather than being encoded as voltage levels, are represented by the configuration of electron pair confined within a quantum-dot cell.QCA promises small size and low power consumption[1, 5, 8, 9, 10, 11, 13, 14, 15, 17, 18, 19, 20].
A combinational multiplier is a good example of how simple logic functions (gates,half adders and full adders) can be combined to construct a much more complex function.It is possible to construct a 4X4 binary combinational multiplier from an array of and gates,half adders and full adders.Consider the following binary multiplication of two positive 4 bit integer values.

$$\begin{array}{lrl} Multiplicand & 1101 & (13) \\ Multiplier & \times\ 1011 & (11) \\ & \ldots\ldots\ldots\ldots\ldots & \\ & 1101 & \\ & 1101 & \\ & 0000 & \\ & 1101 & \\ & \ldots\ldots\ldots\ldots\ldots & \\ & 10001111 & (143) \end{array}$$

In the course of multiplying two binary numbers,each bit in the multiplier is multiplied with the multiplicand.Each of the four products is aligned by shifting left.The four resulting products are added to form the final product.Since we are dealing with binary numbers, forming the products is particularly easy.If the multiplier bit is 1,then the corresponding product is simply the shifted copy of the multiplicand.If the multiplier bit is 0,then the product is zero.1-bit binary multiplication is thus just an AND operation.The above method can be generalized for N bits.For N-bit multiplication(an NXN product),the result is 2N bits wide.Hence,4X4 bit multiplication is an 8-bit result.
This paper demonstrate the use of QCA devices to implement binary multiplier.A QCA multiplier could be an important element of future quantum computing systems.

2. PRELIMINARIES

The quantum dot cellular automata use a binary representation of information, by replacing the current switch with a cell having a bistable charge configuration. One configuration of charge represents a binary "1", the other a "0", but no current flows into or out of the cell. The field from the charge configuration of one cell alters the charge configuration of the next cell.

2.1 QCA Cells

A QCA cell[3],shown in fig1 contains four quantum-dots at four corners of a square and two mobile electrons.These electrons can move to any of the quantum dots by electron tunneling.Due to Coulombic interaction,these electrons usually tend to reside at the diagonal corners of the square,giving rise to two configurations that are stable.Assigning polarization +1 and -1 to these configurations lead to the two binary logic state 1 and 0.

2.2 QCA Wires

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells .During each

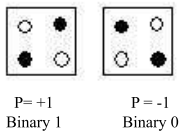

Fig. 1. Basic QCA cell and Two Possible Polarizations

clock cycle, half of the wire is active for signal propagation, while the other half is unpolarized. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly activated cells to be polarized. Thus, signals propagate from one clock zone to the next.

QCAwire-eps-converted-to.pdf

Fig. 2. QCA wire

2.3 QCA gates

Majority voter gate and inverter acts as the basic gates in QCA. The governing equation of majority voter gate is

$$M(A, B, C) = AB + BC + AC \tag{1}$$

Two input AND and OR gate can be implemented from three input majority voter gate by making one input constant.

$$M(A, B, 1) = A + B$$
$$M(A, B, 0) = AB \tag{2}$$

Fig 3 and Fig 4 shows the gate symbols and their layout.

3. COMBINATIONAL MULTIPLIER

In this approach, the multiplier is constructed from an array of building blocks as shown in the figure 5.Each building block consists of an AND gate for computing the corresponding partial product($x_i \times y_j$).Another component of the building block is a full adder in which,the output of the AND gate,the carry(C_in) from the previous block and the sum of the previous block acts as input.It generates a carry out bit(C_out) and a new sum out bit(Sum_out).The circuit diagram of the multiplier block is shown in figure 6.

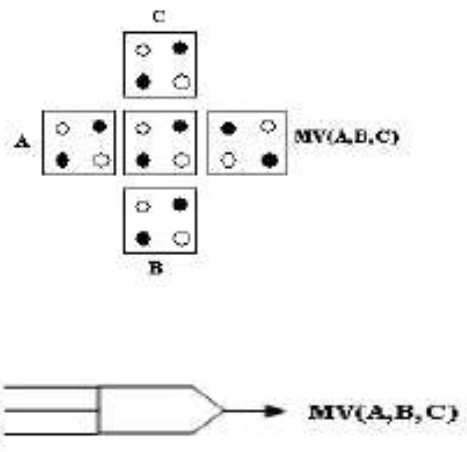

Fig. 3. QCA Majority Voter Gate

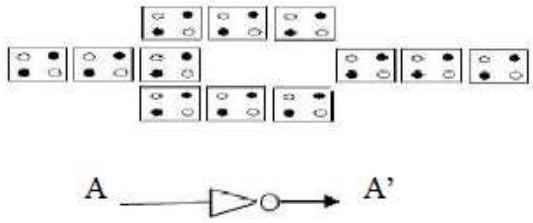

Fig. 4. QCA Inverter Gate

When this building block is implemented in QCA,two majority gate and an inverter is used to realize the full adder and the AND gate can be implemented using another three input majority gate Majority gate 3 by making one of the input equal to 0.Majority gate 1 is a five input majority gate,whose three inputs are (Sum_in),(C_in) and the output of the AND gate ($x_i \times y_j$)and the other two inputs are shorted to the output of the inverter.The output of majority gate 1 is the sum (Sum_out).Majority gate 2 is a three input majority gate.The previous inputs act as the inputs to majority gate 2 and the output is the carry (C_out).The output of majority gate 2 is also fed into an inverter whose output goes into majority gate 1 .The layout of the multiplier is shown in figure 7.
Figure 8 illustrates the interconnection of these building blocks to construct a 4X4 combinational multiplier.

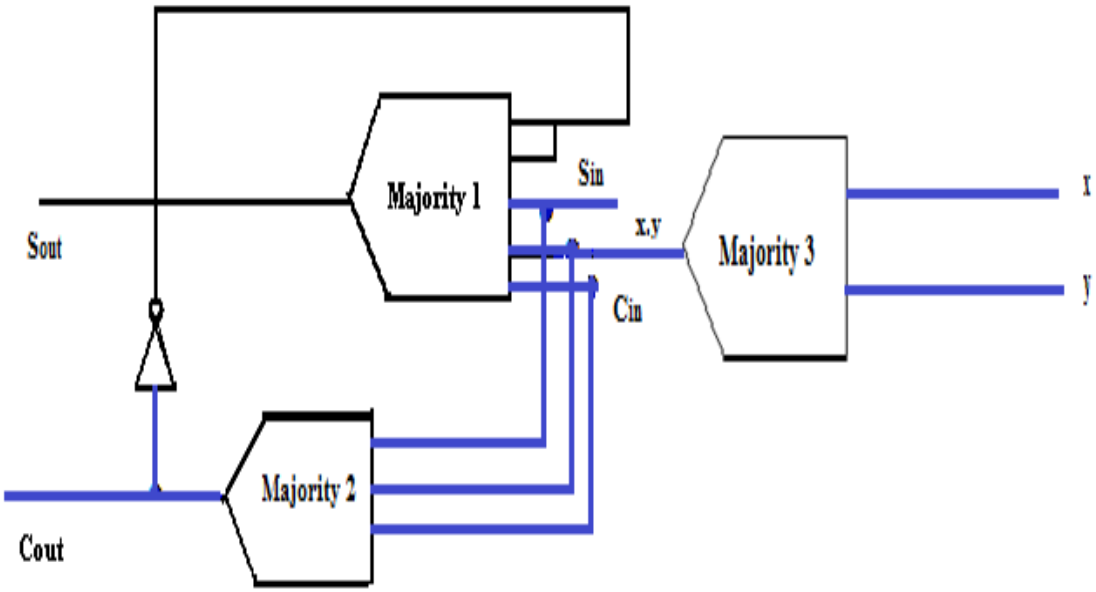

Fig. 6. Circuit diagram of multiplier block

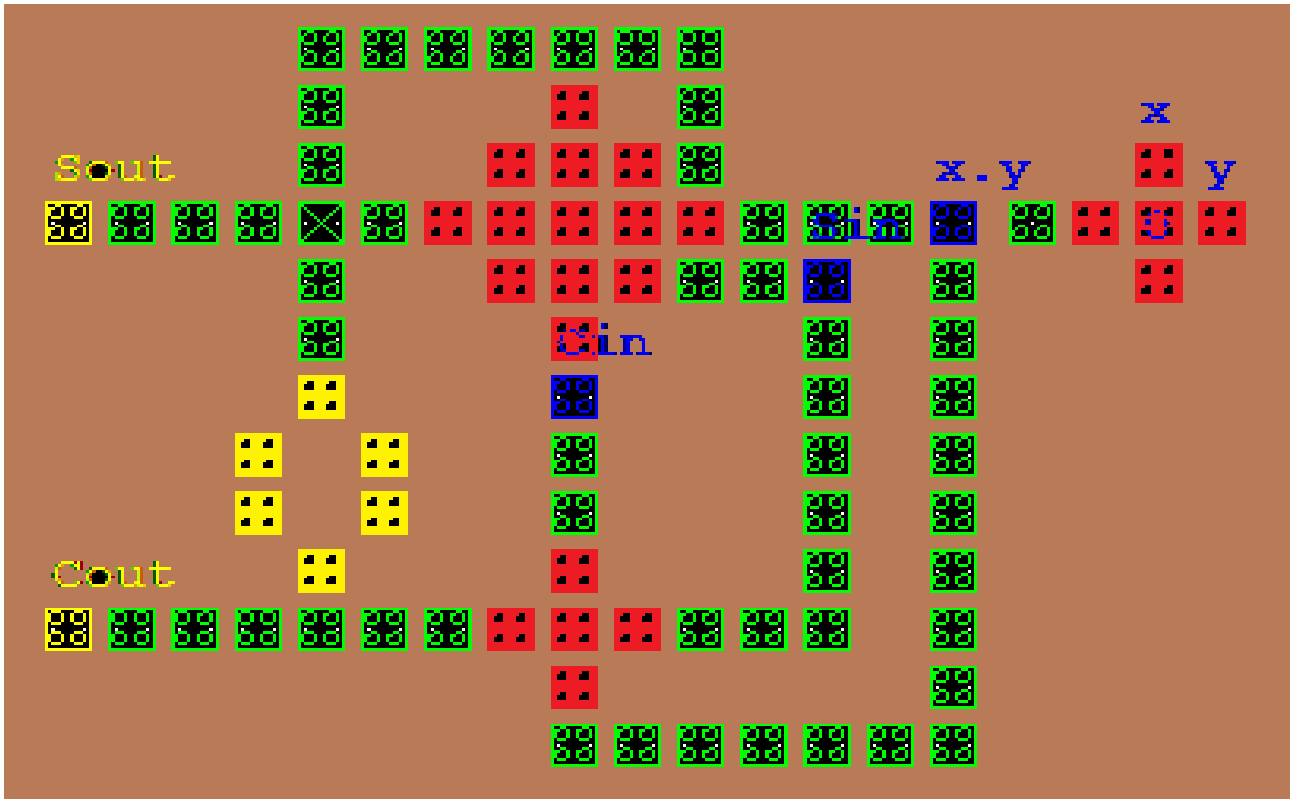

Fig. 7. Multiplier Block Layout

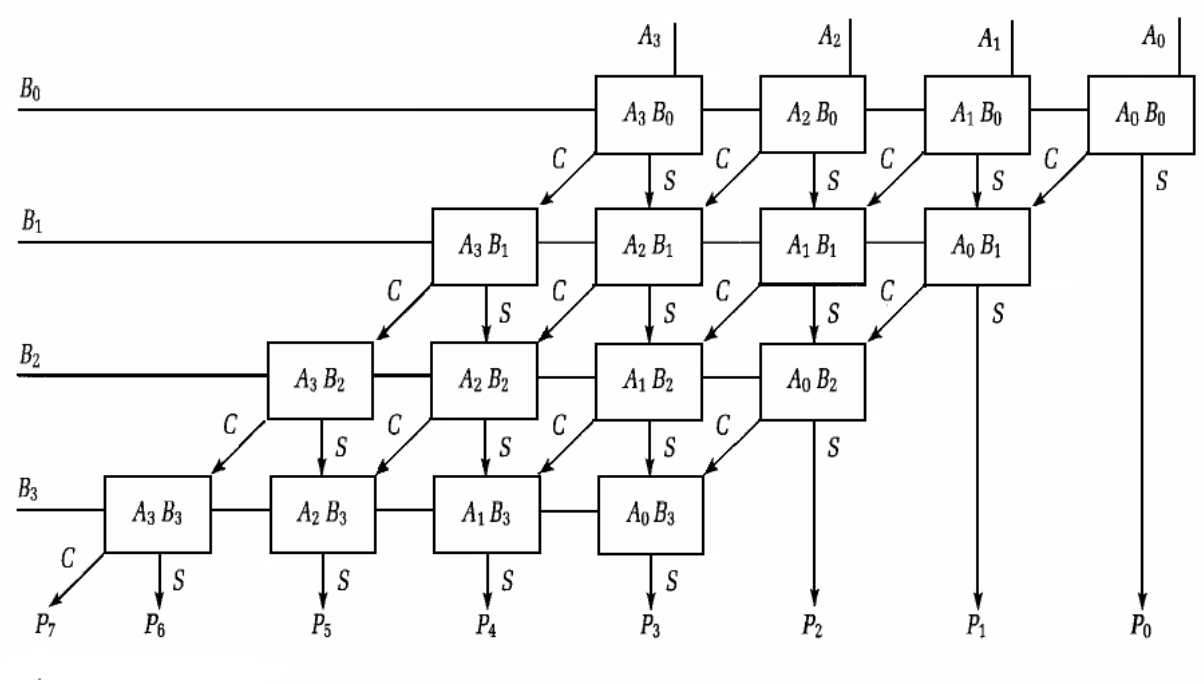

Fig. 8. 4X4 Multiplier Structure

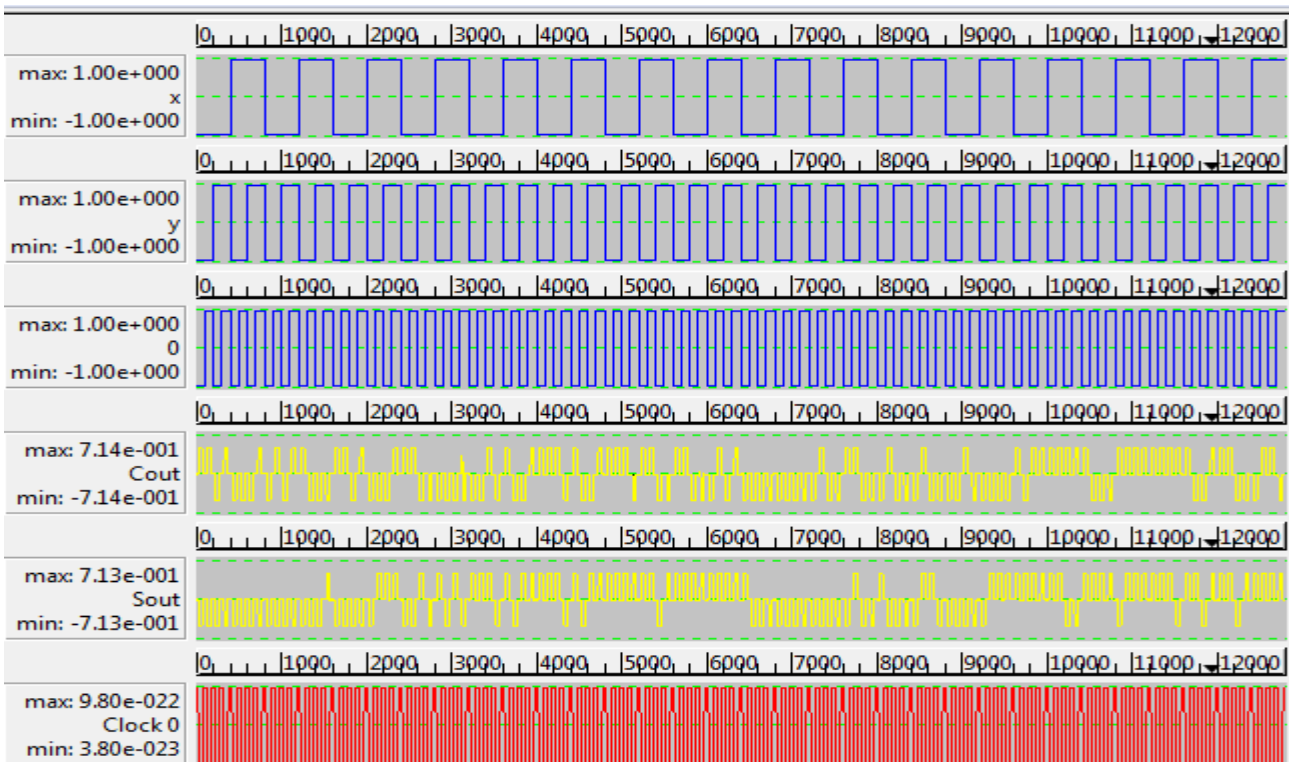

Fig. 9. 4X4 Multiplier Block Simulation Result

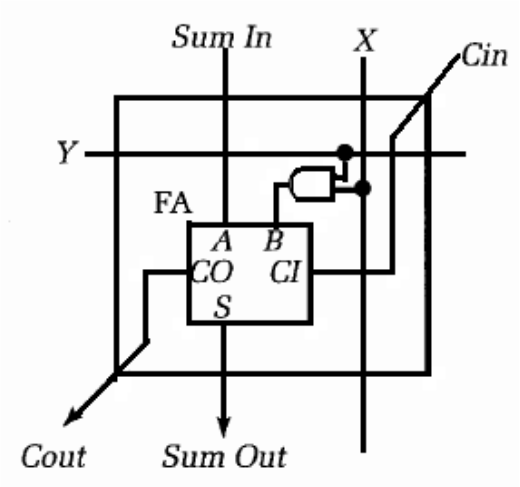

Fig. 5. Multiplier Block

4. RESULT ANALYSIS

The multiplier building block is implemented in QCAdesigner. The simulation result is shown in figure 9. The area of the block is $0.10\mu m^2$ which consist of 89 QCA cells.From this result it can be concluded that if the circuit in figure 7 is designed in QCAdesigner,the approximate area of the circuit will be four times the area of the block i.e $0.40\mu m^2$ approximately.The area of the circuit is much less than that of CMOS binary multiplier.Moreover,if figure 8 is observed carefully, it will be seen that binary multiplier of any combination can be implemented by simply adding that many number of blocks in each level and the number of levels will be equal to the order of multiplication.For example,a 5X5 binary multiplier will have five levels with five blocks in each level.

5. CONCLUSION

This method successfully proposes an efficient circuit design of a binary combinational multiplier.From the simulation result, it can be seen that there is a delay in the generation of S_out and C_out.But,even if there is a delay,since the circuit is designed in blocks,this approach is undoubtedly much more modular,systematic and regular.

6. REFERENCES

[1] Ja'Ja', S.M.Wu.," A new approach to realize partially symmetric functions".Tech.Rep.SRCTR86-54, Dept.EE, University of Maryland, 1986.

[2] C. S. Lent, P. D. Taugaw, W. Porod , G. H. Berstein.," Quantum Cellular Automata.Nanotechnology", vol. 4, no. 1, pp49-57,January 1993.

[3] A. O. Orlov, I. Amlani, G. H. Bernstein, C. S. Lent, G. L.Sinder.," Realization of a Functional Cell for Quantum Dot Cellular Automata", Science, vol. 277, no. 5328, pp 928-930,August 1997.

[4] C. S. Lent, P. D. Taugaw." A Device Architecture for Computing with Quantum Dots", Proceedings IEEE, vol. 85, no. 4, pp.541-557,April 1997

[5] I. Amlani, A. O. Orlov, G. Toth, C. S. Lent, G. H. Bernstein, G. L.Sinder.," Digital Logic Gate using Quantum Dot Cellular Automata", Science, vol. 284, no. 5412, pp. 289-291,April 1999.

[6] M. Lieberman, S. Chellamma, B. Varughese, Y. Wang, C. S. Lent, G.H. Bernstein, G.L.Snider, F. Peiris.," Quantum Dot Cellular Automata at a Molecular Scale", Annals of the New York Academy of Sciences, vol. 960, pp. 225-239,2002.

[7] Whitney J. Townsend, Jacob A. Abraham." Complex Gate Implementations for Quantum Dot Cellular Automata", 4th IEEE Conference on Nanotechnology , pp. 625-627,August 2004.

[8] R. Zhang, K.Walus, W.Wang, G.A.Jullien.," A Method of Majority Logic Reduction for Quantum Cellular Automata", IEEE Trans on Nanotechnology, vol. 3, no. 4, pp. 443- 450, Dec 2004.

[9] K. Walus, G. Schulhof, G. A. Jullien, R. Zhang, W. Wang.," Circuit Design Based on Majority Gates for Application with Quantum Dot Cellular Automata", IEEE Trans Signals, Systems and Computers, vol. 2, pp. 1354-1357,Nov 2004.

[10] M. Momenzadeh, M. B. Tahoori, J. Huang, F. Lombardi.," Characterization, Test and Logic Synthesis of AND-RINVERTER (AOI) Gate Design for QCA Implementation",IEEE Trans on Computer Aided Design of Integrated Circuits and Systems, vol. 24, no.,pp. 1881-1893, December 2005.

[11] H. Rahaman, B. K. Sikdar, D.K. Das." Synthesis of Symmetric Boolean Functions Using Quantum Cellular Automata", International Conference on Design and Test of Integrated Systems in Nanoscale Technology (DTIS 06), pp.119-124, Tunis, Tunisia.

[12] Z. Y. Xu ,M. Fenga ,W. M. Zhang." Universal Quantum Computation With Quantum-Dot Cellular Automata In Decoherence-Free Subspace", Quantum Information and Computation, Vol. 0,No. 0000-000c Rinton Press,2008.

[13] Mostafa Rahimi Azghadi*, O. Kavehei, K. Navi."A Novel Design for Quantum-dot Cellular Automata Cells and Full Adders"

[14] Heumpil Cho." Adder Designs and Analyses for Quantum-Dot Cellular Automata", IEEE Transactions on Nanotechnology, Vol. 6, No. 3, May 2007

[15] Heumpil Cho, Earl E. Swartzlander." Adder and multiplier Design in Quantum-Dot Cellular Automata", IEEE Transactions on Computers, Vol. 58, No. 6, Jun 2009

[16] Geza Toth* , Craig S. Lent." Quantum computing with quantum-dot cellular automata", Physical Review A, Volume 63, 052315

[17] Pijush Kanti Bhattacharjee." Use of Symmetric Functions Designed by QCA Gates for Next Generation IC", International Journal of Computer Theory and Engineering, Vol. 2, No. ,April 2010 1793-8201

[18] Hema Sandhya Jagarlamudi, Mousumi Saha, Pavan Kumar Jagarlamudi." Quantum Dot Cellular Automata Based Effective Design of Combinational and Sequential Logical Structures", World Academy of Science, Engineering and Technology 60, 2011.

[19] C.Rovetta , M.Mouffron." De Bruijan sequences and complexity of symmetric functions", Cryptography and Communications journal, vol.3, no. 4, pp.207-225,(December,2011).

[20] S. Basu, S. Bhattacharjee." Implementation of Symmetric Functions Using Quantum Dot Cellular Automata", ICACNI,2014