An Efficient Full Adder Design using Different Logic Styles

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ABSTRACT

The paper discusses a comparative study of full adders with various logic style of designing. Logic style affects the switching capacitance, transition activity, short circuit current and delay. Various logic styles have been compared taking full adder as a reference circuit and power dissipation and delay as reference parameters. Simulation results of all the full adders at technologies of 180nm, 90nm, 45nm of CMOS process have been provided. It is observed that less power is consumed in the Transmission based full adder than the Convention full adder and Pass Transistor full adder.

General Terms

VLSI, Full Adder, CMOS

Keywords

CPL, Complementary CMOS, DPL, Transmission Gate (TG), Pass Transistor Logic, Adder Circuits, Low Power Logic Styles.

1. INTRODUCTION

Computational and market demands have driven VLSI microprocessors to double their performance every three years. It is impossible to keep up this performance rate through fabrication technology only. Improvements in other domains are necessary to support the performance rate. A good circuit design and choice of appropriate logic style is equally important in achieving this performance goal.

Enhancing the performance of macros is quite important in order to design high performance microprocessors. Arithmetic unit is the key element of any microprocessor, FPGA (Field Programmable Gate Array) and media processing applications. Performance of Arithmetic Unit is of vital importance in estimating the performance of processor. In today's world of mobility and portability, where efficient battery back up is necessary, power consumption of the system is a critical factor in determining system's performance. There are some other limiting factors too, that have reduced the development of microprocessors and that are fabrication technology, designer productivity and design cost. The increasing demand of high speed VLSI microprocessors can be addressed at various design levels such as architectural, circuit, layout and fabrication. Designing an Arithmetic Unit at a particular circuit level effects its performance as various performance determining factors such as switching capacitance, transition activity and short circuit current are strongly influenced by chosen logic style.

In this paper, various methods of implementing full adder using different types of logic styles have been discussed and their corresponding results have been summarized. Cadence tool has been used to get the results.

Section 2 gives the short introduction about various logic styles available, their advantages and disadvantages. Section 3 provides basic introduction power dissipation in CMOS devices. The implementation details of various full adders qualitatively are given in section 4. Results are given in section 5. Finally, some conclusions are drawn on the basis of results depicted in section 6 that are summarized in section 6.

2. LOGIC STYLE

Logic style of a circuit influences its speed, power dissipation, size and wiring complexity. The circuit delay depends upon the number of transistors in series, transistor sizes and wiring capacitances. Robustness with respect to voltage and transistor scaling as well as varying process, working conditions and compatibility with surrounding circuitries are important aspects influenced by implemented logic style.

2.1 Static / Dynamic logic style

In the static logic style, each gate output is connected either to Vdd or GND through low resistance path while in dynamic logic style; each gate output relies on temporary storage of signal values on the capacitance of high impedance circuit nodes. The dynamic logic gates are good for high speed applications. However, large clock loads and high signal transition activities due to pre-charging mechanisms result in excessive power dissipation. Therefore, Dynamic circuit design is not good for low power circuit design. Static Logic Style can be classified as Complementary CMOS logic, Ratio-ed Logic and Pass Transistor Logic.

2.1.1 Complementary CMOS

Complementary CMOS logic style is a combination of two networks; the Pull up Network (PUN) and the Pull down Network (PDN). The Pull up Network consists of PMOS transistors and Pull down Network consists of NMOS devices. The function of Pull up Network is to provide connection between gate output and Vdd, anytime the output of the gate is meant to be high. Similarly, function of Pull down Network is to provide connection between gate output and GND anytime the output of the gate is meant to be low. The Pull up Network and Pull down Network are mutually exclusive to each other. The noise margin and propagation delay depends on the input patterns.

The advantage of CMOS includes its robustness against voltage scaling and transistor sizing. The layout of CMOS is straight-forward and efficient due to complementary transistor pairs. The drawback of Complementary CMOS includes the usage of large number of transistor resulting in increased area overhead. Another drawback is the relatively weak output driving capability due to series transistor in output stage. However this can be corrected by using additional output buffers and inverters.

2.1.2 Ratioed Logic

It is an attempt of reducing the number of transistors to implement a logic function, at the cost of reduced robustness and extra power dissipation. The entire Pull up Network is replaced by a PMOS transistor known as load which is always grounded while the logic function is realized by the pull down Network.

a. Pseudo NMOS

It uses a total of N + 1 transistor for implementing an N- input logic function as compared to 2N transistors in Complementary CMOS. The nominal high output voltage is Vdd in this case because the pull down network is conditionally off when output is pulled high. However, the nominal low output voltage is not GND as there is contention between devices in pull down network and grounded PMOS load device. The size of the load device with respect to pull down device can be varied in order to optimize the noise margin, propagation delay and power dissipation. Since the overall functionality of Pseudo NMOS depends upon the ratio of PMOS and NMOS sizes, it is called Ratioed logic [11].

b. Differential Cascode Voltage Switch Logic (DCVSL)

It eliminates the problem of static currents (arises due direct current path between Vdd and GND) and provides rail to rail swing. It is based on differential Logic and positive feedback. The differential logic enables it to have its output, both in true and complementary form. The feedback mechanism ensures that the load device is turned off when not required. The circuit is still ratioed, thus increasing the design complexity. Power dissipation is still there due to cross over currents. During the transition, both PMOS and PDN are turned on for short duration of time, thus providing short-circuit path [13].

2.1.3 Pass transistor Logic Style

It attempts to reduce the number of transistors used to implement a logic function. The primary inputs are used to drive the gates of transistors as well as source drain terminals of the MOSFET. The use of reduced number of the transistors provides lower capacitance. However there is a problem of threshold voltage drop through NMOS transistor Logic which necessitates the use of swing restoration logic at the gate output.

Since the MOS networks are connected to variable inputs rather than constant power lines, therefore only one signal path is active throughout the entire network. As these pass transistor multiplexer structure require complementary control signals therefore, dual rail logic is used. As a consequence, two MOS networks are required which annihilates the advantage of using low transistor count. Layout of Pass transistor is not as straight-forward and efficient as complementary CMOS, due to their irregular structure. Some

of the pass transistor logic styles have been summarized below:

a. CPL (Complementary Pass transistor Logic)

In CPL, the given function is implemented by two pass transistor networks with one implementing the function f and the other implementing f'. CPL implements differential logic as every variable is represented in its true and complementary form. The logic structure of CPL is shown in figure 1.
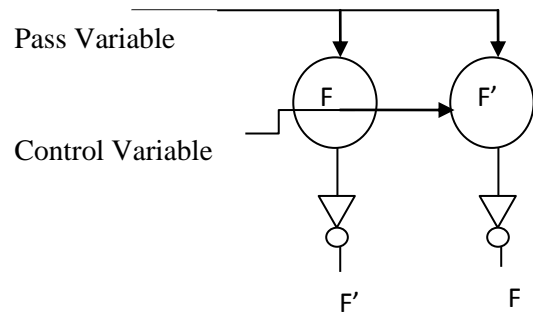

Fig 1: CPL Logic Structure

CPL suffered from problems of signal degradation when the signal is passed through a series of transistor, its value is degraded by one Vt (threshold voltage). The problem of threshold voltage drop can be eliminated by using level restoration circuit that consists of special type of inverters which has the ability of restoring logic to its full potential [7] as shown in figure 2.
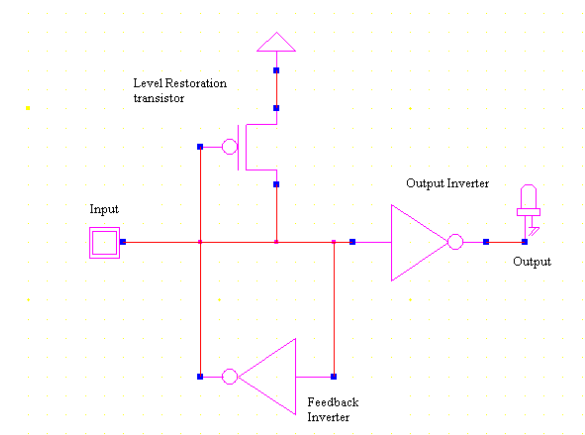

Fig 2: CPL Restoring Logic

b. DPL (Double Pass Transistor Logic)

It attempts to eliminate the problem of threshold voltage drop exhibited in CPL. It uses both PMOS and NMOS transistor to implement the true and its complementary logic function. Elimination of inverters (as used in CPL) results in enhanced speed, however buffering of signals after every two or three stages is necessary.

c. Transmission Gate(TG)

It consists of n-channel transistor as well as p-channel transistor with separate gate connections and common source and drain connections. The control signal is applied to gate of n-channel transistor and its complement is applied to the gate of p-channel transistor. By combining the characteristics of p-channel transistor as well as n-channel transistor, it is able to pass logic '1' and logic '0' efficiently without any distortion.

3. POWER DISSIPATION

There are three sources of power dissipation viz. static power, dynamic power and short circuit power dissipation [1]. Static power dissipation is associated with leakage current and can be improved with the advancement in fabrication technology only. Dynamic power dissipation is given by the following equation:

$$P_d = \alpha C_L V_{DD}{}^2 f_{CLK}$$

Where α is the switching activity, C_L is the load capacitance, V_{DD} is the supply voltage and f_{CLK} is the clock frequency.

Other source of power dissipation is short circuit power dissipation that arises when direct current flows from V_{DD} to ground. Short circuit power dissipation, depends on rise time and fall time because it is only during transition that transistors between V_{DD} and ground remains on and short circuit power dissipation comes into play. In the optimized full adder circuit, both transistor count and area has been reduced that lowers the dynamic power dissipation as well as short circuit power dissipation and hence the total power dissipation reduces.

4. FULL ADDER IMPLEMENTATION USING DIFFERENT LOGIC STYLES

The various logic styles discussed above can be used for implementing different elements of Arithmetic unit. Each of the circuit style has its own advantages and disadvantages. Full Adder is the basic design element of any Arithmetic Unit aiming to achieve three basic design goals such as minimizing the power consumption, minimizing the transistor count and increasing the speed. Minimizing the transistor count will lead to lower power consumption, as well as high speed.

The design details of full adder implemented using three different logic styles viz. CMOS, Transmission Gate and Pass Transistor Logic are given below.

I. CMOS based Full Adder

CMOS Full Adder consists of 20 transistors in each full transistor. The schematic diagram of 4 bit CMOS full Adder is designed using Cadence tool shown in figure 3. The design has been simulated at180nm , 90nm, 45nm of CMOS process. The full adder operation can be stated as follows:

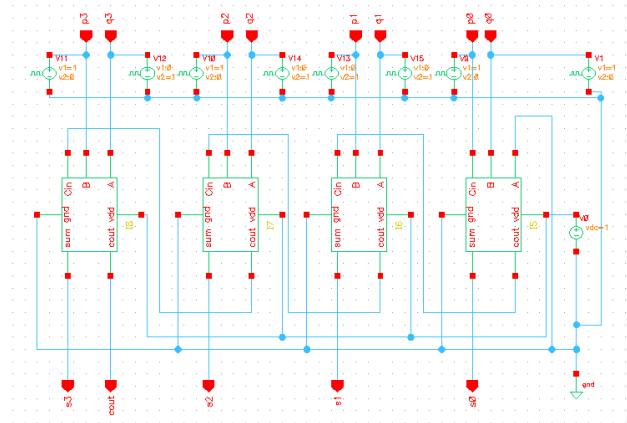Sum = (A xor B) xor C

Carry = A (A xor B)' + C (A xor B)

Fig 3: Schematic of CMOS Full Adder

II. Transmission Gate

Transmission Gate Full Adder uses 15 transistors to implement the sum and carry logic. Transmission Gate Full Adder performs better than CMOS Full Adder in case of power dissipation as well as delay with lesser number of transistors being used. Its schematic diagram is shown in figure- 4:
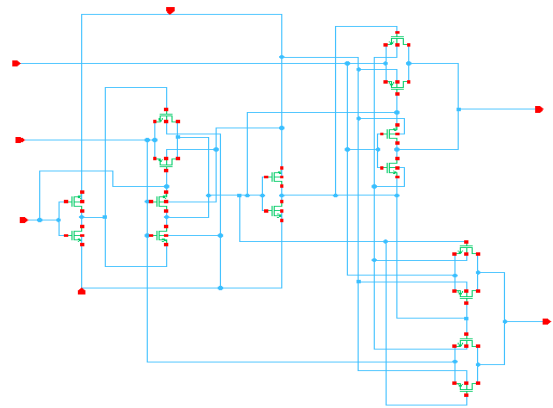

Fig 4: Schematic diagram of TG Full Adder

III. Pass Transistor

The proposed 9-transistor Full Adder is designed using Pass Transistor logic. It uses lesser number of transistors than the above two. Power dissipation is quite less in this case. Simulation results of the proposed full adder have been shown 5:
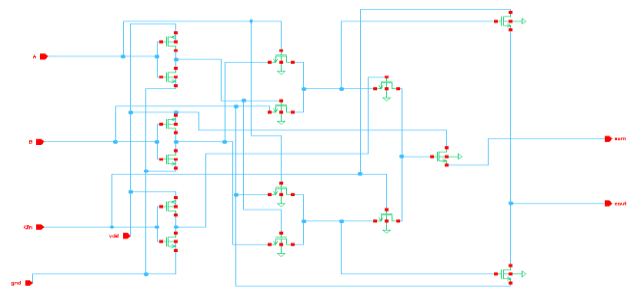

Fig 5: Schematic of pass transistor based Full Adder

5. RESULTS AND DISCUSSION

The simulation result shows in fig 6 that, at a supply voltage of 1.2V, the Full Adder exhibits a power dissipation of 3.9 µW at the clock frequency of 1GHz. Output has full voltage swing but the main drawback is the larger number of transistors used. . The way functions are implemented in transmission gate full adder and pass transistor is different from implemented in CMOS based Full adder. But transient analysis is same. Similarly the signals used are also same.
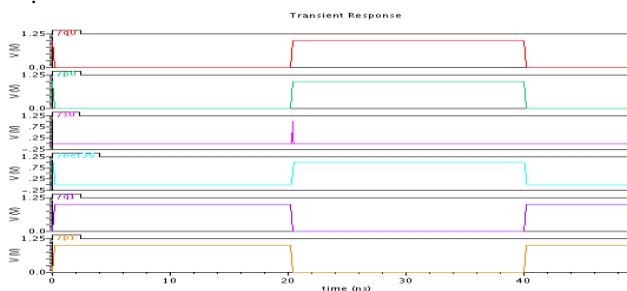

Fig 6: Transient Analysis of Full Adder

The CMOS ,TG and Pass transitor based full adder is designed for the various CMOS technology like for 180nm,90nmand 45 nm results for the power consumed is calculated in power calculator . The comparison of power consumed in the CMOS, TG, Pass Transistor based full adders are given in table 1

Table1: Comparison among various Adders

Circuit (Full Adder)	Power		
	180 nm	90 nm	45nm
CMOS Full Adder	3.998E-6	348.9E-9	79.12E-9
TG Full adder	1.519E-6	180.7E-9	24.86E-9
Pass Transistor Full Adder	1.823E-6	251.8E-9	27.36E-9

6. ACKNOWLEDGMENTS

7. CONCLUSION & FUTURE WORK

From the various logic styles discussed and taking results into consideration, it is very clear that pass transistor logic provides the minimum load capacitance as well as transistor count but suffers from the problem of voltage degradation which can be improved using transistor sizing. The power dissipation is least in the case of transmission gate transistor implementation of full adder due to reduced load capacitance. The present work can be extended to make complete Arithmetic unit.

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