Techniques for Sub-threshold Leakage Reduction in Low Power CMOS Circuit Designs

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ABSTRACT

Power dissipation is a key consideration in the design of nano-scale CMOS VLSI circuits. Various techniques have been proposed for reduction of leakage in CMOS transistors. As the technology is emerging power dissipation due to leakage current has become a major contributor of total power consumption in the integrated devices. For high performance and device reliability, reduction of power consumption is highly desirable. Thus the importance of low power circuits has increased currently. The trend of scaling down has led to the increase in sub threshold leakage current and hence static power consumption. In this paper the different leakage reduction techniques for deep submicron technologies are focused comprehensively. The predominating sub threshold leakage current problem can be overcome by techniques like stacking of transistors, power gating, optimal body bias voltage generation at the circuit level thus providing a large range of choices for low-leakage power VLSI designers.
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General Terms

Your general terms must be any term which can be used for general classification of the submitted material such as Pattern Recognition, Security, Algorithms et. al.

Keywords

Sub threshold leakage, low power, stacking of transistors, power-gating and body bias voltage.

1. INTRODUCTION

In recent years the size of transistors has been reduced to increase the operational speed of devices and density on chip to achieve better manufacturing results. In the growing world of mobile applications power consumption is a top issue for VLSI designers since battery life is the main concern. For higher performance, scaling down of supply voltages ensures continuous reduction in threshold voltages of transistors that leads to increase in sub-threshold current implying rise in static power consumption. With this technology trend transistor leakage power has increased exponentially [1]. Miniaturization in feature size, short channel lengths and low threshold voltage tends to increase the sub threshold leakage current. Therefore, the transistor does not turn off completely when it is off thereby increasing static power dissipation. Moreover thinner gate oxides have also caused increase in gate leakage current [1]. Recent research has shown that the sub threshold leakage current is more prominent than the dynamic current in the overall power dissipation [2][3]. Reduction of sub threshold leakage power is highly desirable for battery operated portable systems, which remain in the standby state for the majority of their operating time. Depending on the circuit operating mode IC power dissipation comprises of various components. Standby leakage components can be made smaller by changing body bias conditions or by power-gating. Figure 1 shows the sub threshold leakage trends with deep submicron technologies. It clearly follows Moore's law and is expected to increase 32 times the device size by the year 2020 [4].

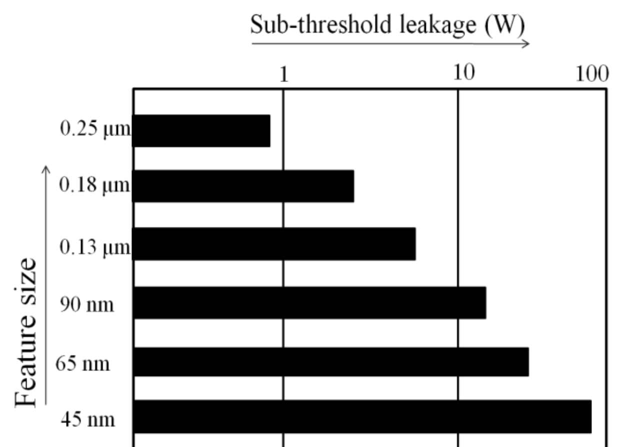


Figure 1 Sub threshold leakage current trends [4].

2. SOURCES OF LEAKAGE CURRENT

2.1 Factors for power dissipation

The main sources of power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub threshold current. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors. Also, gate induced drain leakage and gate direct tunnelling leakage have become the significant sources of leakage power.

2.2 Weak Inversion leakage current

The sub threshold leakage is the current between drain-source of a transistor operating in weak inversion region. The sub threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOSFET [5]. A MOSFET is said to operate in weak inversion region when the surface potential at the source terminal of the channel is enough to form an inversion layer, but band bending is less that is required for strong inversion. The magnitude of the sub threshold current is a function of the temperature, supply. voltage, device size and process parameters, so the threshold voltage (Vth) plays an important role. I_{SUB} is calculated by equation as below:

$$I_{SUB} = \frac{W}{L} \mu V_T^{\,2} C_{sth} \exp \frac{VGS - VT + \eta V_{DS}}{n\,Vth} \left(1 - \exp\frac{-VDS}{Vt}\right) \quad (1)$$

Where W and L denote the transistor width and length, μ denotes the carrier mobility, Vt =kT/q is the thermal voltage T, $C_{sth} = C_{dep}+C_{it}$ denotes sum of depletion region capacitance and interface trap capacitance η is DIBL coefficient [5] and n is slope shape factor as n= C_{sth} / C_{ox}

C_{ox} is the gate input capacitance per unit area of the MOS gate. Collectively the leakage current of an OFF transistor is

$$I_{OFF} = I_{REV} + I_{GIDL} + I_{SUB} \quad (2)$$

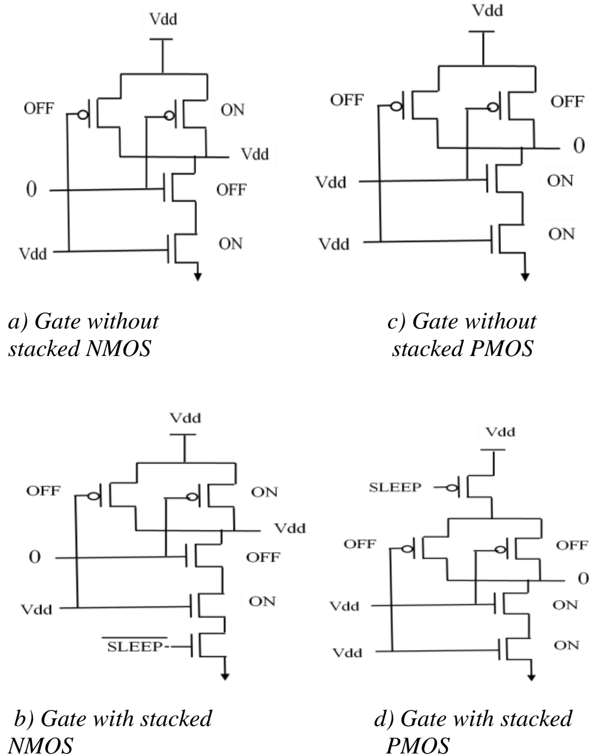
Where I_{SUB} is the dominant component because I_{REV} (small reverse bias current between source and drain regions when the transistor is OFF) and I_{GIDL} (gate induced drain leakage current) are maximum when $V_{DB} = V_{DD}$. For short channel devices, I_{SUB} increases with V_{DB} due to DIBL (drain induced barrier lowering) effect.

3. LEAKAGE REDUCTION METHODS

Most microelectronic systems remain in standby state for considerable time. So the expected standby state duration may be calculated while devising a power management policy. Various strategies can be adopted based on mode of operation of the circuit. In this section methods to decrease the sub threshold leakage current are presented for circuits that are in standby or active state.

3.1 Stack Effect Based Technique

If the value of the input of a circuit in standby mode is known, some NMOS and PMOS can be added in series with gates to increase the stack effect and reduce the leakage [6].



a) Gate without stacked NMOS

c) Gate without stacked PMOS

b) Gate with stacked NMOS

d) Gate with stacked PMOS

Figure 2 Stack Effect

In Fig. 2 a) and b) the output of the gate is high in standby mode, which means pull down network is OFF. Hence putting an OFF transistor in series with pull down network in standby mode will not change the output value. This increases the resistance between supply and ground, thereby reducing leakage of logic gate as seen in Fig. 2 c) Stack Effect. Also, in Fig. 2(d) the insertion of a leakage control transistor, which can be shared by multiple gates, is depicted. Also, by dividing the circuit and stacking into two half width of the total transistor size sub threshold current is reduced [4]. Here stacked transistors turn ON and OFF simultaneously. A positive potential gets generated at the stacked transistor node due which gate to source voltage V_{gs} becomes negative and the sub threshold is minimized.

3.2 Power Gating

Power Gating includes adding a sleep transistor between actual ground terminal and circuit ground (termed as virtual ground) [7]. In sleep mode to cut-off the leakage path this device is turned off. Power gating uses high Vth sleep transistors that cut off Vdd from circuit block when not switching. This is also known as MTCMOS (Multi threshold CMOS). Power gating affects the architecture and increases time delays. In MTCMOS technique, high threshold voltage transistor is inserted in series with the power supply in existing circuit. In active mode sleep transistors are turned ON and facilitate normal operation since there is a direct path from supply to ground. During standby the sleep transistors are turned OFF, creating the virtual path between the supply and the ground. In SCCMOS (Super Cut-off CMOS) technique the sleep transistors have identical low Vth and helps in reduction of additional delay caused by high Vth transistors during active mode.

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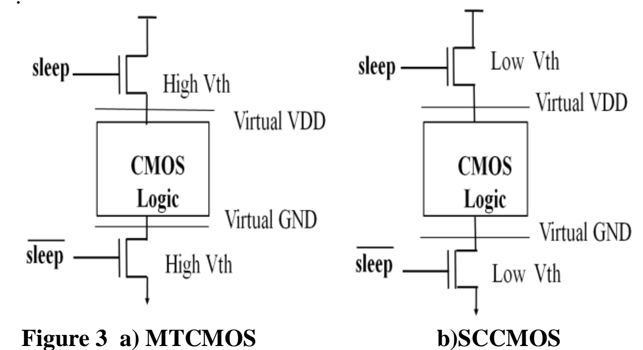

Figure 3 a) MTCMOS b)SCCMOS

Another variation in which sleep transistor and stacking are combined together called as sleepy stack technique divides the existing transistors into two half size transistors like the stack approach. Further, additional sleep transistors are inserted parallel to one of the divided transistors. The sleep transistors are turned off during sleep mode, and stacked transistors suppress leakage current, during active mode they are on. Area penalty in this type of approach is more and a matter of concern. Fig. 4 [1] shows the structure in which PMOS sleep transistors are added in parallel to each of the divided network.

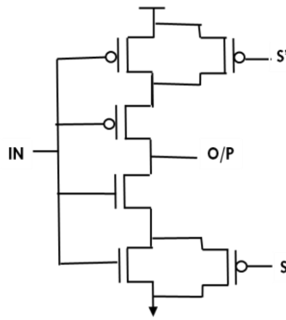

Figure 4 Sleepy stacking

3.3 Body Biasing Technique

In Body biasing method the substrate/wells on the die are biased to something different other then GND (of NMOSFET) or VDD (of PMOSFET). This technique reduces sub threshold leakage and has little effect on dynamic power (the source and drain junction capacitances are changed to lower values by means of body biasing). The body bias voltage can be applied to the circuit from an external source or an internal source. In the external approach, the design usually includes a charge pump circuitry that generates a reverse body bias voltage and/or a voltage divider to generate a forward body bias voltage. Reverse body bias (RBB) method applies a negative body-to-source voltage to NMOS transistor and thus raises the threshold voltage. Whereas, a positive body-to-source voltage is applied to NMOS transistor in Forward body biasing, this lowers the threshold voltage.

Variety of body biasing methodologies exists. A fixed body bias voltage value that is set during design phase can be applied to entire "chips". Adaptive body biasing can be used to correct systematic manufacturing variations, by decreasing Vth variations. Dynamic body biasing reduces temperature and age effect. This makes power management modes more effective at optimizing very low power operation. It changes the body bias several times, providing flexibility while the chip is operating rather than fixing the body bias for once during design or production tests [8]. So, leakage current reduction can be achieved by using RBB thereby increasing the threshold voltage of transistors in the standby state [9]. Threshold voltage, Vth is related to reverse body bias voltage (between source and body) Vsb by equation as follows:

$$Vth = Vtho + \gamma \left(\sqrt{|2\emptyset_F + Vsb|} - \sqrt{|2\emptyset_F|} \right) \quad (3)$$

Where γ is body effect co-efficient, $\emptyset_F$ is Fermi potential, Vsb is source to bulk potential difference. To reduce the leakage power and increase threshold voltage of a circuit, adaptive reverse body biasing (ARBB) technique is proposed during standby mode [10]. In this technique, a leakage monitoring circuit is used to determine the optimal body bias voltage of CMOS circuits. In standby mode, the first step includes monitoring each leakage component. The leakage monitoring circuit separates the ISUB and IBTBT currents from the total leakage components. In the second step, sub threshold leakage current and BTBT (Band-to-Band-Tunnelling) leakage are compared with each other. Comparison of these two currents is possible by a current mirror comparator circuitry. If the sub threshold leakage current (ISUB) is greater than the BTBT leakage current (IBTBT), the RBB will increase [11].

On the other hand, if the sub threshold leakage current is smaller than the BTBT leakage, forward body bias will increase. This is achieved with a charge pump circuit that charges or discharges according to the two signals coming from current comparator and its own bias voltage. In standby mode the point where the sub threshold leakage is equal to the BTBT leakage is found to be the optimal leakage point [10]. As the optimal body bias point is detected, body voltage adjustment is stopped. Fig. 5 Optimal Vth and body bias control mechanism in standby mode, shows the block structure of the system with feedback. This body voltage can be applied to a chip for controlling the sub-threshold leakage.

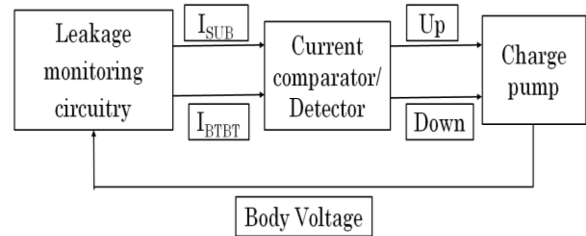

Figure 5 Optimal Vth and body bias control mechanism in standby mode

4. CONCLUSION

It is highly undesirable to waste battery power on long standby mode. To curb this problem, various leakage power reduction techniques are discussed in this paper that reduces the leakage power in nano-scale VLSI circuits. Stacking performs well as the threshold voltage decreases and aids in minimization of transistor sizes. But, stacking is more effective in reducing leakage in an active mode of circuit operation. Sub threshold leakage reduction during standby mode in SCCMOS technique is comparatively better than MTCMOS and stacking. However, these techniques require significant circuit modification and have not been robust enough to be applied to VLSI system. Optimisation of body bias voltage approach presented in this paper gives better performance over other methods in terms of power and delay. Further, it reduces hardware overhead as compared to various other power reduction techniques that employ optimal body bias selection.

5. ACKNOWLEDGMENTS

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