# Reconfigurable Adder Architectures for Low Power Applications

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## ABSTRACT
The growing design complexity has attracted the designs with Reconfigurable fabrics, where adaptable fabrics are utilized to solve the computational problems. Reconfigurable computing provides the flexibility in arriving at the problem specific architectures which helps in improving the performance due to custom approach. In this paper, a flexible reconfigurable architecture with different adder variants like Ripple Carry, Carry Look-ahead, Carry Select and Carry Bypass adders are implemented to form dynamically reconfigurable Hybrid adder architectures. Such hybrid architectures are utilized for the applications where design constraints are only for low power or high performance or the low area or sometimes a balanced design metrics. The design was modelled using Verilog HDL and synthesized in Synopsys Design Compiler by mapping to TSMC 65nm technology node. Standard ASIC design methodologies are considered to bench mark the results. The proposed architecture enables the designer to perform efficient Design Space Exploration. The design can be made adaptable to any of the reconfigurable processor and a similar improvement can be obtained. The proposed architectures results in 18-54% reduced power consumption when designed with various combinations of reconfigurable adder architectures and also accounted for 14-44% of area reduction.

## Keywords
Adders, Reconfigurable, Low Power VLSI

## 1. INTRODUCTION
In the portable world, the major issues in the designs are low power and flexibility. Most of the portable computing devices contain the sophisticated and power hungry signal processing techniques, hence there is a need to reduce the power consumption of these devices or to increase the power back-up of the portable devices. Flexibility in the components is another concern regarding the use of programmable components which face significant power and performance trade-offs. Therefore there is a requirement to develop the efficient architectures at most aspects of the designs quality matrices.

Most of the electronic applications require adders in their computations, as they are the most commonly and copiously used components in digital design. Hence the impact of the adders will be large on the overall performance of the system. Many organizations have spread their interest in the research of "high performance" / "low area" / "low power" adders [1-3]. From past decade, the design of reconfigurable adders has been attracted, which helps in achieving the real time signal processing of the multi-media applications [4-7]. Furthermore the research will integrate the programming and reconfigurable computations on the chips. Hence flexible adders are required for all arithmetic computations of the digital design units.

The reconfigurable adders reported in [4 -7] has adder variants and partitioned the larger width system using additional bits so that smaller adders are achieved. For example in [4], the author has partitioned the 64 bit Carry select adder to perform as one 64-, two 32-, four 16-, and eight 8-bit adders. Similarly in [7], a carry skip adder has been illustrated. Such adders will provide only the selection of the bit widths of the adders and improves the efficiency of the design. But still the designs can incorporate more flexibility in to the system by introducing different adder architectures. An effort has been put in [8], to add the extra flexibility into the system. Here different adder variants of smaller bit widths are incorporated in the larger adder system. Such architectures are called as Heterogeneous adders.

This paper proposes the more flexible reconfigurable adder architectures by exploring the regularity of the adder architectures with minimum additional multiplexers. Here reconfigurability has been achieved between the adder variants. Regularity between the adder variants helps in reducing the large amount of area and power consumption. The following sections of the paper are organized as follows. Section 2 briefs about the reconfigurable architectures and classifications of computing. Section 3 deals with the regular and proposed architectures of reconfigurable computing. Results are discussed and concluded in the sections 4 and 5 respectively and the references are provided in section 6.

## 2. RECONFIGURABLE COMPUTING
Reconfigurability is the method which combines the high performance hardware by some flexible software with the use of computing fabrics. In reconfigurable computing there is the possibility of adapting to the hardware during the runtime by the use of new circuit. However the reconfigurability can be viewed with different perspectives viz. the system level and at the functional unit level. The reconfigurable systems are again classified based on their degree of coupling between the functional units and the processing units. These systems may typically contain one or two processors, one or more memories and one or more reconfigurable fabrics.

Secondly the reconfigurable fabrics are again classified into fine grained and coarse grained reconfigurable fabrics. In fine grained reconfigurable fabrics, the bit level reconfigurability will be achieved in the functional units, whereas in coarse grained fabrics, reconfigurability is achieved between the operations of the functional units and also between the entire functional units. The functional units may contain the arithmetic and logical units and possible may also contain the memories [9 - 12].

## 3. ARCHITECTURE

As mentioned in section 2, reconfigurability can be achieved with different levels and with combinations depending on the application. Coarse grain reconfigurable architecture is proposed in this paper. The adder variants like Ripple Carry, Carry Look-ahead, Carry select and Carry bypass adders are configured to achieve the reconfigurability in the design. Figure 1 shows the regular architectures of the Ripple Carry, Carry Look-ahead, Carry select and Carry bypass adders.

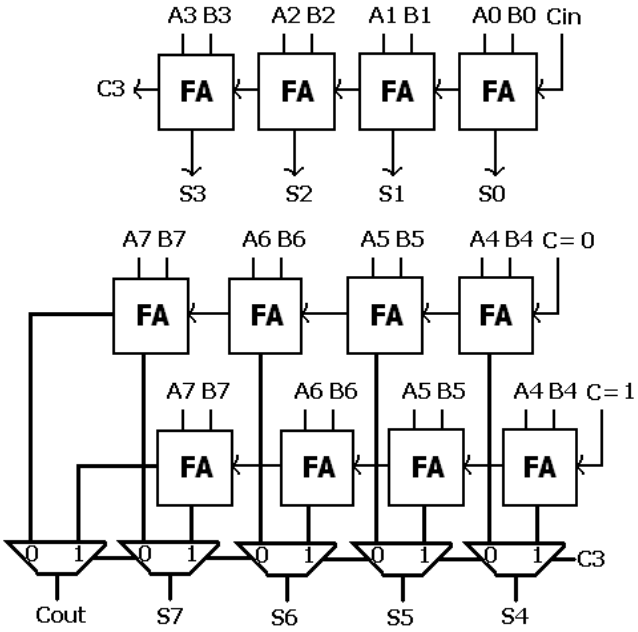


**Figure 1 (a): Regular CSLA architecture**

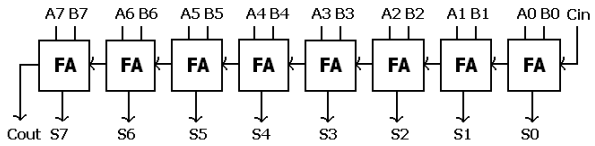


**Figure 1 (b): Regular RCA architecture**

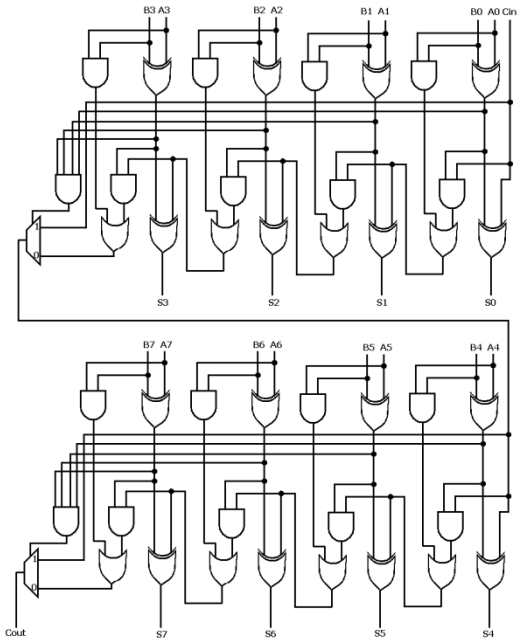


**Figure 1 (c): Regular CBA architecture**

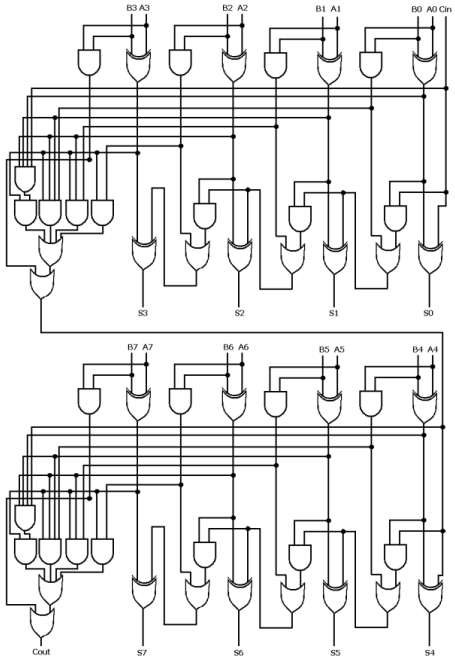


**Figure 1 (d): Regular CLA architecture**

In the state of the art reconfigurable architectures, only bit width is configured. Based upon the variable bit width, the designer chooses different system constraints. In the state of the art hybrid architectures, there is no scope for dynamically selecting the architectures. Hence in both existing reconfigurable architectures and hybrid architectures, the designer has only limited scope for design space exploration. In this paper we address both of the above limitations. The designer can; not only

vary the bit widths, but also dynamically choose different architectures there by one can efficiently conduct design space exploration.

Different adder variants are considered as the functional units. The combinations of these adder architectures are used to design the reconfigurable architectures. Such reconfigurable architectures aids in achieving different quality metrics for the designs at the system level. For example system level designs like Image processing applications has high priority for performance and in speech processing of signals have higher priority for power and less priority with its performance. Therefore reconfigurable architectures providing such flexibility save the chip area and power by combining the architectures of both design constraints. However from the system level perspective, different applications operate at different design constraints, but it is the basic building units operation that brings the difference. Hence in this paper effort has been put to arrive at the reconfigurability with adder architectures, which enables different corners for analysis. The corners like low power, less area, high performance can be approached individually, or combined or balanced as per the requirement of the applications.

The combinations of reconfigurable architectures proposed in this paper are a) (RCA) Ripple Carry Adder with each of the following, (CLA) Carry Look-ahead Adder, Carry Bypass Adder, and Carry Select Adder. b) CLA with Carry Bypass Adder. Regularly these architectures are implemented as separate individual functional units as shown in Figure 2 (a). Each of the functional units will have different adder variants and their combinations are mentioned above. The individual regular architectures of the adder architectures are shown in Figure 1. Full Adders, Multiplexers and basic gates like AND, OR & XOR are the basic buildings of adder architectures. The demerits of the regularly implemented reconfigurable architectures are; more area and more power consumption due to the separate individual implementation style. The more area will lead to higher chip area and lesser features with the application or more features with larger device and reduced power back-up for the system.

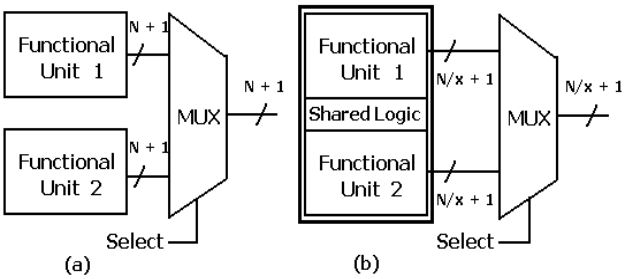


**Figure 2: (a) Regular Reconfigurable architectures, (b) Proposed Reconfigurable architectures**.

Here N = adder bit-width. In Figure 2 (b) x = 2 for proposed reconfigurable RCA – CSLA architecture and x = 8 for proposed reconfigurable adder architectures (RCA – CLA, RCA – CBA, CLA – CBA).

By exploring the regularity of the adder architectures, the logics are shared to achieve the reconfigurability in the proposed architectures. Figure 2 (b) shows the abstract view of the proposed reconfigurable adder architectures. In the RCA – CLA combination, the logics of CLA are utilized and RCA is achieved at the cost of some additional multiplexed circuitry to the CLA, and area of complete RCA is saved. This helps in reduced area and reduced power consumption. Proposed RCA – CLA reconfigurable adder is shown in Figure 3. Similarly in RCA – CBA combination, additional multiplexed circuitry for the CBA will derive RCA architecture. Even though the CBA will behave as RCA if it doesn't satisfy the condition of bypass, but to access particularly RCA architecture additional multiplex circuitry is required when the bypass condition is satisfied. The proposed reconfigurable RCA – CBA architecture is shown in Figure 4. The proposed RCA – CSLA reconfigurable architecture shares the logic of the First half of the CSLA as shown in the Figure 5. In proposed CLA – CBA reconfigurable architecture additional Multiplexed circuitry is used for CLA to arrive at the reconfigurable CLA – CBA architecture and it can be observed in Figure 6. All the reconfigurable adder architectures are implemented for 8 bit-widths.

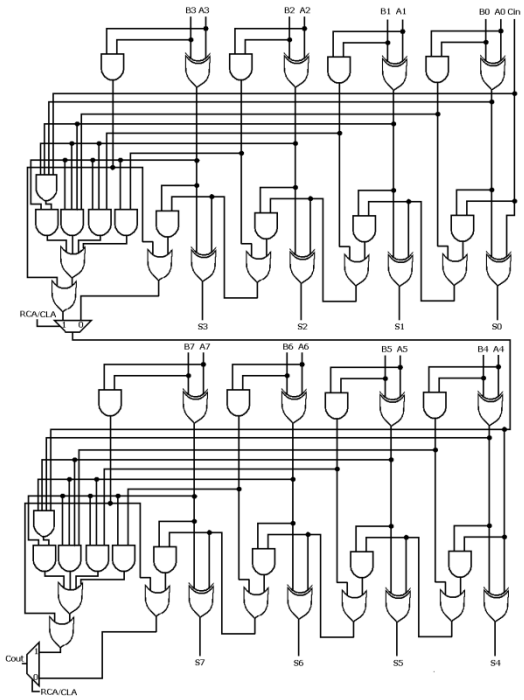


**Figure 3: Proposed Reconfigurable RCA – CLA Architecture**

The other important advantage of the sharing logic in proposed reconfigurable architectures is its simpler control logic and also it reduces the area for its implementation. Regular reconfigurable architecture needs "8 + 1" multiplexers to provide the reconfigurability among the 8 bit adder architectures. But in the proposed architectures it requires only two multiplexers (for multiplexing the carry logic) for the 8 bit adder architectures due to the merging and sharing among the adder architectures.

Resource sharing: Merging the architectures of two adder

variants flexibles the concept of resource sharing and provides space for sharing more logics. This concept reduces the required area at the comparable performance. The reduced area will impact to reduce - power consumption, chip cost, fabrication time and in some cases aids in the addition of extra feature for the applications. By using this in the above mentioned reconfigurable adder architectures, the complexity in the control logic will be increased. Resource sharing concept can be utilized for any bit widths and for any levels of abstraction. The benefits would be higher when incorporated for higher bit-widths.

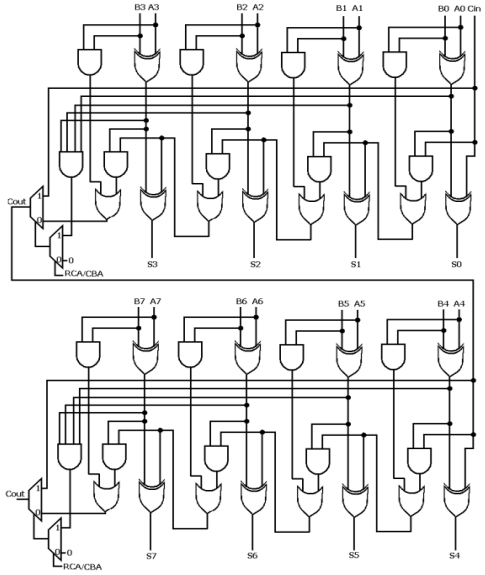


**Figure 4: Proposed Reconfigurable RCA – CBA Architecture**

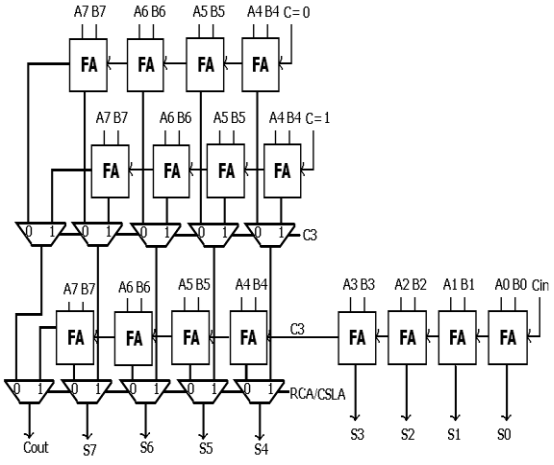


**Figure 5: Proposed Reconfigurable RCA – CSLA Architecture**

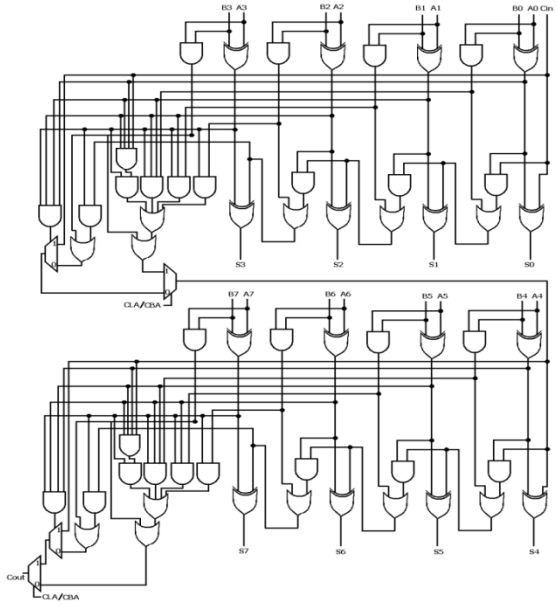


**Figure 6: Proposed Reconfigurable CLA – CSLA Architecture**

## 4. RESULTS AND DISCUSSIONS

Both the conventional and the proposed reconfigurable architectures are designed and developed in gate level for synthesis, using the Synopsys Design Compiler EDA tool. The designs were simulated using the Mentor Graphics Model-sim simulator and verified for functionality with the help of waveform editor. A standard ASIC design methodology was considered to benchmark the results. The results are tabulated in Table 1. The designs were targeted to the 65nm technological node and all required input parameters are applied as per the technological node. As per the test set-up, the design was synthesized to get accurate measurement of quality metric values.

Table 1 gives the comparisons of both proposed and conventional reconfigurable adder architectures of 8bit width. From the Table 1, we can observe that the significant amount of area of the proposed architectures has been reduced. By reflecting the area reduction, the power consumption has also got reduced. As mentioned in the section 3, the shared logic between the adder variant's has reduced the area required and also reduced the power consumption. From this we can prove that the area is one of the factors to reduce the power consumption. Regularity in the architectures has made the logics to be shared and enables the flexibility for operation at different design constraints. This helps in incorporating the reconfigurable architectures where the design supports various applications and yields in reduced chip area and power consumption. The reduced area will also reduce the chip cost and fabrication time.

The main advantage of resource sharing concept is to reduce the implementation area; and it was possible due to the merging of architectures between the adder variants. The reduced area will directly impact on the power consumption, as lesser gates area will lead to lesser switching activity. The results of the proposed

**Table 1: Comparison of Conventional and Proposed reconfigurable adder architectures of 8 bit width**

| Adder variant | | CLA_CBA | | | RCA_CBA | | | RCA_CLA | | | RCA_CSLA | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | | Existing | Proposed | % gain | Existing | Proposed | % gain | Existing | Proposed | % gain | Existing | Proposed | % gain |
| Area | | 290.880 | 249.120 | 14.35 | 253.430 | 130.68 | 44.49 | 249.120 | 151.92 | 39.01 | 254.159 | 199.430 | 21.52 |
| Timing | | 1.160 | 1.160 | NC | 1.160 | 1.100 | 5.17 | 0.850 | 0.830 | 2.35 | 0.68 | 0.730 | -7.35 |
| Dp | Ip | 43.315 | 35.490 | 18.06 | 43.065 | 18.591 | 56.83 | 43.244 | 20.587 | 52.39 | 53.529 | 41.766 | 21.97 |
| | Sp | 11.585 | 9.101 | 21.44 | 7.803 | 4.286 | 45.06 | 8.392 | 5.651 | 32.66 | 6.487 | 4.958 | 23.57 |
| Lp | | 2.925 | 2.480 | 15.21 | 2.833 | 1.316 | 53.54 | 2.907 | 1.476 | 49.21 | 3.629 | 2.856 | 21.29 |
| Tp | | 57.825 | 47.071 | 18.59 | 53.702 | 24.194 | 54.94 | 54.543 | 27.715 | 49.18 | 63.646 | 49.581 | 22.09 |

Note: Area in Square microns; Timing in (ns) nano seconds; "Dp" is Dynamic Power;
"Ip" is Internal Power in (uW) micro watts; "Sp" is Switching Power in (uW) micro watts;
"Lp" is Leakage Power in in (uW) micro watts; "Tp" is Total Power in (uW) micro watts;

approach for the 8-bit reconfigurable adder architectures with this concept has enabled the design to be analyzed from different analysis of corners like less area, low power and comparable performance. Similar kind of results can be obtained for different bit widths and more the bit widths more will be opportunity for resource sharing and higher will be efficiency of quality metrics. This Concept can be applied at any levels of abstraction.

The proposed concept will enable new corners of optimizations like "low area - low power" for same performance, "lowest power", "smallest area" as per the design constraints. It also enables new applications for the existing chip architectures.

## 5. CONCLUSION

A coarse grained reconfigurable fabric is implemented in this paper; the proposed 8 bit architectures results in 18-54% reduced power consumption when designed with different combination of reconfigurable adder architectures and also accounted for 14-44% of area reduction. A standard ASIC design methodology has been used to test and benchmark the results. The design was mapped to 65nm technological node and synthesized using the Synopsys Design Compiler. The partitioned multiplex concept has reduced the area and thereby directly reduces the power consumption of the design. The proposed reconfigurable architectures can be utilized where the application needs ultra low power in terms of leakage, high performance, low area, and a balanced design quality metrics. Further carrying this reconfigurability in to the system level will impact the same way and helps in accommodating all adder variants within the same/reduced area of the regular architecture. These architectures are pervasive and can be implemented at various levels of hierarchical abstractions.

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