Efficient Comparator based Sum of Absolute Differences Architecture for Digital Image Processing Applications

Narendra C.P
Asst. Professor, Dept. of ECE
Bangalore Institute of Technology
Bangalore, India.

K.M. Ravi Kumar, Ph.D
Professor & PG Coordinator,
Visvesvaraya Technological University
Regional Office, Mysore, India.

ABSTRACT
The prolific use of images & videos in portable devices, raised the need to develop the efficient architectures for the ever increasing demand of portability with low power and high performance quality metrics. However the images and videos are the information's to be stored, but there compression while storing is the important part. This paper introduces a basic hardware component "comparator" for the compression architectures. Comparator augments as general purpose core to Sum of Absolute difference (SAD) architecture used for the object recognition, generation of disparity maps of the stereo images and for estimating the motion in videos. The Subtraction part of the comparator is optimized by providing the parallel computation in processing the 2's complement operation. Transistor stacking and Logic optimization concepts are utilized to reduce the leakage power of the comparator design. 4-bit wide Comparator with "smallest of two binary numbers" functionality is modeled using Verilog HDL and synthesized using Synopsys Design Compiler. The design was mapped to 65nm technological library node and results were benchmarked with respect to standard ASIC design methodology. The proposed architectures have resulted in reduced leakage power about 7-42 % for different proposed architectures and enabled the different corners for analysis.

Keywords
Adder, Comparator, SAD, Digital Signal Processing, Low Power VLSI

1. INTRODUCTION
Video processing is one of the techniques in Image processing which contains the filters where video frames are the inputs and outputs. The video frames may have some parts to be in motion or the entire frame. Hence video frames forms the vectors for estimating the motion. The motion is a 3-D scene while the image will be a projection of 3D scene on to the 2D plane. In today's world compression ratio plays the major role in the field of image processing. But the motion in the video scene will reduce the efficiency of the compression ratio. By exploiting the similarities between the video frames, efficiency of the compression ratio can be increased. The SAD algorithm is the simple metric system where the absolute difference between the corresponding elements is added and the smallest SAD value among the SAD blocks is considered as the similarity image.

The other matching criteria for the motion estimation are mean absolute difference (MAD), mean square error (MSE), sum of absolute transformed difference (SATD). MAD implementation is simple and easy but it exaggerates the smaller differences and results inferior to MSE. While MSE provides accurate results but its implementation are complex for both software and hardware. However the SATD has better quality prediction technique, an added transformation will increase the hardware complexity. Even though MAD is simple and easy for implementation but its average operation needs an divider which is not needed in SAD as the averaging is not required due to the constant block size during subtraction. The other important advantage of SAD is that needs only addition, averaging between the pixel values like MAD is not required. This makes overall computation simpler than all other matching criteria algorithms [1- 5].

In real time coding applications, the computational cost of the Block matching algorithm is a significant problem. Many VLSI architectures are developed to reduce the computational cost and its complexity by speeding up the associated arithmetic calculation [4]. The various coding systems don't provide the flexibility as suggested to be with VLSI implementations. The other reasons to go for VLSI design is their adaptability to newer developments, sufficient performance and also faster design times by re-use of the designed IP cores.

Due to the increasing demand for the portable devices with low power consumption and high performance; many research organizations has put their effort on the development of architectures with such design characteristics. Such kind of architectures at the basic building block level would impact largely at the efficiency. In the proposed architectures, effort has been put to improve the efficiency of the architectures at the system level by optimizing the architectures at basic building component level. In this paper, efficient hardware architecture for the basic building block – "comparator" of the SAD architecture is implemented. In comparator, the subtraction part is optimized by exploring the parallel computation in the existing architecture. Logic optimization technique is utilized to achieve the power efficient architecture. The optimizations at the component and basic building block levels are addressed. The new comparator architectures are proposed which optimizes design metrics such as performance & power.

The other sections of the paper are organized as follows. Related work is briefed in section 2. Section 3 gives the background about SAD Processor for its application in Digital image processing. Architectural artifacts are characterized in section 4. Methodology is discussed in Section 5. Results and discussions are provided in section 6. Finally the paper is concluded in the section 7 and references are given section 8.

2. RELATED WORK
In SAD architecture the similarities between the images are measured by calculating the absolute differences between the image pixels and their corresponding ones within the block. Then these absolute differences are added within the block,

and compared against such SAD blocks for the smallest value and result in the similarity block. The SAD algorithm is the simple parallel computation system which considers all the pixels in the block for computation separately. Hence its implementation is easy and faster due to its parallel computation. It is the most widely used technique in motion estimation and object recognition [5].

The SAD architecture can be implemented in many ways and also in many domains. In [2] the SAD algorithm has been addressed by implementing it on FPGA. In [4], the author modeled SAD architecture using VHDL and utilized for motion estimation system and implemented in FPGA. Similar kind of implementation can be obtained in [5] but in different context while it has been synthesized using Cadence RTL Compiler. MATLAB implementation of SAD algorithm for Visual Landmark detector is implemented in [6].

3. BACKGROUND

Digital Image processing applications like multimedia, surveillance, medical electronics, space exploration and others are dealt with processing of images, frames and videos, in the compressed form. The idea behind the compression is to correlate the data from time domain to frequency domain to reduce the required storage space. Generally image coding algorithm will be used for compression where correlation between the pixels is reduced and then Quantized & entropy coding is followed. Figure 1 show the steps involved in Image Coding Algorithm [7].

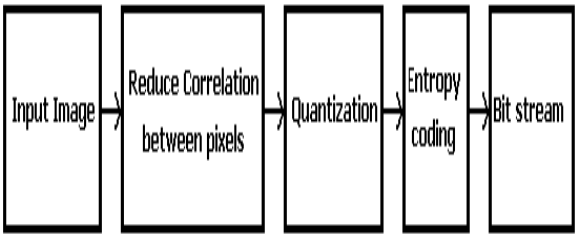

Figure 1: Image Coding Algorithm [7]

But in Videos the frequency domain also needs to be correlated, which is done using Motion Estimation algorithm. Here the best motion part of the image will be searched which is the displacement of the best similar block in the previous block in the current block of frame and replaced [4].

Windowing technique plays an important role in improving the performance of the motion estimation system. In this technique matching is established only on interesting regions in the images or the frames. For instance, only high variation of intensity values in horizontal, vertical and diagonal directions are selected. Choosing the size of the window is critical part in this technique. Once the region is selected, a simple correlation scheme is applied in the matching process.

As mentioned in section I about the advantages of the VLSI hardware implementations; basic building block component - "comparator" of SAD Processor of the Motion estimation system shown in Figure 2 is addressed in this context.

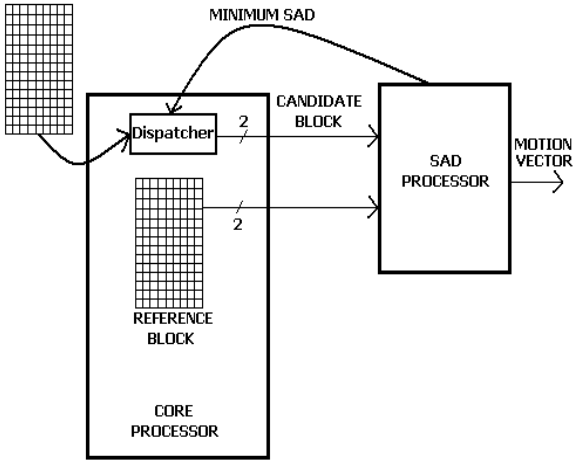

Figure 2: Motion Estimation System [4]

Block diagram of SAD processor is shown in the Figure 3. The main blocks of the SAD processor are Absolute difference, SUM and Comparator blocks.

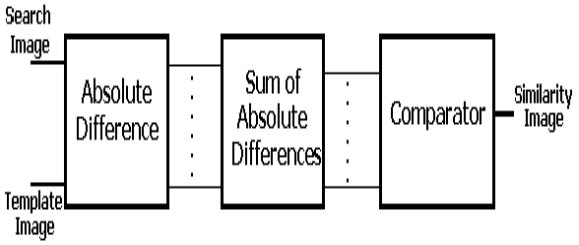

Figure 3: Block diagram of SAD Processor

In SAD processor, the Absolute difference block is used to calculate the absolute differences between the reference pixels of 4X4 block size and the corresponding current input pixel data of 4X4 block size; in the larger search area. 16 Absolute difference units are required for 4X4 block size. The outputs of each absolute difference units of 4X4 block are summed to form the single SAD value, and the process is repeated for next input 4X4 block size with reference pixel of 4X4 block size. The single SAD values of the each 4X4 block size in the search area are compared using comparator for the minimum SAD value. The corresponding 4X4 block sized current input pixel data of the minimum SAD value is considered as the block similar to the reference block against the other SAD blocks. The block size depends on the size of the reference block.

4. ARCHITECTURE

In SAD processor, comparator forms the basic core block. It is used in absolute difference block and in the last stage to find the minimum between the numbers of SAD blocks. In absolute difference block, it is used to compute the smaller number functionality. Regularly implemented comparator architecture is shown in Figure 4.

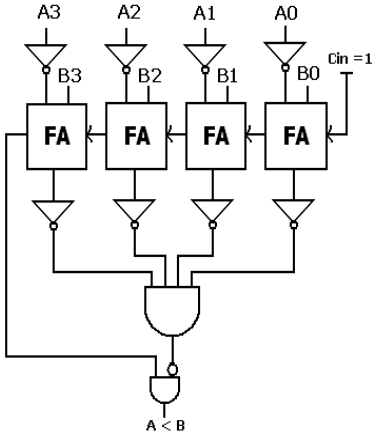

Figure 4: Regular Comparator Architecture [8]

This comparator is used to determine the smaller of the two binary numbers. It computes $\mathbf{B - A = B + \bar{A} + 1}$ to compare the two unsigned binary numbers. Comparator shown in Figure 4 is built using the ripple carry adder and the two's complementor. In Figure 4 for input "Cin" logic '1' is applied to achieve the 2's complement for the subtraction of binary numbers. Design was modeled using Verilog HDL and synthesized using Synopsys Design Compiler. Comparator was built of 4 bit wide and the Design compiler utilizes the standard Full Adder architecture shown in Figure 5 from the library to implement the ripple carry adder based two's complementor.

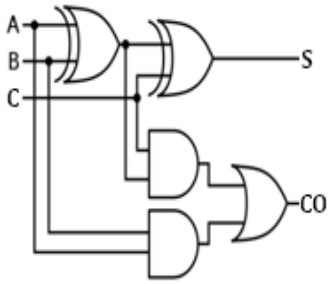

Figure 5: Regular Full Adder Architecture (FA)

TSMC 65 nm Library Standard cells XOR, AND & OR gates are utilized to build the Full adder architecture shown in Figure 5. Here the carry and sum path are not computed parallely and the transistor stacking in these gates are not more two transistor levels, which increases the power consumption of the design. Typically for low power consumption of the designs the transistor stacking levels should be higher. To overcome the high power dissipation, new Full adder architecture with higher transistor stacking levels is proposed. The proposed Full Adder architecture is shown in Figure 6 (a). This architecture computes the sum and carry path parallely which increases the performance of the design. Here the standard cell AO222 is used for the carry path and its transistor stacking is more than (three levels instead of two) the XOR, AND & OR gates. In the Sum path of the Full Adder architecture, the NOR gate based architectures are used as its transistor stack levels are higher. The proposed full adder architecture is designed by considering the Low Leakage power consumption for the device. A similar kind of basic building component level optimization is proposed by the author in [9]. Proposed_1 comparator architecture with proposed full adder is shown in Figure 6(b).

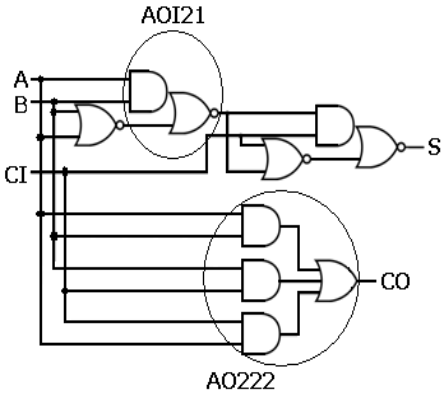

Figure 6 (a): Proposed Full Adder Architecture (FA_P)

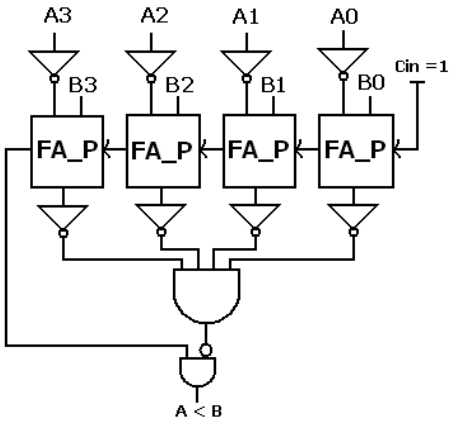

Figure 6 (b): Proposed_1 Comparator Architecture with proposed Full Adder architecture (FA_P)

Transistor stacking is analyzed by the sub-threshold and gate leakage current. In serially connected transistors stack, the gate to source voltage (Vgs) will become negative as the transistor closer to the top stack; and due to the reverse biased body to source voltage; the threshold voltages of top transistors increase. Thus the OFF transistors in the stack leaks less than the single transistor in the stack [10]. For smaller technology nodes the impact of transistor stacking would be larger and is due to the body effect of the transistor. In 32 nm technology the difference in sub-threshold currents between the single transistor in stack and to the double transistors in stack is almost 30 times and reduces the leakage power of the double transistors in stack by about 30% [11].

Other optimizations proposed in this paper are shown in Figure 7. In the proposed_2 comparator architecture, logic optimization techniques are applied at the gate level. Here the input & output inverted AND gate of the regular architecture in Figure 4, is replaced by the OR gate which reduces the number of inverters. This will reduce the area required for the implementation and since area & power are interrelated, lower area will reduce the power consumption of the design.

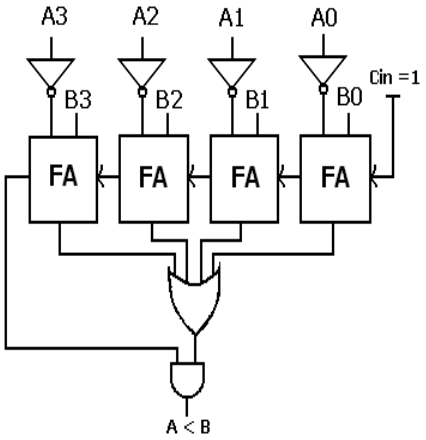

Figure 7 (a): Proposed_2 Comparator Architecture with regular Full Adder architecture (FA) & logic optimizations

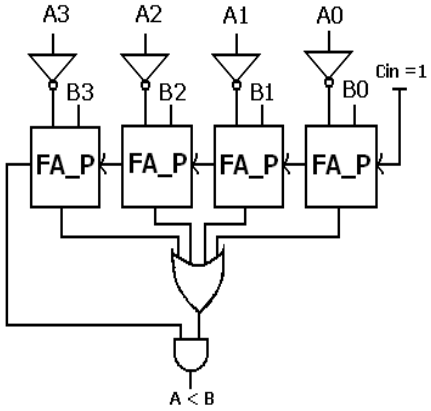

Figure 7 (b): Proposed_3 Comparator Architecture with proposed Full Adder architecture (FA_P) & logic optimizations

Three variations are illustrated in this paper

- 4-bit Comparator with proposed Full adder architecture (Proposed_1).
- 4-bit Regular Comparator architecture with logic optimizations (Proposed_2).
- 4-bit Comparator architecture with proposed Full adder architecture and logic optimizations (Proposed_3).

5. IMPLEMENTATION METHODOLOGY

The proposed and regular comparator architectures of 4 bit wide are designed and modeled using Verilog HDL and verified the functionality with the Mentor graphics Modelsim simulator using Waveform editor. The designs were synthesized using the Design Compiler and mapped to the TSMC 65nm technological library node. Standard ASIC methodology was considered for benchmarking the results.

Figure 8(a), Figure 8(b) and Figure 8(c) shows the Mentor Graphics Model-sim simulators basic steps of simulation flow, typical VLSI flow for synthesis and the Synopsys DC synthesis flow respectively. Modelsim is a simulation and Verification tool for Verilog HDL, VHDL, System Verilog, System C and mixed language designs. Initially working directory is created and all the design files are sourced in to it. Next the Design Units are compiled and simulator is loaded by invoking the top-module of the design. Finally the simulation will be run, and expected results are debugged [13].

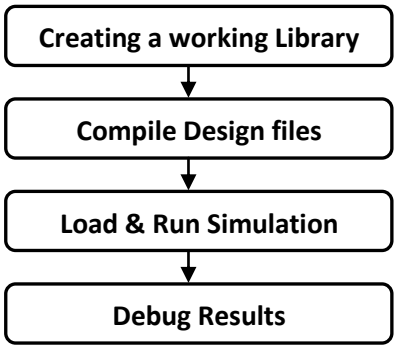

Figure 8 (a): Basic Simulation Flow

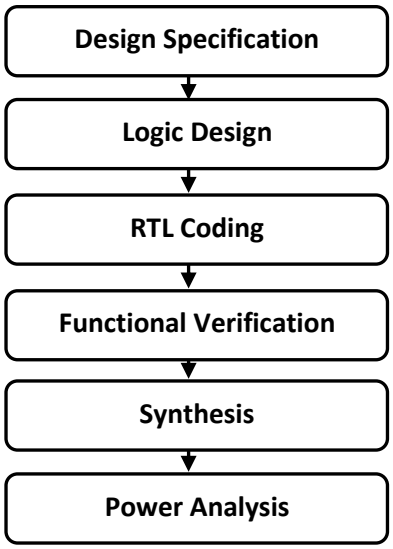

Figure 8 (b): Design & Power Analysis Flow

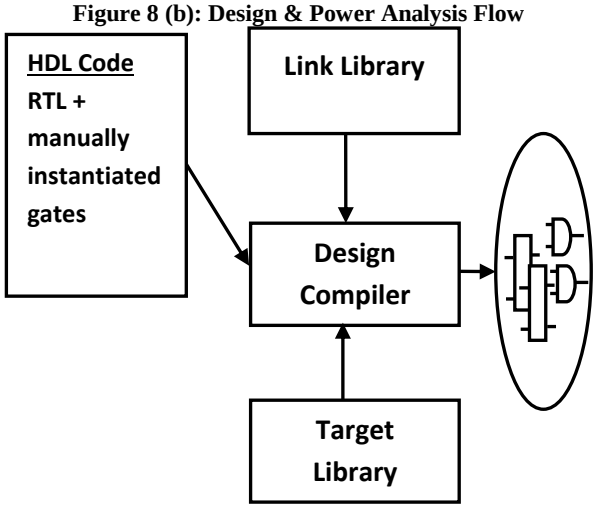

Figure 8 (c): Synopsys DC Synthesis Flow [14]

Synopsys DC synthesis is the complex task which consists of several phases and requires various inputs to arrive at the functionally correct netlists. Synthesis phases are reading the design, setting the constraints, optimizing the design, analyzing the design & saving the design database. In first

phase it reads the input HDL & checks for the syntactical errors and finally translates the HDL objects in to the technology independent design. Setting the constraints means instructing the Design Compiler to behave as per the requirement. The optimization step translates the HDL description into gate-level netlist using the cells available in the technology library. Final phase includes the generation of the results of the synthesized design [12 - 15].

6. RESULTS & DISCUSSION

The core component "Comparator" in SAD processor of the motion estimation system is implemented in this paper. The results of the regular and proposed 4 bit comparator architectures are tabulated in Table I. The proposed architectures were designed for low power consumption and the impact of the basic building component in the block level is addressed in this paper. Functional waveform of 4-bit wide Comparator with "smallest of two binary numbers" is shown in Figure 9. DC synthesized gate level schematics of the regular and proposed architectures are shown in Figure 10. The Full adder cell impact in the comparator architecture can be observed from the proposed_1 architecture column in Table I.

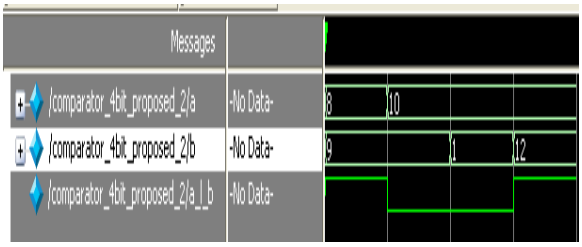

Figure 9: Proposed_2 comparator's functional waveform

The transistor stacking concept has reduced the leakage power of the proposed_1 architecture against the regular comparator architecture. It has reduced 36.61 % of leakage power against its counterpart architecture. Similarly proposed_2 architecture result suggests that efficiently optimized architectures also impact the quality metrics of the design. Here it reduces the leakage power by 7.27 %. Proposed_3 architecture has the combination of the first two optimizations. This has reduced the leakage power by 43.74 %.

From the proposed architecture's results in Table I, it can be observed that different quality metrics are better in different optimizations. This enables the choices for the architectures as per the applications .i.e., the architectures can be chosen as per the design constraints of the applications. The design constraints may be like low power - low performance, low power – relaxed performance, low area – low power, low area – low power – high performance and etc.

7. CONCLUSION

The basic building block component "Comparator" of SAD processor of Motion Estimation for Video compression is implemented. The impact of cell level computational logic at the block level is addressed by incorporating the Full adder in the comparator is addressed in this paper. The transistor stacking concept in the proposed architecture has reduced the leakage power by a significant amount (7- 43 %). The designs were modeled with the Verilog HDL and used 65nm technological library node for the synthesis in Design compiler tool. It can be observed that the proposed architectures are more power efficient than the counterpart regular architecture and enables the architectures to be analyzed with different corners of design constraints. The impact of Full adder at the comparator level proves that the power aware architectures at the component level can impact largely at the system level and can be carried over any level of abstractions as per the application requirement.

Table I: Results of the regular and proposed 4-bit Comparator Architectures

	Column I	Column II		Column III		Column IV	
Architecture	**Existing**	**Proposed_1**	**% gain**	**Proposed_2**	**% gain**	**Proposed_3**	**% gain**
Area	56.16	61.92	-10.26	50.76	9.62	56.52	-0.64
Timing	0.57	0.80	-40.35	0.50	12.28	0.73	-28.07
Dp	11.38	9.09	20.11	10.23	10.09	7.95	30.16
Lp	0.74	0.47	36.61	0.69	7.27	0.42	43.74
Tp	12.12	9.56	21.12	10.92	9.92	8.36	30.99

Note: Area in Square microns; Timing in nano seconds; Dp = Dynamic power in micro watt; Lp = Cell Leakage power in micro watt; Tp = Total power in micro watt

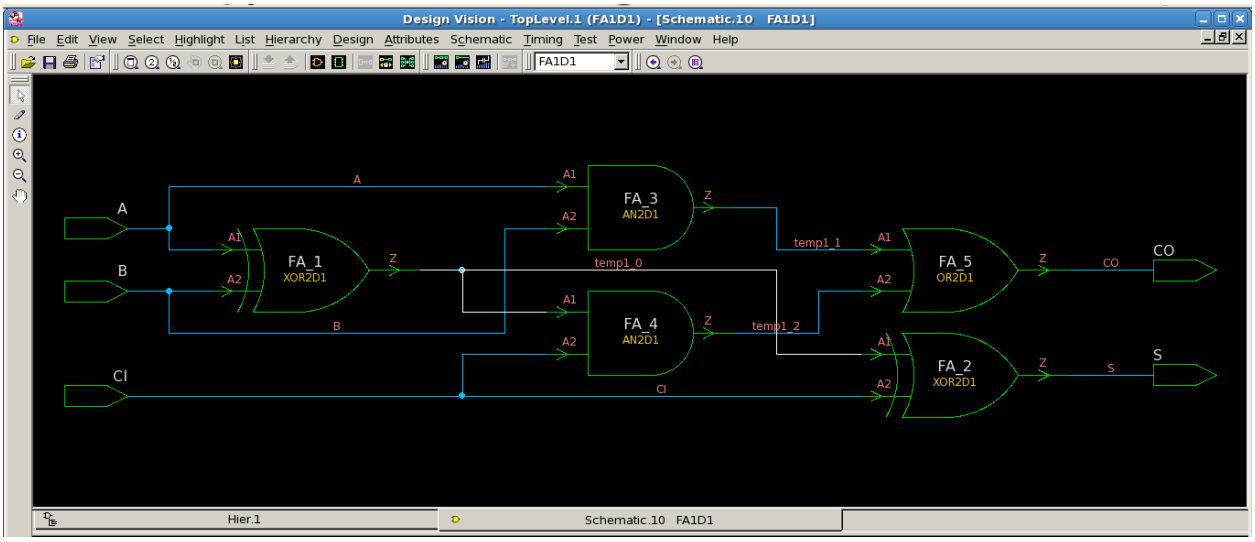

Figure 10 (a): Schematic of regular Full Adder Architecture

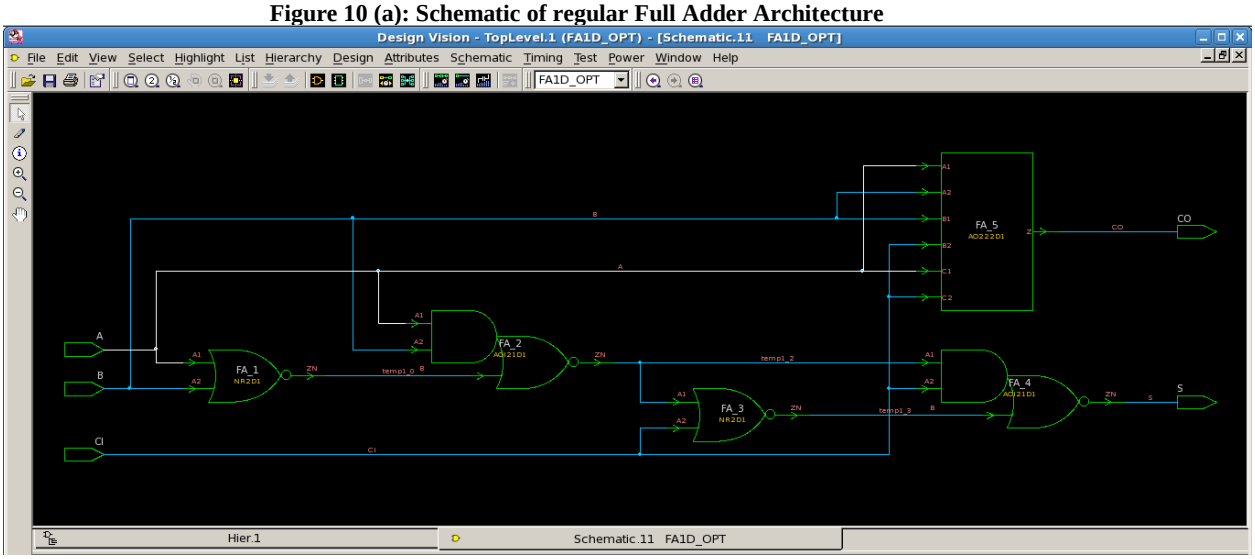

Figure 10 (b): Schematic of proposed Full Adder Architecture

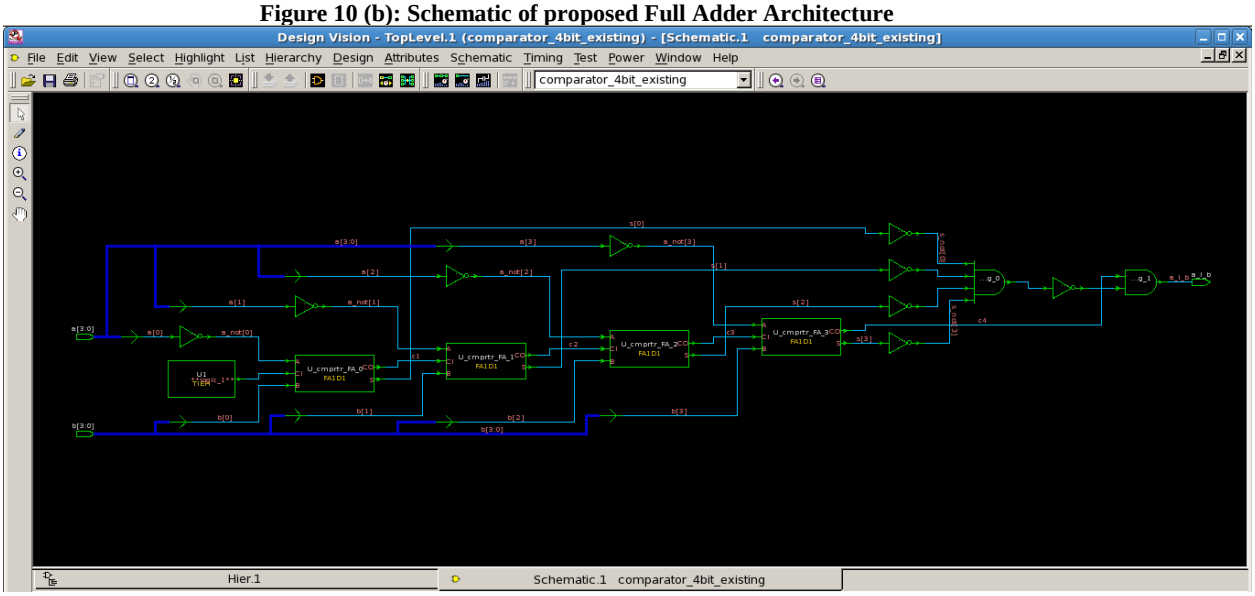

Figure 10 (c): Schematic of regular 4-bit comparator architecture

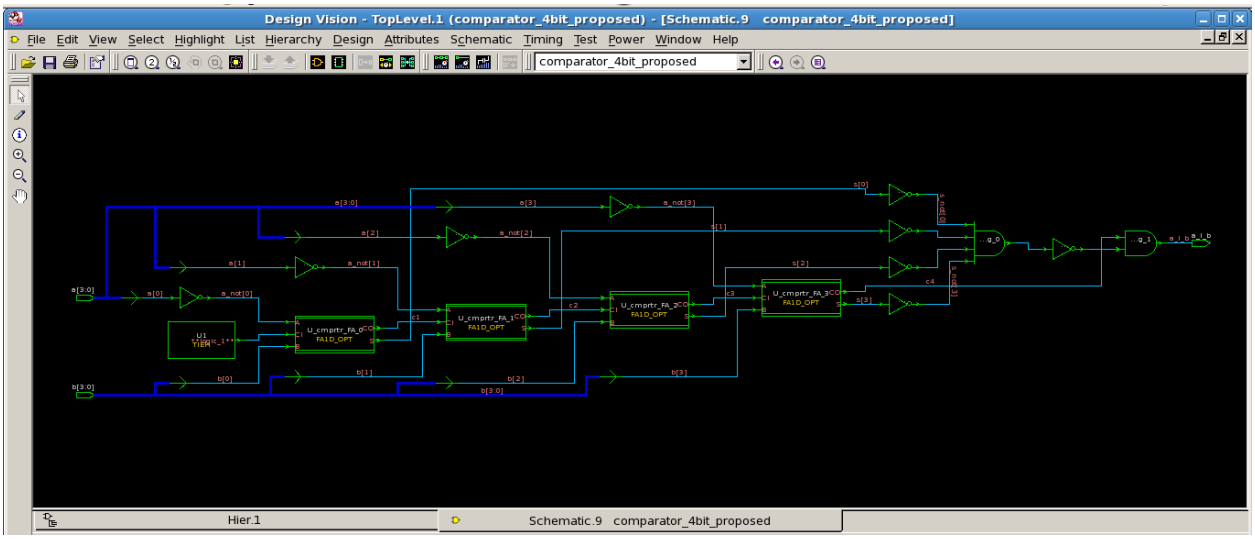

Figure 10 (d): Schematic of proposed_1 4-bit comparator architecture

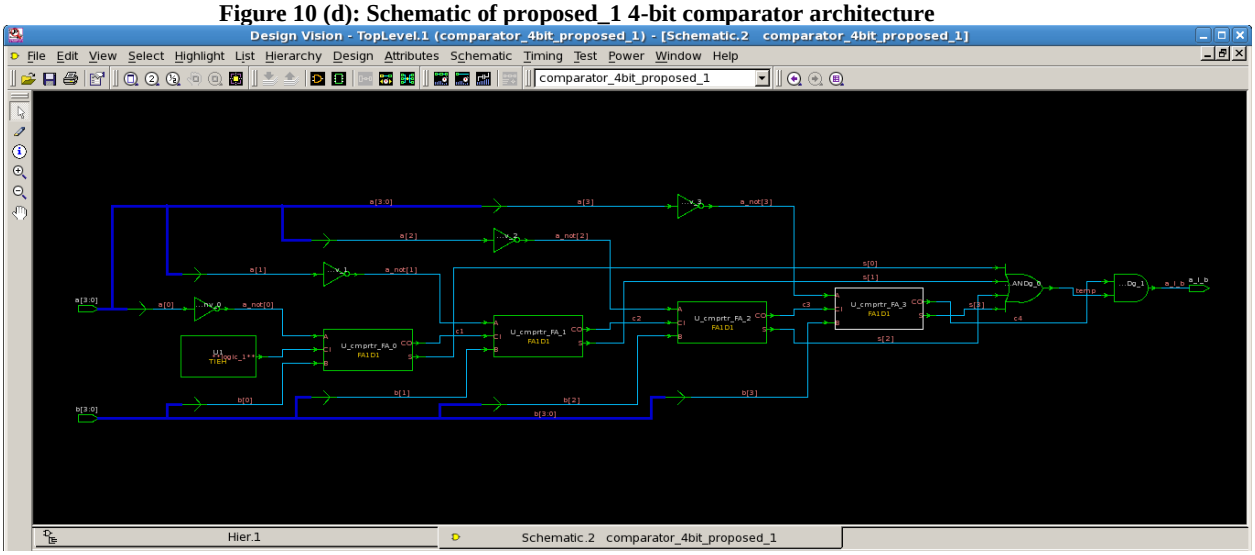

Figure 10 (e): Schematic of proposed_2 4-bit comparator architecture

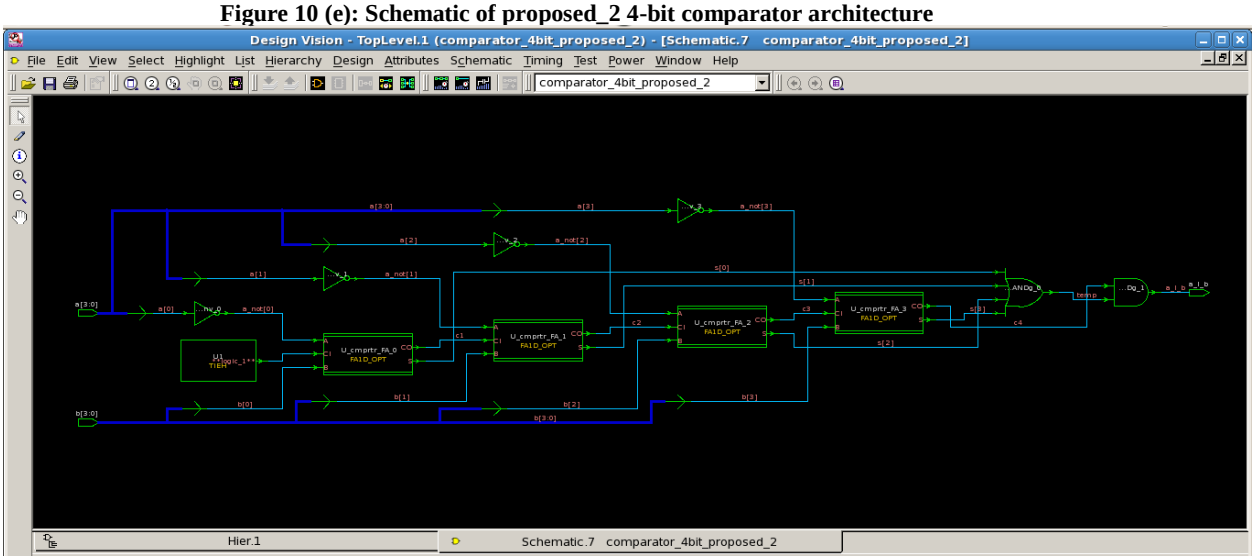

Figure 10 (f): Schematic of proposed_3 4-bit comparator architecture

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9. AUTHOR'S PROFILE

Mr. Narendra C. P is Assistant Professor in the Department of Electronics and communication Engineering, Bangalore Institute of Technology, Bangalore. Obtained B.E. degree in Instrumentation and Electronics from Bangalore University. The specialization in Master degree was Digital Electronics and Communication from NMAMIT, Nitte, Visvesvaraya Technological University (VTU), Belgaum, Karnataka and published 2 papers and currently pursuing Ph.D. under the guidance of Dr. K.M. Ravi Kumar ,Professor and PG Coordinator, VTU-Regional office, Mysore Regional Centre, Mysore –Karnataka. His research interests include Digital Signal Processing, Digital Image Processing and VLSI Signal Processing.

Dr. K.M. Ravi Kumar is Professor and PG Coordinator, VTU-Regional office, Mysore Regional Centre; Mysore .He obtained his Bachelor of Engineering in Electronics and Communication from Bangalore University and Master of Technology in Biomedical Instrumentation, SJCE, Mysore. He was awarded Ph.D. in Digital Signal Processing from NMIT, Bangalore, Visvesvaraya Technological University (VTU). He has over 18 research publications in refereed International Journals and Conference Proceedings. His research interests include Digital Signal Processing, Speech Signal Processing, Adaptive Signal Processing, Image Processing, VLSI Signal processing, and Communication networks.