Design of Soft Switching Sepic Converter Fed DC Drive Applications

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ABSTRACT
High efficiency DC-DC converters with high-voltage gain have been researched due to increasing demands. A soft-switching single-ended primary inductor converter (SEPIC) is presented in this work. An auxiliary switch and a clamp capacitor are presented in this project. A coupled inductor and an auxiliary inductor are utilized to obtain ripple-free input current and achieve zero voltage-switching (ZVS) operation of the main and auxiliary switches. The voltage multiplier technique and active clamp technique are applied to the conventional SEPIC converter to increase the voltage gain, reduce the voltage stresses of the power switches and diode. Moreover, by utilizing the resonance between the resonant inductor and the capacitor in the voltage multiplier circuit, the zero-current-switching (ZVS) operation of the output diode is achieved and its reverse-recovery loss is significantly reduced. The converter achieves high efficiency due to soft switching commutation of the power semiconductor device. The circuit is simulated using MATLAB Simulink and output result is verified.

Keywords
Sepic converter, DC drive,

1. INTRODUCTION
SEPIC converters have been adopted for many applications such as power factor correction, photovoltaic system and LED lighting. However, it has several drawbacks. Its two major drawbacks are high voltage stresses of power semiconductor devices and low efficiency due to hard switching operation of the power switches. Especially in high voltage applications, higher voltage rated power semiconductor devices should be used. When the voltage rating is higher, the *Rds*(on) of power MOSFET is higher. So, it causes higher conduction loss at the same current level. Therefore, if the voltage stress is reduced at the same current level, the overall efficiency can be Improved. To reduce the voltage stress and increase the voltage gain,
Voltage multiplier techniques are proposed. In order to reduce the volume and weight of the converter, soft-switching techniques such as zero-voltage switching (ZVS) and zero-current-switching (ZCS) are necessary. High frequency operation of dc-dc converters allows reduction of the volume and weight of their magnetic components. However, switching losses and electromagnetic interference noises are significant in high frequency operation. Therefore, various soft-switching techniques have been introduced. Among them, the active clamp technique is often used to limit the voltage spike effectively, achieve soft-switching operation, and increase the system efficiency.
SEPIC converters can have a low input current ripple, which is one of the advantages of SEPIC converters. However, a bulk inductor should be used to minimize the current ripple. Input current ripple becomes one of important requirements due to the wide use of low voltage sources such as batteries, super capacitors, and fuels cells. It is because large ripple current may shorten the lifetimes of those input sources [22]-[24]. In [25], a ZCS PWM SEPIC converter was proposed. Two switches can operate with soft switching. However, three power diodes and three separate inductors are utilized.
The voltage stress of the power switches is the sum of the input voltage and the output voltage which is equal to that in the conventional SEPIC converter. In [26], a resonant step up/down converter was proposed. Sort-switching operation is achieved.
Two power switches and two magnetic components are required. However, it has a pulsating input current and an additional filter stage is requires in the input stage to suppress the input current ripple. Therefore, the number of magnetic components can be increased. Bidirectional ZVS PWM SEPIC/ZETA converter was proposed. Two main switches can operate with soft switching. However, a bidirectional switch consisting of two power MOSFETs is required. Many switches are required and also complex driving circuits for them are required. Moreover, the voltage stress of the switches is equal to that in the conventional SEPIC converter. In addition, a snubber circuit is required to suppress the parasitic voltage ringing across the bidirectional switches.
A soft-switching SEPIC converter with ripple-free input current is proposed. An auxiliary switch and a clamp capacitor are added to the conventional SEPIC converter. A coupled inductor and an auxiliary inductor are utilized to obtain ripple-free input current and achieve ZVS operation of the main and auxiliary switches. The voltage stresses of the power switches and diode are reduced by half by utilizing the voltage multiplier technique. Moreover, the reverse-recovery loss of the output diode is significantly reduced due to the resonance between the resonant inductor and the capacitor in the multiplier circuit. The proposed converter achieves high efficiency due to soft-switching characteristics of power semiconductor devices. The theoretical analysis is verified by an 80-W by simulation of prototype with 48-200V conversion.

2. DESIGN ANALYSIS
The conventional SEPIC converters are shown in Fig 1. The separate inductor version is shown in fig 1 and the coupled inductor version is shown in fig .2. In the coupled inductor version, loosely coupled inductor Lc is used instead of two separate inductors L1 and L2. L1k1 and L2k2 imply the leakage inductances of the coupled inductor. The coupled inductor version has advantages such as single magnetic component and a ripple free input current.
The ripple free condition is related with the magnetizing inductance, the turn ratio, and the leakage inductance Lk 2 of the coupled inductor. However, the leakage inductance is hard to control in mass production. Fortunately, the leakage inductance Lk 1 is not related with the ripple free condition. Therefore, a tightly coupled inductor can be used with an additional inductor La instead of Lk 2 as shown in Fig 3.

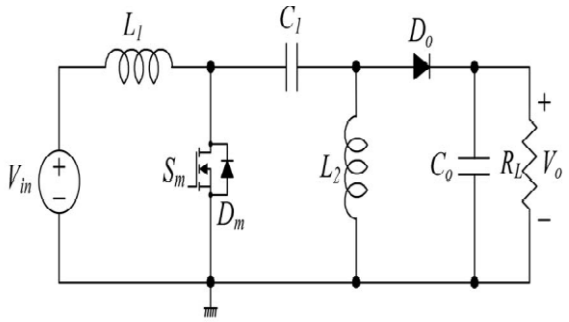

Fig 1 conventional SEPIC converter

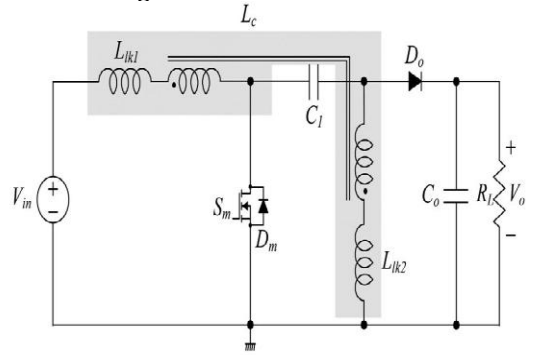

Fig.2nripple free SEPIC converter with lossel coupled inductor

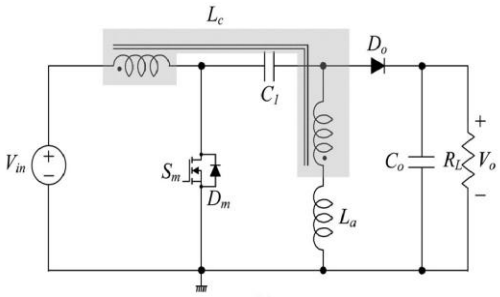

Fig 3 ripple free SEPIC converter with tight

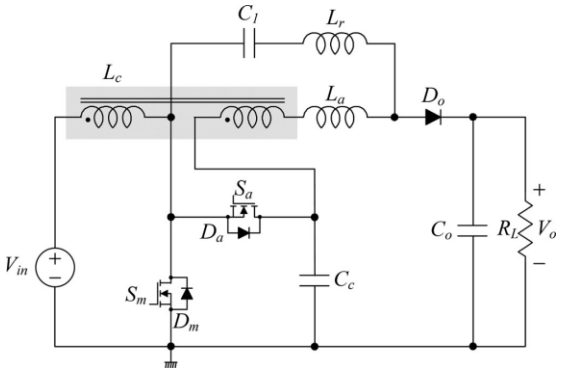

Fig 4. proposed soft switching SEPIC

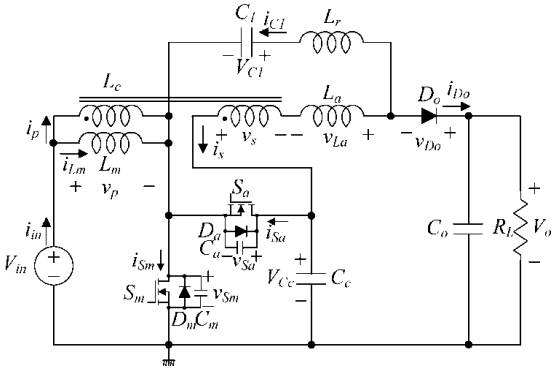

Fig 5 equalent proposed soft switching SEPIC converter

The circuit diagram of the proposed soft-switching SEPIC converter with a ripple free input current is shown in fig.4. In the proposed converter, the resonant inductor *Lr* and the active clamp cell consisting of the auxillary switch Sa and the clamp capacitor Cc are added to the conventional SEPIC converter shown in Fig 4. The equivalent circuit of the proposed converter is shown in Fig.5. The coupled inductor *Lc* is modeled as the magnetizing inductance Lm and an ideal transformer with a turn ratio of 1:n.Coupled inductor

The diodes *Da* and *Dm* are the intrinsic body diodes of the auxiliary switch Sa and the main switch *Sm*. The capacitors *Ca* and Cm are their parasitic output capacitances. Key waveforms of the proposed converter are shown in Fig.4.

The switches *Sa* and *Sm* are operated asymmetrically and the duty ratio Dis based on the main switch Sm. The operation of the proposed converter in one switching period its can be divided into five modes as shown fig . to simplify the steady state analysis, it is assumed that those capacitors C1, Cc and Co have large values and the voltage ripples across them can be ignored.

3. MODES OF OPERATION

3.1 Mode 1

At t0, the auxiliary switch Sa is turned OFF. Then, the energy stored in the magnetic components such as Lm, Lr, and La starts to charge Ca and discharge Cm. Therefore, the voltage vSa across the auxiliary switch Sa starts to rise from zero and the voltage vSm across the main switch Sm starts to fall from VCc. Since the capacitors Ca and Cm are very small, the transition time interval Tt1 is very short and it can be simplified as follows.

$$Tt1 = \frac{(Ca + Cm)VCc}{(1-n)ILa1 - ILm2} \qquad (1)$$

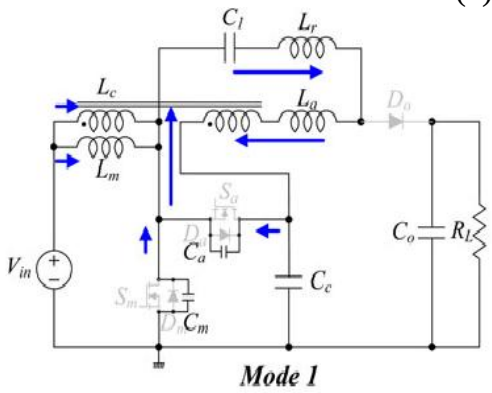

Fig 6. Mode1 operation

3.2 Mode 2

At [t1, t2]: At t1, the voltage vSm arrives at zero. Then, the body diode Dm is turned ON. After that, the gate signal is applied to the switch Sm and the channel of Sm takes over the current flowing through Dm. Since the voltage vSm is clamped as zero with turn on of Dm before the switch Sm is truned ON, zero voltage turn on of Sm is achieved. In this mode, the input voltage Vin is applied to Lm and the current iLm increases linearly from its maximum value ILm2 as follows.

iLm (t) =ILm2+Vin/Lm(t-t1) (2)

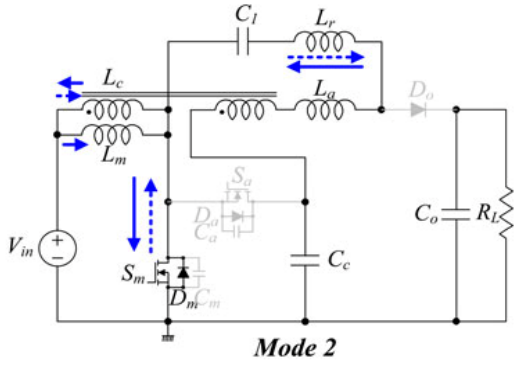

Fig.7 mode2 operation

Since the voltage vs at the secondary side of the coupled inductor Lc is nVin, the voltage vLa across La is –(VCc-nVin-VC1) La / (La=Lr). Therefore, the secondary current is decreases linearly from its maximum value ILa1 as follow.

$$is(t) = ILa1 - \frac{VCc - nVin - Vc1}{La + Lr}(t - t1) \quad (3)$$

The input current I in is the sum of ip and *iLm* and given by

$$Iin(t) = iLm(t) + ip(t) = ILm2 + nILa1 + \left[\frac{Vin}{Lin} - \frac{n(VCc - nVin - Vc1}{La + Lr}\right](t - t1) \quad (4)$$

The main switch current i*Sm* in this mode can be derived by

$$ism(t) = iLm(t) - (1-n)is(t)$$
$$= -[(1-n)ILa1 - ILm2] + \left[\frac{Vin}{Lm} + \frac{(1-n)(VCc - nVin - Vc1)}{La + Lr}\right](t - t1) \quad (5)$$

3.2 Mode 2

At [t2, t3]: The main switch *Sm* is turned OFF at t2. Then, the voltage *vSm* increases from zero and the voltage *vSa* decreases from *VCc* at the same time due to the energy stored in the magnetic components. With the same assumption as in model, the transition time interval *Tt 2* can be simplified as follows.

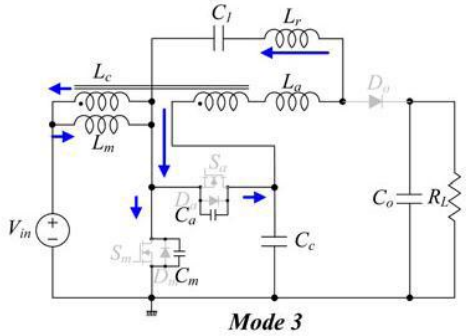

Fig 8 mode 3 operation

$$Tt_2 = \frac{(Ca+Cm)VCc}{ILm1 - (1-n)ILa_2} \quad (6)$$

3.3 Mode 3

At [t3, t4]: At t3, the voltage vSa arrives at zero. Then, the body diode Da is turned ON. After that, the gate signal is applied to the switch Sa and the channel of Sa takes over the current flowing through Da. Since the voltage vSa is clamped as zero before the switch Sa is turned ON, zero-voltage turn on of Sa is achieved. In this mode, the voltage vp across Lm is –(VCc-Vin) and the current iLm decreases linearly from its maximum value ILm1 as follows.

$$iLm(t) = ILm1 - \frac{VCc - Vin}{Lm}(t - t3) \quad (7)$$

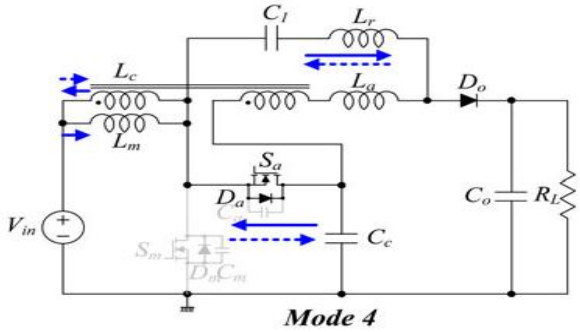

Fig.9 mode 4 operation

With the turn on of Sa, the output diode Do starts to conduct. Then the resonance between the resonant inductor Lr and the capacitor C1 occurs. Since the voltage across the inductor La is Vo+nVin-(1+n) Vcc, the current is increases linearly in this mode as follows.

$$is(t) = ILa2 + \frac{Vo + nVin - (1+n)VCc}{La}(t - t3) \quad (8)$$

The current *iC1* is given by

$$ic1(t) = \frac{Vo - Vc1 - VCc}{Zr}\sin\omega r(t - t3) - ILa2\cos\omega r(t - t3) \quad (9)$$

Where the resonant frequency ωr and the impedance Z of the resonant tank are

$$\omega r = \frac{1}{\sqrt{LrC1}} \quad (10)$$

$$Zr = \frac{1}{\sqrt{\frac{Lr}{C1}}} \quad (11)$$

In this mode, the output diode current *iDo* and the switch current iS1 can be written by

$$iDo(t) = -is(t) - iC1(t) \quad (12)$$

$$isa(t) = -iin(t) - iC1(t) \quad (13)$$

3.4 Mode 4

At [t4, t5]: At t4, the output diode current iDo decreases to zero and the zero current turn OFF of the diode Do is achieved. Since the current changing rate of Do is controlled by a resonant manner, its reverse recovery problem is significantly alleviated. Since the voltage across the inductor La is (VC 1 – nVCc+nVin) La / (La+Lr), the current is increases linearly in this mode as follows.

$$is(t) = is(t4) + \frac{Vc1 - nVCc + nVin}{La + Lr}(t - t4) \quad (14)$$

At the end of this mode, iLm arrives at its minimum values ILm2 and maximum value ILa1

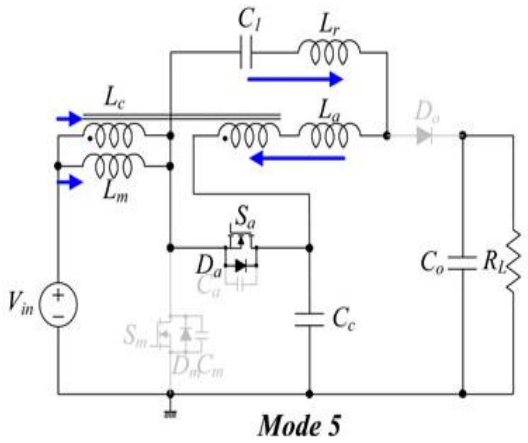

Fig.10 mode 10 operation

4. DESIGN PARAMETER

4.1 VCc and VC1:

Since the average voltage across *LM should* be zero under study state, the clamp capacitor voltage *VCc* is obtained by

$$VCc = \frac{Vin}{1 - D} \quad (15)$$

Also, the average voltages across the inductors *Lr* and *La* should be zero. Therefore, the voltage *VC* 1 is obtained by

$$Vc1 = VCc - Vin = \frac{D}{1 - D}Vin \quad (16)$$

4.2 Voltage Gain:

By applying the volt-second balance law to the voltage across the inductor *La* , the following relation is obtained.

$$-\frac{La}{La+Lr}(VCc - nVin - Vc1)DTs + (Vo - VCc - n(VCc - Vin))d2Ts + \frac{La}{La+Lr}(VC1 - n(VCc - Vin))(1 - D - d2)T2 = 0 \quad (17)$$

From (15) to (17), the voltage gain *M* of the proposed converter Can be obtained by

$$M = \frac{Vo}{Vin} = \frac{1}{1-D}\left(1 + nD + \frac{(1-n)DLa}{La+Lr}\right) \approx \frac{1+D}{1-D} \quad (18)$$

The voltage gain of (18) is plotted and compared with other Converters in Fig. 11.

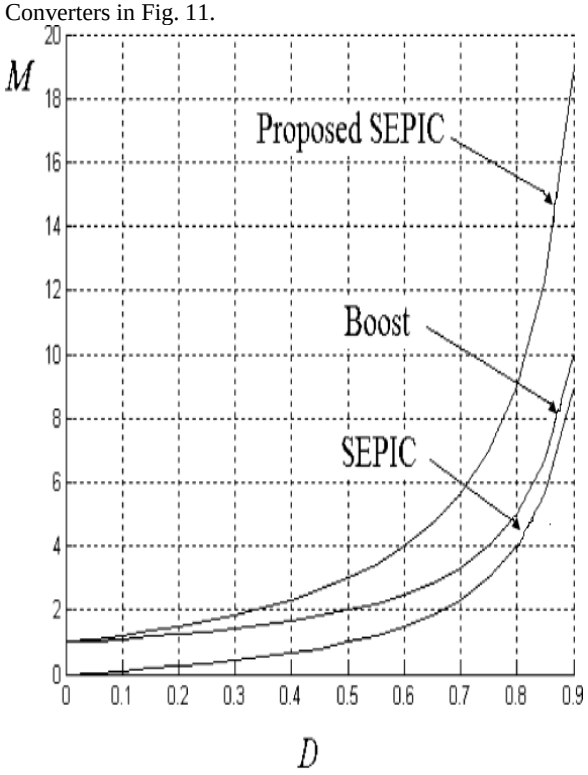

Fig.11 plot for gain

4.3 Input Current Ripple:

In mode 2, the input current *i*in is given by (3). From (15) and (16), the ripple component of *i*in can be removed by satisfying the following condition

$$La + Lr + n(1-n)Lm \quad (19)$$

Under the condition of (19), the input current *i*in is constant as *ILm*2 + *nILa*1 . In mode 4, the input current *i*in is given by (8). Similarly, from (15), (16), and (18), its ripple component can be removed by satisfying the same condition of (19). In this mode, the input current *i*in is constant as *ILm*1 + *nILa*2. From (18), it can be seen that the inductor current *ILA* has the same slope both in mode 4 and 5. Therefore, the input current *i*in does not change in mode 5.

From (1), *ILm*1−*ILm*2 is obtained by

$$ILm1 - Ilm2 = \frac{Vin}{Lm}DTs \quad (20)$$

Similarly, *ILa*1−*ILa*2 is obtained from (2) as follows.

$$ILa1 - ILa2 = \frac{VCc - nVin - VC1}{La + Lr}DTs \quad (21)$$

With the condition of (19), the following relation can be easily derived from (15), (16), (20), and (21)

$$ILm2 + nILa1 = ILm1 + nILa2 \quad (22)$$

Therefore, the ripple component of the input current *i*in can be removed under the condition of (19).

4.4 Minimum and Maximum Values of ILm:

is = *IC* 1 + *iDo*. Since the average capacitor current should be zero under a steady state, the average value *IC* 1, avg of the capacitor current *IC* 1 is zero. And the average output diode current *iDo*, avg is equal to the average output current Io. Therefore, the following relation can be obtained from the waveform of the secondary current *is* in

$$ILa1 + ILa2 = -2Io \tag{23}$$

From (15), (16), (19), (21), and (23), the maximum and minimum values of *is* are derived by

$$ILa1 = \frac{(1-n)VinDTs}{2(La+Lr)} - Io \tag{24}$$

$$ILa2 = \frac{(1-n)VinDTs}{2(La+Lr)} - Io \tag{25}$$

Similarly, from Fig. 3, the input current *i*in is the sum of *ip* and *iLm*. Since the average current *is*, avg is−*Io*, the average primary current *ip*, *avg* is equal to−*nIo*. Therefore, the following relation can be obtained from the waveform of the magnetizing current *iLm* in Fig. 4.

$$ILm1 + ILm2 = 2\left(\frac{Po}{nVin} + nIo\right) \tag{26}$$

Where
η is the efficiency
Po is the output power.
From (21) and (27), the maximum and minimum values of *iLm* are derived by

$$ILm1 = \frac{Po}{nVin} + nIo + \frac{VinDTs}{2Lm} \tag{27}$$

$$ILm2 = \frac{Po}{nVin} + nIo - \frac{VinDTs}{2Lm} \tag{28}$$

4.5 ZVS Conidition:

From Fig. 4, the ZVS condition for Sa is given by

$$ILm1 - (1-n)ILa2 > 0 \tag{29}$$

Since *ILm*1 is always positive from (28) and *ILa*2 is always negative from (26) for *n* < 1, the condition of (30) is always satisfied for *n* < 1. Therefore, the ZVS of *Sa* is always achieved. Similarly, for the ZVS of *Sm*, the following condition should be satisfied

$$-ILm2 + (1-n)ILa2 > 0 \tag{30}$$

From (19) and (29) the inequality (30) is rewritten by

$$Lm < \frac{VinDTs}{2n\left(\frac{M}{n}+1\right)Io} \tag{32}$$

4.6 ZCS Condition:

From (8), (10), and (13), the output diode current reset timing ratio *d*2 can be obtained by solving the following equation

$$-ILa2 - \frac{Vo + nVin - (1+n)VCc}{La} d2Ts - \frac{Vo - Vc1 - VCc}{Zr} \sin \omega r d2T + ILa2 \cos \omega r d2Ts = 0 \tag{33}$$

To obtain ZCS of the output diode, the following condition should be satisfied

$$d2 < 1 - D \tag{34}$$

4.7 Voltage Stresses of the Power Switches and Output Diode:

From Fig. 2, it can be seen that the voltages across the main and auxiliary switches are confined to the clamp capacitor voltage *VCc*. By using (16) and (19), the voltage *VCc* can be rewritten as (*V*in+*Vo)*/2. Since the voltage stress of the power semiconductor devices in the conventional SEPIC converters shown in Fig. 1 is *V*in + *Vo*, the voltage stress in the proposed converter is reduced by half. In the proposed converter, the voltage stress of the output diode is also reduced by half. In mode 2, the voltage *VLA* is − (*VCc*−*nV*in−*VC* 1) La / (*La*+*Lr)*. Therefore, the maximum voltage *vDo*, max across the output diode is given by

$$vDo,max = Vo + \frac{(1-n)VinLa}{La+Lr} + nVin - VCc \tag{35}$$

For *La* >> *Lr*, it can be easily seen that *vDo*, max is (*V*in+*Vo)*/2, which is half of that in the conventional SEPIC converters.

5 .EXPERIMENTAL RESULTS

To verify the steady-state performance and the theoretical analysis of the proposed soft-switching SEPIC converter with ripple-free input current, a laboratory prototype is implemented and tested with the following specification. 1) Input voltage *V*in = 48V. 2) Output voltage *Vo* = 200V. 3) Switching frequency *fs* = 100 kHz. 4) Output power *Po* = 80W. The control circuit was implemented with a constant frequency pulse width modulation controller KA7552 from Fairchild. The required voltage gain *M* is 4.17. From (19), the duty cycle *D* is calculated as 0.613. The turn ratio *n* of the coupled inductor is selected as 0.25. The ZVS condition

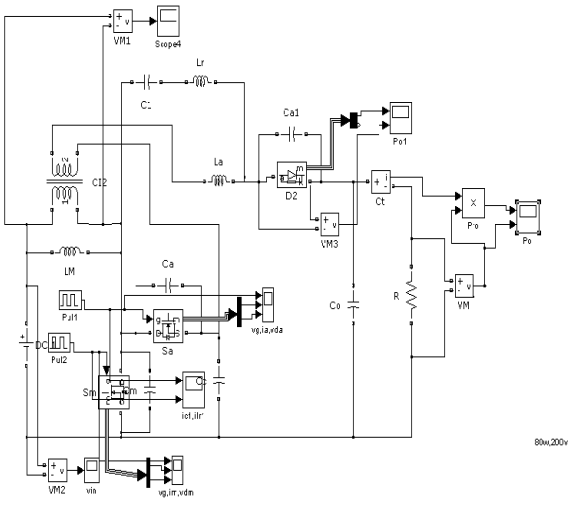

Fig.12 SEPIC using MAT LAB model

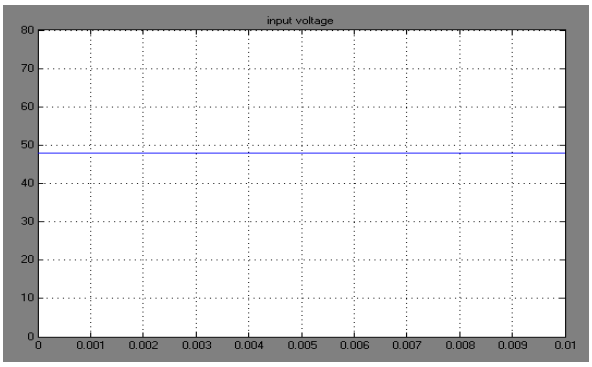

Fig 13.input DC Voltage

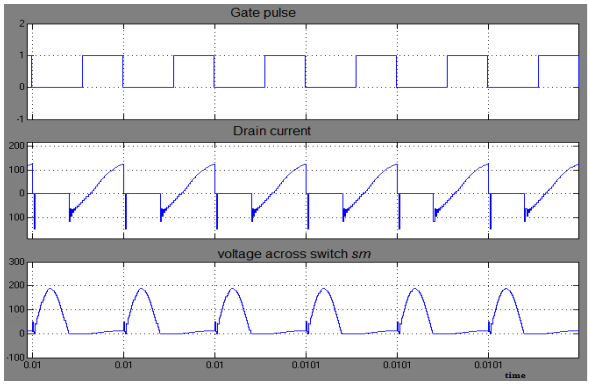

Fig.14. voltage across switch sm

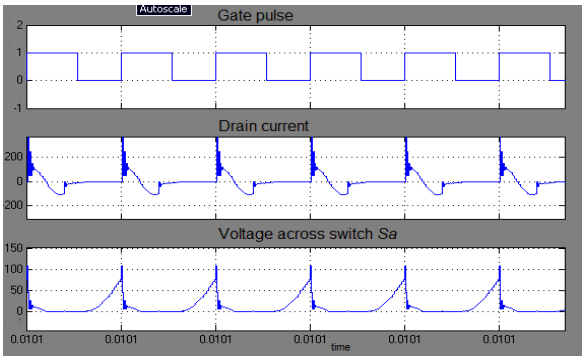

Fig.15 voltage across switch sa

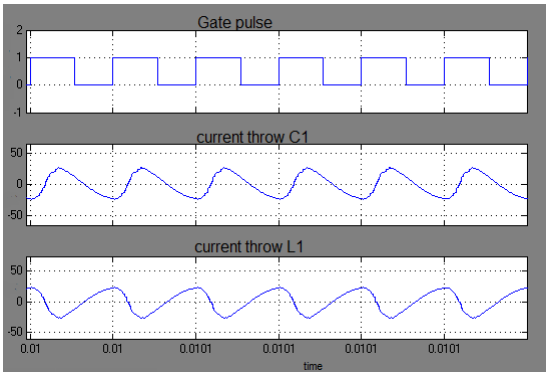

Fig 16 current throw C1 and Lr

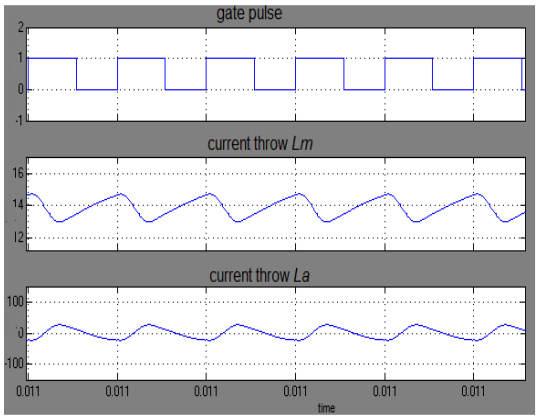

Fig 17 .magnetising inductance Lm and current throw La

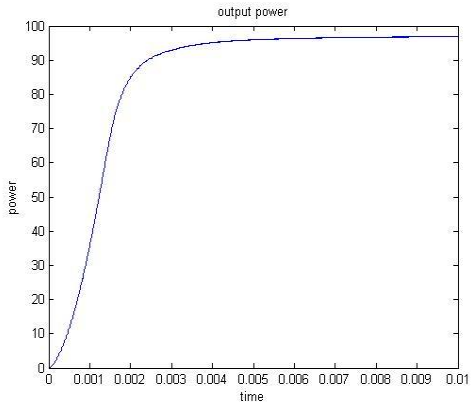

Fig 18. Output power

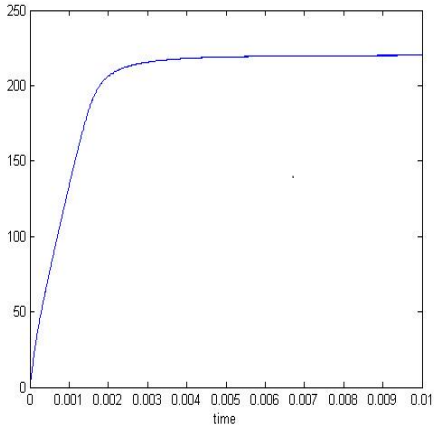

Fig 19.input power

6. CONCLUSION

The operation principle, theoretical analysis, and the implementation of a soft-switching SEPIC converter with ripple-free input current are presented in this paper. In the proposed converter, the coupled inductor with an auxiliary inductor is used to provide ripple-free input current and achieve ZVS operation of main and auxiliary switches. The advantages of the proposed converter are low voltage stresses, low switching losses, ripple free input current, alleviated reverse-recovery problem of the output diode, and high efficiency. The design consideration of the proposed converter is included. The experimental results based on a prototype are presented for validation.

7. REFERENCES

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