Reconfigurable CPL Adiabatic Gated Logic –RCPLAG based Universal NAND/NOR Gate

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ABSTRACT
In precursory efforts authors have illustriously consolidated the benefits of CPL based circuits and adiabatic logic conjoint the use of clock for even combinational blocks and reported the power diminution. With the adhibition of clock in combinational blocks, the same circuit topology may be employed for sequential behavior as manifested by authors in their erstwhile works. Proceeding forward in the same direction and augmenting another edge into this, authors have reported the reconfigurable circuit implementation utilizing the reported CPLAG concepts. In pursuance of the same authors have contemplated and implemented reconfigurable 'Nand' and 'Nor' gates. The same circuit topology can be used for either functionality governed by a control signal. The functional behavior of the circuit realized for 'Nand' and 'Nor' are analyzed and found to be cogent. The power results shows improvement by 4-5% as compared to SCMOS based circuits. The proposed RCPLAG universal gate is investigated for different voltage levels and transistor size. The parameters like power dissipation, power fed back to system, T_{rise}, T_{fall}, propagation delays, PDP are further examined and found to be satisfactory. The best operating conditions for the said circuit lies in voltage range of less than 2.5V. The P_{avg} at 1V, 180nm technology is 12.2nW with 36f units PDP, 5µs maximum delay.

General Terms
Low Power, VLSI Design, CPL, Adiabatic Logic. Power delay product, fully adiabatic logic, semi adiabatic logic

Keywords
CPLAG, RCPLAG, Nand, Nor, universal gate

1. INTRODUCTION
There is convincing alteration in the VLSI design approach since last decade. Previously major focus was given to operating speed of the circuit which used to be center of all optimization algorithms. On contrast, now power used to be the center point of optimization. This shift in design approach is obvious because of market needs, social obligations, and also political and governmental policies to some extent which forces the researchers, engineers globally to implement the desired day old functionalities on power aware circuits maintaining the performance parameters and integration advantages. Globally researchers are approaching limitations in the traditional design techniques to implement low power circuits, which encourage several intellectuals to utilize the concepts from other science/ technologies in VLSI design domain to lower down the power equations. Adiabatic logic is one such design approach well proposed around 10-15 years earlier. Due to speed limitations adiabatic logic was not commercially exploited then but now many organizations like "Adiabatic Logic- UK" [16] are commercially bringing solutions and IPs in market. Also as power equations are becoming most critical design parameter with advances in integration and fabrication technologies well appreciated by market demand adiabatic based circuit are well providing competitions to different low power design technologies both traditional and modern approaches. Adiabatic logic circuits are broadly classified as semi adiabatic and full adiabatic circuits. Partial adiabatic family circuits dissipate non adiabatic energy along with adiabatic energy loss. Contrasts to these, fully adiabatic circuits dissipate only adiabatic power which is inherent due to circuit topology and transistor switching [11-12]. Two main rules while switching the transistors that need to be taken care are regarding the equivalent potential across source and drain terminals while switching 'ON' the transistors and zero current across the switch while switching it "OFF". The power dissipation by the circuit even after following the above rules constitutes the adiabatic energy loss. Secondary an alternate power source is used instead of constant source for reducing the rate of charge transfer in the circuit nodes. Reducing the rate provides mechanism for low down the power dissipation. These two mechanisms allows the circuit operation to a satisfactory level keeping the power equation with in prescribed boundaries [4,5,8,9]. Equation 1 shows the said control on power dissipation by rate of charge transfer using an alternate periodic voltage source as depicted in figure 1 [6,7].

$$E = \int_0^T {RC^2V^2}/{T^2}\, dt = {RC}/{T}\, CV^2 \quad \ldots 1$$

2. RECONFIGURABLE CPL ADIABATIC GATED LOGIC
Figure 2 shows the block representation for proposed RCPLAG universal gate. Being based upon CPL family both prime and unprimed inputs are used, which assist in circuit evaluation for 'Nand' and 'Nor" functionalities. Seven Nmos and four Pmos are used for implementing the dual functionalities. Both out and complementary out signals are generated with good level of signal integrity, as conventional inverter pair are used in the last stage for output signal processing maintaining the proper strength assisting the easy integration with next stage processing. CNT control signal is used for configuring the circuit topology into 'Nand' gate or 'Nor" gate functionalities. The advantages associated with CPL family namely high operating speed compensated the slow charge transfer process in adiabatic logic families [13-15]. CPL further assists in lowering the power dissipation by making use of Nmos transistors. In RCPLAG authors have used 2 Pmos switch for control signal actuation which can be implemented using Nmos switch and primed signal. The adiabatic logic concept reduces the rate of charge transfer and hence uses a time varying source as supply called power source as shown in figure 4. Authors have make use of same

time variant power source as clock as well for gating purpose. The gating in combinational block assists in controlling the time variables [1-3, 11-12]

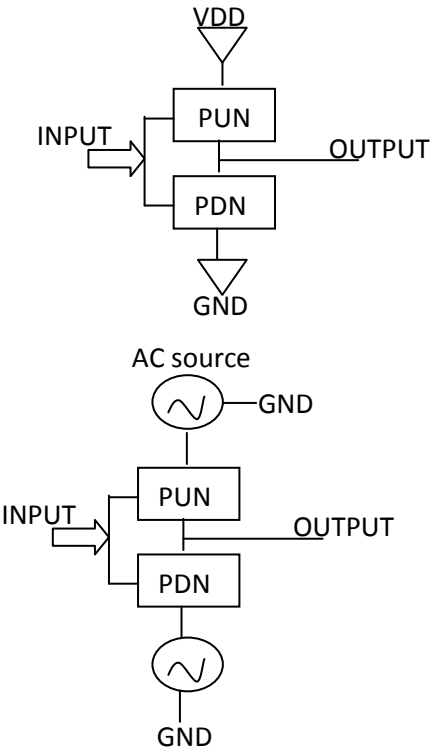

Fig 1: CMOS structure and adiabatic structure outlay

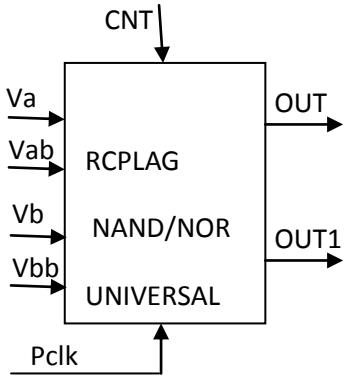

Fig 2: RCPLAG block level representation

3. RCPLAG NAND/NOR

3.1 Circuit Description

The proposed circuit topology is shown in figure 3. Seven Nmos and 4 Pmos transistors are used. 2 Pmos transistors which can be replaced by 2 Nmos transistors with primed signal actuation are used for control signal. Another two Pmos transistors are used in conventional back to back connected inverter stage driven by power clock. This guarantees the output signal integrating and proper strength levels improving the noise margins associated. Asynchronous gating is used which can be converted into synchronous behavior with the use of one additional transistor. Output terminal out provides functionality of 'Nor" and Out1 provides 'Nand' with associated complimentary levels at other terminal respectively.

3.2 Circuit Implementation

A trapezoidal power clock having four phases as shown in figure 4 is used as power source. Actions performed by the circuit during different phases are as follows:

a) Evaluate phase- Based upon input signal permutations logic is evaluated
b) Hold phase- The evaluated logic is maintained
c) Recovery phase- Charge stored in circuit nodes are harvested back to source/sources.
d) Idle phase- No action. Potential are equal and next input are actuated.

The implementation parameters associated for the circuit simulation are tabulated in Table 1. The circuit simulation waveforms are shown in Figure 5 and Figure 6.

Table 1. Simulation parameters

Simulation parameters			
Technology	**Value**	**Simulation**	**Value**
Channel Length	.180 microns	Power clock	pulse type with Trise and Tfall
Min. width	.180 microns	Input Signal	Bit type
Max. width	36 microns	Delay calculation	50% points
|Vton|	0.3932664	Data Sequence	8 cycles
TOX	4.10E-09	Power clock Time period	40 micro sec
MOS Gate Capacitance Model:			
capmod=0			
Conditions:			
Voltage	1V to 5 V (+0.5V)		
Temperature	25		

For first hand calculations basic Nmos and Pmos current equations as shown below, for three regions of operation are used.

$$Id = {}^{k}/_{2}\,[2(Vgs - Vt)Vds - Vds^{2}] \quad \ldots 2$$

$$Vgs \geq Vt, Vds \leq Vgs - Vt$$

$$Id = {}^{k}/_{2}\,(Vgs - Vt)^{2} \quad \ldots 3$$

$$Vgs \geq Vt, Vds > Vgs - Vt$$

$$Ids = 0\ Vgs < Vt \quad \ldots 4$$

where I_d = Drain to Source current, k = device transconductance ($\mu_n C_{ox} W/L$), V_{gs} = Gate to source voltage, V_{ds} = Drain to source voltage, V_t = Threshold voltage, μ_n = Electron surface mobility, C_{ox}=Gate oxide capacitance per unit area. From these equations, drain current depends upon the biasing, transistor size and threshold voltage. So

controlling and analyzing these parameters provide mechanism to control the operation region for the transistors in the said circuit and hence the drain currents.

4. RESULTS

The required 'Nand' and 'Nor" functionalities are examined for different voltage levels and transistor size. The circuit is investigated with 9 voltage levels namely 1V, 1.5V, 2V, 2,5V, 3V, 3.5V, 4V, 4.5V and 5V peak levels using a trapezoidal power source. The signal integrity for the circuit is found to be satisfactorily working for the said power source levels. Further it is analyzed for 20 transistor widths namely 1.8µ, 3.6µ, 5.4µ, 7.2µ, 9µ, 10.8µ, 12.6µ, 14.4µ, 16.2µ, 18µ, 19.8µ, 21.6µ, 23.4µ, 25.2µ, 27µ, 28.8µ, 30.6µ, 32.4µ, 34.2µ and 36µ.

The power delay product is shown in Figure 7. The power drawn from two signals are higher as compared to power source, yet the PDP wrt to power source is on higher side for larger voltage levels as compared to PDP for signals. As the supply voltage increases slope for PDP – power source increases exponentially as compared to linear increase in signal PDP approximately. Till 2V voltage range all PDP shows similar variation wrt voltage change. After 2V the variation in power source PDP and signal PDP is quite high. Therefore good operating condition for the proposed circuit is in the range of 0.6V to 2V and best PDP would be till 1.5V. PDP range from 0.06p and 4p units for 1V and 1.5V respectively associated with 7.5nW power at 1V and 0.6µW power dissipation at 1.5V.

The average power distribution wrt P_{clk}/V_{puls} is shown in Figure 8. The rate of increase in average power for transistor size is more for higher voltage levels. For smaller size rate of increase of average power with voltage is linear approximately till 10 micron, but beyond this the variation becomes parabolic in nature. For same voltage levels the P_{avg} variation can be linearly interpolated wrt transistor size. Till 18micron transistor size P_{avg} is less then 10mW which is for 5V supply. In more than 75% permutations of transistor size and supply voltage the P_{avg} is less then 10mW and around 20% it is less then 20nW to 10nw. Very small part of it crosses 20nW values. At 1.8micron transistor, 1V supply, P_{avg} is 0.14µW which is very attractive option for RCLAG universal gate. There is sharp increase in Pavg for in the range of 1V to 1.5V ranging from 0.14µW to 7.25µW counting for nearly 70% increase in P_{avg} value. P_{avg} increases by 6% from 1.5V to 2V. The incremental rate in P_{avg} decrease with further voltage increase. The input signal applied to circuit needs to be having a maximum of 30-40µW for extreme case at 5V. Also for 1.8micron size, 1V supply 0.6µW input signal is sufficient for satisfactory operation of the circuit. Average power consumed from signal source is in the range of 1nW to 50nW. With increase in voltage levels the signal source strength required to be increased by 2-3% and by same factor with transistor size for particular supply voltage.

Input signal delay wrt out and complementary out (out1) terminal is shown in Figure 9. The signal to out1 delays decrease with voltage levels with a low rate. Centrally signal to out delays has variable behavior perhaps because of the change of quantum of charge at the nodes with increasing voltage levels. Till 1.5v levels delays increases lineally to 54µs approximately and remain constant till 3V, and further it increase to 78.6µs till 3.5V. Beyond 3.5V delay again remains constant. Figure 11 shows rise time and fall time variation for 1.8µ transistor size. T_{rise} and T_{fall} pertaining to out terminal are similar. Till 3V these timings are identical for out1 terminal and increases to 24µs approximately and then it remains constant for further increase in voltage levels. The increase in fall time is perhaps because of excess charge that needs to be removed from the circuit nodes. The change in quantum of force, responsible for signal integrity and proper levels leads to the timing variation with supply voltage. Normalized power distribution is shown in Figure 12 Negative normalized power depicts the feedback power and positive normalized power depicts the power drawn from the source. The power drawn from the signal is also feedback through power source. This harvesting of charge, from the circuit nodes lowers the cumulative power utilization equation for the circuit operation. Higher the charge availability because of higher supply voltage, more charge is harvested to power source as evident in the power variation graph. From signal source V_a, V_b the power is drawn which is harvested in power source. Till 1.5 V supply the variation of power flow in either direction is approximately same. Increasing supply level beyond 1.5V, charge drawn from V_a, V_b are also accumulated through power source and amount of power feedback/ harvested increases. Also power utilization for V_a, V_b and V_{ab}, V_{bb} are identical. For power supply below 3V, signal power variation is approximately same. Peak power distribution for input signal and power source are shown in figure 13 Peak power drawn from the signal is 0.1mW. Eventually normalized power drawn from signal is high as compared to power source. Power source acts as output signal establisher and reservoir for charge stored in circuit needs. On the other hand the functional evaluation process for the reconfigurable universal 'Nand'/'Nor" gate is primarily input signal driven. Also the peak power for the power source and signal can be linearly interpolated approximately. Node capacitance contribution in circuit topology is shown in figure 14. 16% of total capacitance is commutatively accounted by input nodes and least 2% is accounted by out terminals. Rest part of the capacitance is accounted by intermediate nodes and a max of 21% is at the 'ndnr' node at parallel combination of two circuit chains. Input resistance decreases sharply parabolically till 3V power supply and then remains constant beyond 3V. Input resistance is high for low voltage and low for high voltage levels. Also input resistance for V_{ab}, V_{bb} and V_a, V_b are identical. An offset exist between these two for low voltage till 3V and input resistance becomes identical. This form a parabolic L shaped behavior with supply voltage. Output resistance is independent of supply voltage which is 3.52n units.

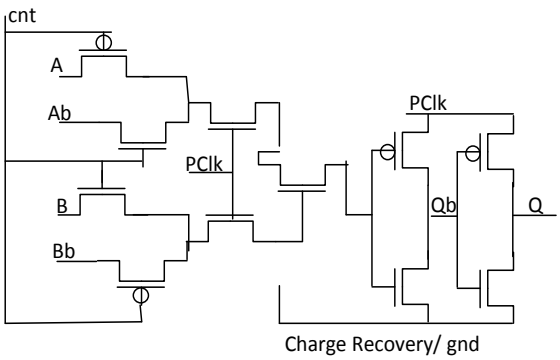

Fig 3: Proposed RCPLAG Nand/Nor universal gate

Table 2. Rise and Fall timings for Q and Qb

Vdd	Qtrise	Qtfall	Qbtrise	Qbtfall
1	1.27E-04	1.38E-04	7.91E-06	6.74E-06
1.5	1.25E-04	1.42E-04	5.33E-06	2.05E-06
2	6.43E-05	6.38E-05	2.94E-06	1.24E-06
2.5	6.43E-05	6.50E-05	2.15E-06	1.21E-06
3	6.41E-05	6.58E-05	1.70E-06	1.36E-06
3.5	6.38E-05	6.64E-05	2.57E-06	2.43E-05
4	6.38E-05	6.68E-05	2.26E-06	2.44E-05
4.5	6.40E-05	6.72E-05	2.03E-06	2.45E-05
5	6.41E-05	6.74E-05	1.89E-06	2.47E-05

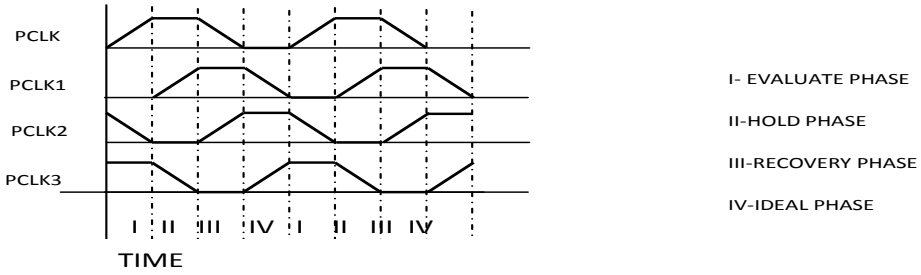

Fig 4: Four Phase power Clock Pclk

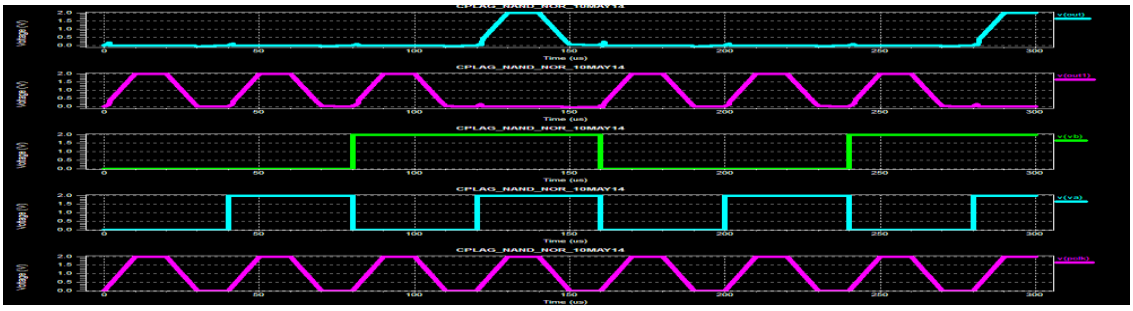

Fig 5: Simulation waveform for RCPLAG NAND/NOR – NAND functionality

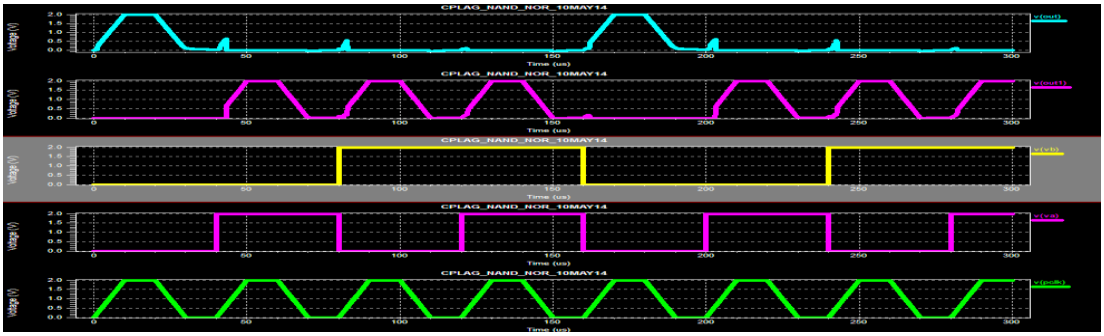

Fig 6: Simulation waveform for RCPLAG NAND/NOR – NOR functionality

Table 3. Average Power comparison

Power Results Nand	
Vpulse_voltage : 4 phase trapezoidal source	
Average power consumed SCMOS	57.76nW
Average power consumed Proposed design	12.2nW

5. CONCLUSION

In the reported work authors have illustriously consolidated the benefits of CPL based circuits and adiabatic logic conjoint the use of clock for even combinational blocks and reported the power diminution. Augmenting further authors have applied reconfigure-ability concept and contemplated and implemented reconfigurable RCPLAG 'Nand'/'Nor' gate universal gates. The functionality of the proposed universal gates is studied and found to be satisfactory. The circuit topology consisting of 4 'Pmos' and 7 'Nmos' transistors, provides the inherent advantages of CPL family. The usage of the clock further assist in timing analysis hence the circuit can be easily synchronized with sequential circuits. The time varying power source used in adiabatic functionality implementation methodology is used as clock signal for the circuit. The circuit has asynchronous gating capability which can be converted into synchronous with one additional transistor. The signal integrity and output swing levels are maintained both 'Nand/Nor' out and it complementary output terminal through traditional inverter pair driven by power clock signal. The functioning is examined a) 11 different voltage levels (0.6V, 0.8V, 1V, 1.5V, 2V, 2.5V, 3V 3.5V, 4V, 4.5V and 5V); b) 20 different transistor sizes (1.8µ, 3.6µ, 5.4µ, 7.2µ, 9µ, 10.8µ, 12.6µ, 14.4µ, 16.2µ, 18µ, 19.8µ, 21.6µ, 23.4µ, 25.2µ, 27µ, 28.8µ, 30.6µ, 32.4µ, 34.2µ, 36 µ) at 25^{o}C. For all these the circuit is analyzed for a) average power from P_{clk}, data inputs; b) P_{clk}_Q delay; c) Input_Q delay; d) power delay product; e) Normalized power drawn and fed back to P_{clk} source. From the PDP variation 0.8V to 3V voltage range, at 50^{o}C, with load of 0.8pf, working with 180nm technology is best suited for circuit working. The average power at 2V is 12.2nW, for different run with P_{clk}_Q delay 50µs, input_Q delay 5µs, Qt_{rise}=0.125ms, Qt_{fall}=0.142µs, Qb_{trise}=5.33µs, Qbtfall=2.5µs with 52p, 78f, 6p, 6p units PDP for V_{puls}, V_a, V_b, V_{ab}, V_{bb} respectively. The improvement in the average power drawn is very much evident while comparing the implemented 'Nand'/'Nor" gates with conventional CMOS. The average power consumption for a conventional CMOS gate is 57.7nW approx as compared to 12.2nW for the implemented 'Nand'.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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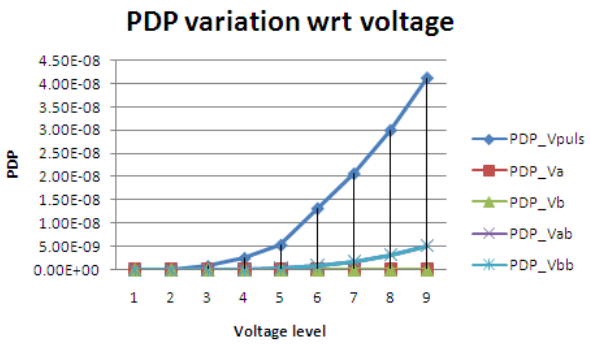

Fig 7: PDP for voltage variation

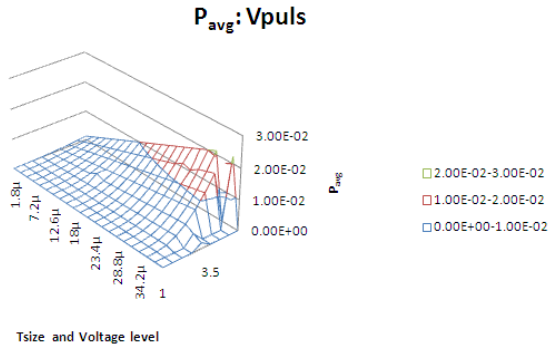

Fig 8: Average Power wrt Vpuls and T size

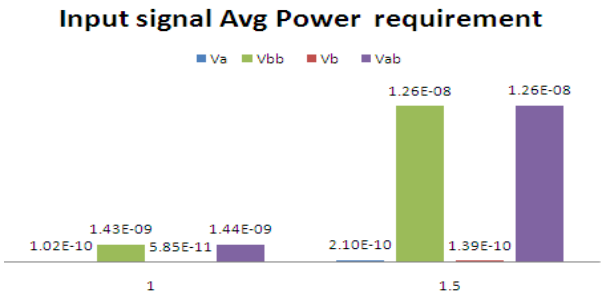

Fig 9: Average Power requirement for Input signal

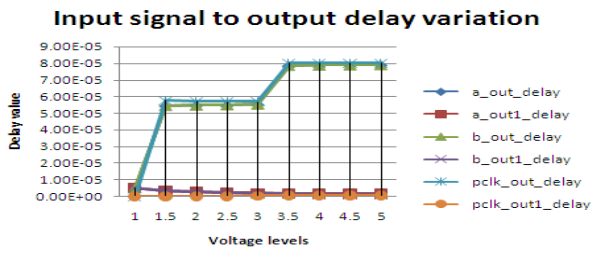

Fig 10: Delay variation wrt input signals

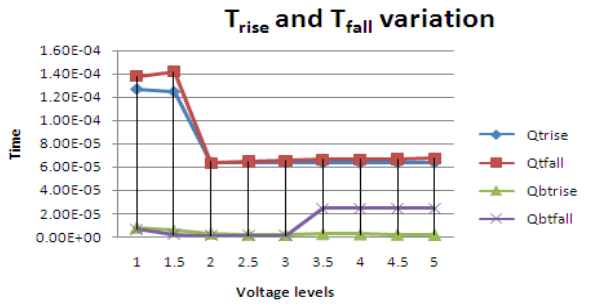

Fig 11: Rise Time and Fall Time variation with voltage

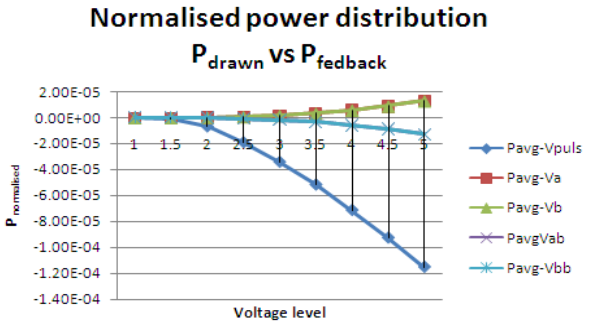

Fig 12: Power drawn and power fedback distribution

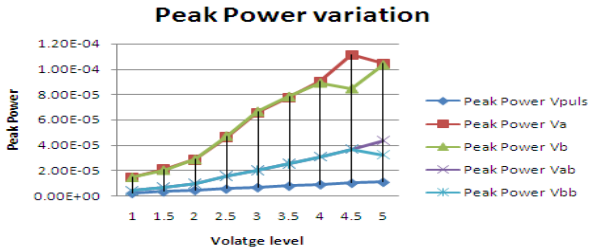

Fig 13: Peak power distribution

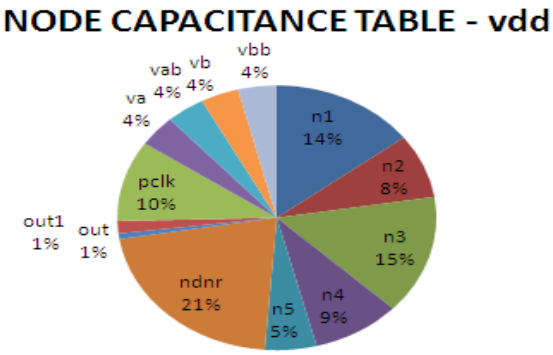

Fig 14: Capacitance distribution

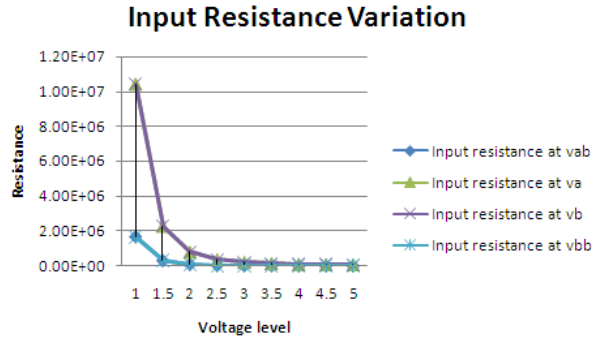

Fig 14: Input resistance distribution