# Modified Two Phase Clocked Adiabatic Static CMOS Logic

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## ABSTRACT
In the past decade, various adiabatic logic techniques have been proposed by various authors. One of the widely known adiabatic logic style is Two Phase Clocked Adiabatic Static CMOS Logic (2PASCL). The logic circuits based on 2PASCL suffer from floating output node due to alternate hold phase in its operation. Keeping a node floating for a long time may result in erroneous node voltage. In this paper a technique to reduce the floating node problem associated with 2PASCL is introduced. Modified 2PASCL is used to design a 2-input NAND gate, a 2-input NOR gate and 1- bit full adder at 45nm technology parameters provided by predictive technology and the circuits are simulated using HSPICE. The 2- input NAND gate designed with Modified 2PASCL is compared with the NAND gates designed with 2PASCL and Static CMOS in terms of average power consumed by them for different values of load capacitance and input frequency. NAND gates are also compared in terms of propagation delay, power delay product and the transistor count to implement them. It is observed that the NAND gate based on Modified 2PASCL offer up to 80.3% power saving in comparison to NAND gate based on static CMOS and also exhibit least power delay product.

## General Terms
Adiabatic Logic, Charge Recycling.

## Keywords
Low Power, Energy Recovery, Floating Node.

## 1. INTRODUCTION
In current era, the demand for more functionality at the same time, portability is very high. In applications like portable devices, energy consumption has become an important concern as the users require smaller devices with prolonged battery life. The major source of power dissipation in digital circuits is the dynamic power. There are several methods to reduce the power dissipation. One of the interesting methods to reduce the dynamic power dissipation is the circuits based on energy recovery or adiabatic logic. The logic circuits designed using adiabatic logic are gaining attention due to their low power dissipation characteristic.

Adiabatic logic minimizes the power dissipation by reducing the dissipation across resistances of ON or conducting MOSFETs and recovering the part of energy given to the output back to the source, which extends the battery life. Several adiabatic logic families have been proposed by different authors in their research work [1], [2], [3], [4], [10], [11], [12], [13], [14].

One of the widely known adiabatic logic style is Two phase clocked adiabatic static CMOS logic [12], [13]. The logic circuits based on 2PASCL suffer from floating output node due to alternate hold phase in its operation [13]. In this paper a techniques to reduce the floating node problem associated with 2PASCL is proposed. The NAND designed with Modified 2PASCL is compared with NAND gates designed with Static CMOS and 2PASCL in terms of average power consumption for different values of load capacitance, input frequency. They are also compared in terms of propagation delay, power delay product and transistor count to implement them.

## 2. ADIABATIC CHARGING

### 2.1 Conventional Charging
The strongest component of the power dissipation in a static CMOS device is the dynamic power required to charge and discharge the capacitive nodes within the circuit [3]. To charge the node capacitance $C_L$ from a dc supply of potential $V_{DD}$, an energy $E = C_L V_{DD}^2$ is withdrawn from supply. Only half of this energy is temporarily stored in capacitor $C_L$. The remaining $0.5C_L V_{DD}^2$ is dissipated as heat in the on resistance of PMOS. When input becomes logic high, the NMOS turns on and energy stored on capacitor $C_L$ is discharged to the ground and dissipated as heat. Hence during a complete charge- discharge cycle, the energy $E = C_L V_{DD}^2$ is withdrawn from power supply and is dissipated as heat. Half of this energy is dissipated during charging and half is dissipated during discharging.

### 2.2 Adiabatic Charging
In static CMOS logic, the sudden application of supply voltage gives rise to high potential across the switching device. The energy dissipation during charging and discharging can be minimized to a great effect by ensuring that the potential across switching device is kept sufficiently small. Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0V. This time varying source rises towards V at a slow rate that ensures that potential across switching device is kept arbitrarily small. The adiabatic charging is shown in Fig 1.

In fact the energy dissipated across the resistance, R is

$$E_{diss} = I^2RT = (RC/T)\, CV_{DD}^2 \qquad (1)$$

From the above Eqn. (1), we can see that if $T >> RC$, the energy dissipation during charging, $E_{diss} \approx 0$. Same is applicable during discharge process.

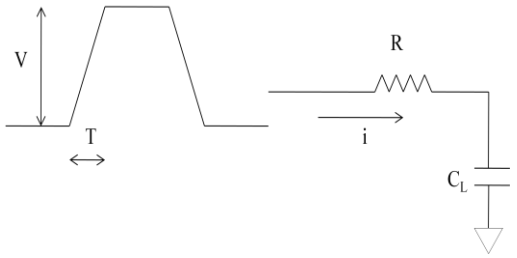


**Fig 1: Adiabatic Charging**

In addition to this, in some adiabatic logics, the energy dissipation also occurs due to threshold voltage of MOSFET or potential difference between drain and source of conducting MOSFETs and diode cut-in voltage [7].

The energy dissipation due to threshold voltage, Vt is

$$E = 0.5CVt^2 \quad (2)$$

The energy dissipation due to diode cut-in voltage, Vd is

$$E = C_L VdVs \quad (3)$$

Where Vs is voltage swing.

## 3. TWO PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC

In the adiabatic logic families [4], [8], [10], [11] which include diode in charging path suffer from output amplitude degradation. To deal with this problem, Anuar et al proposed a new logic family named as two phase clocked adiabatic static CMOS logic [12], [13]. This logic family does not include diode in charging path, so that output amplitude degradation does not occur. The 2 phase clocked adiabatic static cmos logic uses a two phase clocking split level sinusoidal power supply as shown in Fig 2. One is in phase while the other is inverted. The voltage level of Vclk exceeds that of $\overline{Vclk}$ by $V_{DD}/2$. By using these two split – level sinusoidal waveforms, which have peak to peak voltages of 0.5V, the voltage difference between the current carrying electrodes can be minimized and subsequently, power consumption can be suppressed [12], [13]. It uses two diodes- one diode is placed between output node and power clock, Vclk and the other diode is placed adjacent to nmos logic circuit and connected to other power clock, $\overline{Vclk}$ . Both the diodes are used to recycle the charge from output node and to improve the discharging speed of internal nodes.

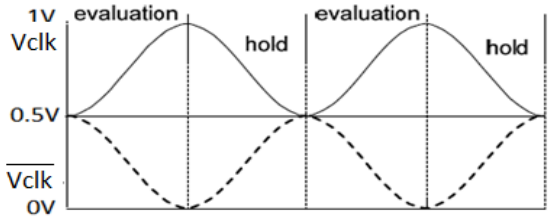


**Fig 2: Power Clocks in 2PASCL**

The schematic of an inverter using this logic family and along with resulting waveforms after simulation is shown in Fig 3.

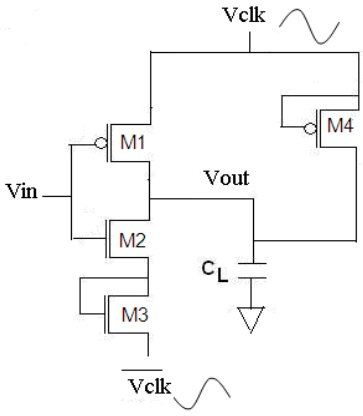


**Fig. 3(a): Inverter using 2PASCL**

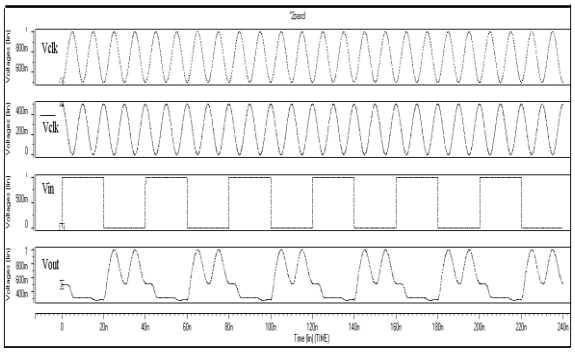


**Fig. 3(b): Simulation Results of 2PASCL Inverter**

### 3.1 Circuit Operation

The circuit operation is divided into two phases: evaluation and hold. In the evaluation phase, Vclk swings up and $\overline{Vclk}$ swings down. On the other hand, in the hold phase, $\overline{Vclk}$ swings up and Vclk swings down.

When Vclk and $\overline{Vclk}$ are in evaluate mode, there is conducting path in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged .When Vclk and $\overline{Vclk}$ are in hold mode, output node holds its value in spite of the fact that Vclk and $\overline{Vclk}$ are changing their values. Circuit nodes are not necessarily charging and discharging every clock cycle, reducing the switching activity. For example in evaluate mode, if the output is logic low and Vin is made logic low, the PMOS will be on and the load capacitor will be charged through PMOS transistor, hence the output in high state. But as no diode is connected in charging path to control backward charge flow, backward flow of charge from load capacitor to Vclk will occur through PMOS transistor (M1) and diode(M4), when $V_{out}$ becomes higher than Vclk. But when Vout is logic high and Vin is made logic high, the PMOS transistor will be off and NMOS is ON and discharging via NMOS (M2) and diode (M3) combination along with diode (M4) will occur and will get logic low output. But suppose Vout is high and Vin is made logic low, no transition will occur. One can clearly see ripples in output due to absence of diode in charging path.

## 3.2 Sources of Power dissipation

The sources of power dissipation in this logic family are diode cut-in potential, the potential drop between drain and source of conducting MOSFETs and dissipation in resistance of PMOS and NMOS while charging and discharging the load. The use of slowly varying power clocks ensures the small energy dissipation across the ON resistance of MOS devices. It is to be noted that the static power dissipation has been ignored as it is not the dominating component of power dissipation.

The energy dissipated in a single inverter is given by

$$E_{2PASCL} = 0.5C_L(|V_{tp}|)^2 + 0.5\, C_L\, Vclk_{p\text{-}p}\, |V_{tp}| + 0.5C_L(\overline{Vclk} - V_{tn})\, V_{tn} \quad (4)$$

## 3.3 Merits of 2PASCL

There are several merits associated with 2PASCL logic which are as follows: It eliminates the energy loss due to the diode in the charging path. Amplitude does not degrade due to absence of diode in charging path [12], [13]. It offers significant energy saving in comparison to the static CMOS Logic.

## 3.4 Demerits of 2PASCL

Although the 2PASCL offer significant energy saving in comparison to static CMOS logic, it suffers from floating output node due to the alternate hold phases during circuit operation [13]. Keeping a node floating for a long time may give erroneous result.

## 4. PROPOSED WORK

The logic circuits based on 2PASCL suffer from floating output node due to the alternate hold phases during circuit operation [13]. In this section a technique to reduce the floating node problem associated with 2PASCL is reported.

Inverter based on Modified 2PASCL is shown in Fig.4.1. It can be seen from the Fig. 4.1 that the circuit does not include the PMOS diode used for discharging the output node or recycle the charge in 2PASCL.

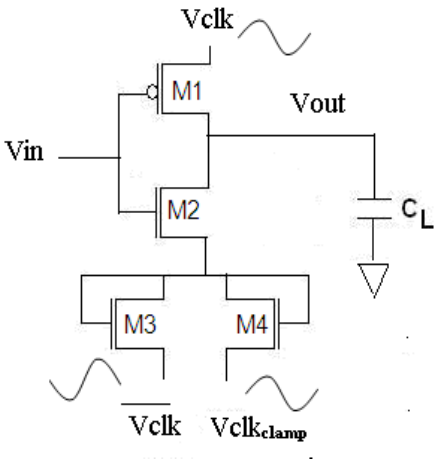


**Fig 4: Inverter using M2PASCL**

But in M2PASCL, a diode (M4) has been added in pull down network for discharging the output node or charge recovery. The n-terminal of the diode (M4) is connected to clamped version of Vclk. The M2PASCL based inverter also uses split level sinusoidal power supplies Vclk and $\overline{Vclk}$ as was the case in 2PASCL. Beside these two power clocks M2PASCL based inverter also uses one additional power clock which is clamped version of Vclk with peak value of $V_{DD}/2$ and peak to peak value also of $V_{DD}/2$. The power clock (Vclk) and clamped version of power clock named as $Vclk_{clamp}$ are in same phase while $\overline{Vclk}$ is in opposite phase as shown in Fig 5.

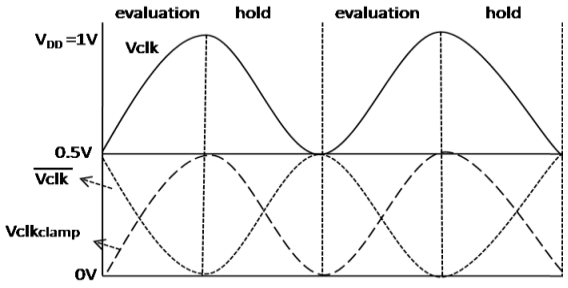


**Fig 5: Power Clocks in M2PASCL**

The simulation waveforms of inverter designed using 45nm technology parameters are shown in Fig 6. The value of $V_{DD}$ is 1V and Power clock frequency is 100MHz for all three power clocks. The load capacitance is 10f farad and input frequency is 25MHz. The channel length is kept at 45nm for both NMOS and PMOS transistors. The channel width is selected to be 67.5n and 202.5n for NMOS and PMOS transistors respectively.

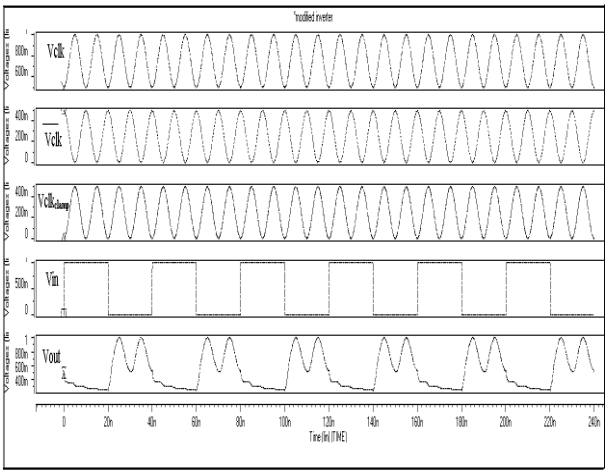


**Fig. 6: Simulation Results of M2PASCL Inverter**

## 4.1 Circuit Operation

The operation of circuit can explained as follows: The circuit operation is divided into two phases: evaluation and hold. In the evaluation phase, Vclk as well as $Vclk_{clamp}$ swings up but $\overline{Vclk}$ swings down. On the other hand, in the hold phase, $\overline{Vclk}$ swings up but Vclk and $Vclk_{clamp}$ swings down. In evaluate mode, there is conducting path in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged .When Vclk, $Vclk_{clamp}$ and $\overline{Vclk}$ are in hold mode, output node holds its value in spite of the fact that Vclk, $Vclk_{clamp}$ and $\overline{Vclk}$ are changing their values.. For example in evaluate mode, if the output is logic low and Vin is made logic low, the PMOS will be on and the load capacitor will be charged through PMOS transistor, hence the output in high state. But as no diode is connected in charging path to control backward charge flow, backward flow of charge from load capacitor to Vclk will occur through PMOS transistor (M1) when $V_{out}$ becomes higher than Vclk. Now consider the case when the power clocks are in evaluate mode with Vout = logic high and Vin is made logic high, the PMOS transistor will be off and NMOS is ON and for discharging two paths are available for

discharging via NMOS (M2) and diode (M3) combination or NMOS( M2) and diode (M4) combination. But at beginning of evaluation mode the value of $Vclk_{clamp}$ is 0V while the value of $\overline{Vclk}$ is $V_{DD}/2$, the path consisting of NMOS (M2) and diode (M4) will get activate and the output node will get discharged through this path and will get logic low output. But as $Vclk_{clamp}$ starts rising towards $V_{DD}/2$, the output node should become floating but the problem is soon removed as $\overline{Vclk}$ swings down and connect the output node to $\overline{Vclk}$ through NMOS (M2) and diode (M3). Similarly in hold mode $\overline{Vclk}$ swing towards $V_{DD}/2$ and made the output node floating but this floating node problem is soon removed as $Vclk_{clamp}$ swings down and connect the output node to $Vclk_{clamp}$ through NMOS (M2) and diode (M4) eliminating weak low problem.

## 4.2 Sources of Power dissipation

If we ignore the static power dissipation then the sources that causes power dissipation in M2PASCL based inverter are:

- Drain-source potential difference when a MOS transistor begins to be conductive.
- Diode Barrier Voltage.
- Dissipation across ON resistance of the MOS transistors.

As the energy dissipation across ON resistances of MOS transistors is negligible in adiabatic logic circuits, the equation for the energy consumption in M2PASCL inverter is

$$E_{M2PASCL} = 0.5C_L (|V_{TP}| - V_d)^2 + C_L (Vclk_{clamp(\,p\text{-}p)} - V_d) V_d + C_L(V_{error} - V_d)V_d \quad (5)$$

Where $V_d$ is the diode barrier potential and $V_{error}$ is the voltage at the output node for momentary floating state.

## 4.3 NAND Gate using M2PASCL

A two input NAND is designed using 45nm technology parameters at 1V, provided by predictive technology. The channel length is kept at 45nm for all the NMOS and PMOS transistors. The channel width is selected to be 67.5n and 202.5n for NMOS and PMOS transistors respectively. The power clock frequency used is 100 MHz. Simulation is carried out using HSPICE at load capacitance of 10f farad with the inputs having frequency of 25MHz and 12.5MHz and observed the transient simulation waveforms. The schematic to realize a two input NAND gate using M2PASCL is shown in Fig 7(a). The simulation results are shown in Fig 7(b).

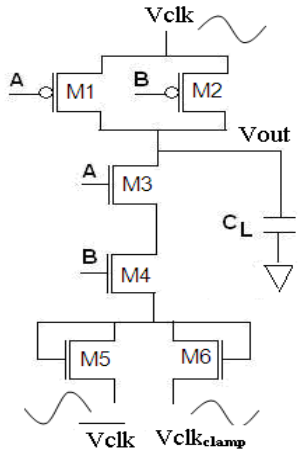


**Fig 7(a): NAND gate using M2PASCL**

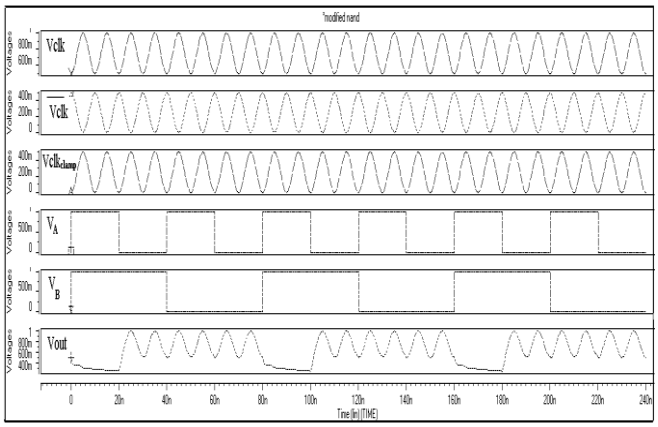


**Fig 7(b): Simulation Results of NAND gate using M2PASCL**

By observing the simulation results in Fig 7(b), basic operation of NAND gate can be verified easily as the output is logic high when at least one of the input is logic low and the output is logic low only when both the inputs are logic high.

## 4.4 NOR Gate using M2PASCL

A two input NOR is designed using 45nm technology parameters at 1V, provided by predictive technology. The channel length is kept at 45nm for all the NMOS and PMOS transistors. The channel width is selected to be 67.5n and 202.5n for NMOS and PMOS transistors respectively. The power clock frequency used is 100 MHz. Simulation is carried out using HSPICE at load capacitance of 10f farad with the inputs having frequency of 25MHz and 12.5MHz and observed the transient simulation waveforms. The schematic to realize a two input NOR gate using M2PASCL is shown in Fig 8(a). The simulation results are shown in Fig 8(b).

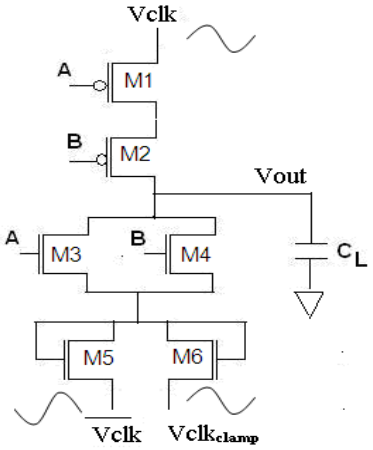


**Fig 8(a): NOR gate using M2PASCL**

The simulation results are shown in Fig 8(b). By observing the simulation results in Fig 8(b), basic operation of NOR gate can be verified easily as the output is logic low when at least one of the input is logic high and the output is logic high only when both the inputs are logic low.

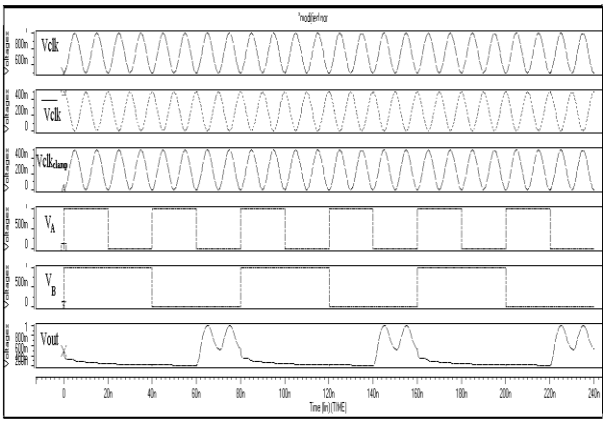


**Fig 8(b): Simulation Results of NOR gate using M2PASCL**

# 5. COMPARISON OF NAND GATES

In this section, the 2-input NAND gates designed with 2PASCL, M2PASCL and static CMOS logic using 45nm technology parameters are compared on the basis of :

1) Effect of variation of different parameters on the average power consumed by them.
2) Propagation delay.
3) Power Delay Product
4) Transistor count to implement the NAND gate.

## 5.1 Effect of variation of different parameters on the average power consumed by them

In this section, the simulation of the 2-input NAND gate is done with varying parameters and the effect of these variations on average power consumed by each NAND gate design is observed. The results so obtained are discussed and compared. The channel length and channel width are selected as 45nm and 67.5nm respectively for all NMOS transistors. Similarly the channel length and width for all the PMOS transistors are selected to be 45nm and 202.5nm. To keep comparison fair, power clock frequency is kept constant at 100MHz for both the 2PASCL and M2PASCL. The frequency of power clock is kept higher than frequency of input, so that effect of phase is not dominating. The simulation of NAND gate designed with these logic families is done for: 1) Varying load capacitance, 2) Varying Input frequencies.

### *5.1.1 Effect of Variation in Load Capacitance*

Normally load capacitor in CMOS based logic forms due to the parasitic capacitances of transistors and interconnects, so the value of load capacitance depends on transistor sizes, interconnect wires, fan- out etc. To observe the effect of variation in these parameters on average power consumption, an external capacitor is connected to represent the load capacitance. Now this load capacitance is varied and the performance of NAND gate is evaluated. In this section, the effect of variation in load capacitance on average power consumed by the NAND gates designed with 2PASCL, M2PASCL and Static CMOS logic is observed. The results so obtained are discussed and compared together.

The power clock frequency is selected to be 100MHz. Input frequencies are 25MHz and 12.5MHz respectively for input A, B of a NAND Gate. The operating temperature is 25°C. The load capacitance $C_L$ is varied from 10f farad to 200f farad in steps of 20f farad and the resulting average power consumption is observed. The simulation results obtained are shown in Table 1.

**Table 1. Variation of Average power consumption with Load capacitance in different NAND Gates**

| $C_L$ (fF) | Average Power Consumption in nano watts | | |
|---|---|---|---|
| | Static CMOS | 2PASCL | M2PASCL |
| 10 | 151.40 | 27.20 | 29.80 |
| 30 | 402.70 | 106.00 | 114.60 |
| 50 | 668.20 | 215.40 | 232.70 |
| 70 | 940.50 | 346.40 | 376.70 |
| 90 | 1186.00 | 492.70 | 538.80 |
| 110 | 1405.00 | 650.60 | 707.10 |
| 130 | 1692.00 | 812.90 | 881.40 |
| 150 | 1925.00 | 973.60 | 1059.00 |
| 170 | 2138.00 | 1130.00 | 1225.00 |
| 190 | 2397.00 | 1285.00 | 1389.00 |

On the basis of simulation results shown in Table 1, a graph has been plotted showing the variation of average power consumption with variation in Load Capacitance as shown in Fig 9.

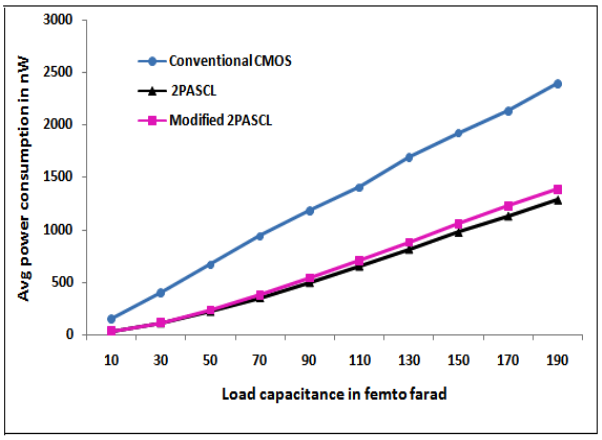


**Fig 9: Variation of Average power consumption with Load capacitance in different NAND Gates.**

As per earlier chapters, the dynamic power is the most dominating source of power dissipation and is directly proportional to the load capacitance. It should increase with increase in load capacitance and above simulation results confirm that. It can be seen in the NAND gate based on static CMOS, the power consumption is rising with rise in load capacitance. From the results mentioned in Table 1 and shown in Fig 9, it is also observed that the NAND gates based on 2PASCL and M2PASCL which utilize the concept of slow charging/ discharging and energy recovery, consume less power in comparison to Static/Conventional CMOS based NAND gate for all of the value of load capacitance.

In 2PASCL based designs, the energy dissipation occurs due to diode voltage ($V_d$) of MOSFET, threshold voltage ($V_t$) of MOSFET, and energy dissipated in MOS resistance to charge and discharge the Load capacitance. Now these components of energy dissipation increases with increasing load capacitance. Now during charging of load capacitance the current through the pull up network flows almost for complete half cycle and every time the current flow through the MOSFET resistance

the power will dissipate. NAND Gate based on 2PASCL is offering up to 82% power saving in comparison to the NAND gate based on Static CMOS.

The M2PASCL includes an additional diode in the discharging path connected to clamped version of power clock ($V_{clk}$) to reduce the floating node problem encountered in 2PASCL. Inclusion of this additional diode provides an alternate path for discharging. In 2PASCL, when the output is logic low and in hold mode, no energy consuming transition occurs and the output node remains floating. But in M2PASCL, the output node can get discharged through either of the two paths available for discharging eliminating the floating node problem but at the expense of little increment in power dissipation. In M2PASCL based design, the energy dissipation occurs due to barrier voltage ($V_d$) of diode, Drain-source potential difference when a MOS transistor begins to be conductive, and energy dissipated in MOS resistance to charge and discharge the Load capacitance. Now these components of energy dissipation increases with increasing load capacitance. Now during charging of load capacitance the current through the pull up network flows almost for complete half cycle and every time the current flow through the MOSFET resistance the power will dissipate. NAND Gate based on M2PASCL is offering up to 80.3% power saving in comparison to the NAND gate based on Static CMOS.

From Fig 9, it is found that the NAND Gate designed with 2PASCL and M2PASCL offer significant power saving in comparison to NAND Gate based on Static CMOS. M2PASCL based NAND gate consume little more power in comparison to NAND gate based on 2PASCL but it adds robustness to the circuit by reducing floating node.

### *5.1.2 Effect of Variation in Input Frequencies*

In this section, the effect of variation in input frequency on average power consumed by the NAND gates designed with 2PASCL, M2PASCL and Static CMOS logic is observed. The results so obtained are discussed and compared together.The power clock frequency is selected to be 100MHz. The load capacitance $C_L$ is fixed at 10f farad and operating temperature is kept at 25°C. Here to represent frequency, we have used $T_{ON}$. Now, as we have used square pulse as input having 50% duty cycle, frequency, $f = \frac{1}{T_{ON} + T_{OFF}}$ . As $T_{ON}$ will increase, the frequency will decrease. Also, as NAND gate designed here has two inputs; A and B, their time periods are selected as $T_A = 2T_B$. Here, the variation of average power consumption with $T_{ON}$ of input A is shown. But as per the relationship mentioned between time periods of input A, and input B the time periods of both the inputs will vary or their frequency will also vary. The simulation results obtained are shown in Table 2.

**Table 2. Variation of Average power consumption with $T_{ON}$ or frequency of input Signals in different NAND Gates.**

| $T_A$(ON) (ns) | Average Power Consumption in nano watts | | |
|---|---|---|---|
| | Static CMOS | 2PASCL | M2PASCL |
| 50 | 123.80 | 50.90 | 53.50 |
| 100 | 66.10 | 18.40 | 19.20 |
| 150 | 55.90 | 28.20 | 29.10 |
| 200 | 44.50 | 15.40 | 15.70 |
| 250 | 32.20 | 19.90 | 20.20 |

On the basis of simulation results shown in Table 2, a graph has been plotted showing the variation of average power consumption with variation in $T_{ON}$ as shown in Fig 10.

Input frequency determines how often the logic switches between 1 and 0 and thus influences the power consumption of the gate. The variation of power consumed for various input data pulse widths is shown in Fig 10.

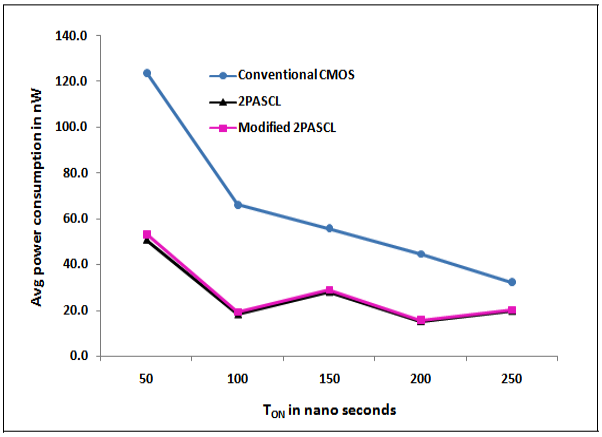


**Fig 10: Variation of Average power consumption with $T_{ON}$ or frequency of input Signals in different NAND Gates**

It is observed that, lower input frequencies (higher time periods) give a low power dissipation. With increase in frequency the power dissipation is increased as the possibility of logic switching between 1 and 0 is increased. More switching leads to more power dissipation. But it is also found that NAND gate based on 2PASCL and M2PASCL show fluctuation in power dissipation/power consumed and that is expected. The power dissipation in adiabatic logic also depends on timing of power clock with respect to input signal at the time of switching; the value of power clock at the instant of switching. In adiabatic logic, the potential difference between the nodes through which charging or discharging will take place should be minimum at the time of switching. But as the input frequency is varied, the value of power clock at the time of switching may be different for different values of input frequency. This fluctuation is more pronounced in logic families, which have ripples in the output. Because in these logic families, the potential difference between nodes can be different at the time of switching. Beside it, in NAND gate based on 2PASCL and M2PASCL, the power dissipation also depends on the duration in which the output stays in logic 1 because during this state the output node is always connected to the Power clock ($V_{clk}$) and follows it. Due to this phenomenon a current flows through the PMOS network and power gets dissipated through the on resistance of MOSFETs.

It can be observed that the NAND gates based on 2PASCL and M2PASCL offer significant power saving in comparison to NAND gate based on Static CMOS.

## 5.2 Comparison of NAND Gates on the Basis of Propagation Delay

The propagation delay of a gate defines how quickly it responds to a change at its input. It expresses the delay experienced by a signal when passing through a gate.

In the previous section, the different designs of full adder were compared on the basis of average power consumed by them for different values of parameters. In adiabatic logic, the

reduction in power dissipation comes at the expense of increased propagation delay or decreased operating speed and sometimes increased fabrication space. To know which design of NAND gate offers maximum operating speed and which design offers least operating speed, the propagation delay exhibit by them is compared.

Here, power clock frequency is kept at 100 MHz and input frequencies are kept at 25MHz, 12.5MHz for the two inputs of NAND. The propagation delay exhibit by each NAND gate designed with Static CMOS, 2PASCL and M2PASCL for different values of load capacitance is shown in Table 3.

**Table 3. Propagation Delay in Different NAND Gates**

| $C_L$ (Ff) | Propagation Delay | | |
|---|---|---|---|
| | Static CMOS | 2PASCL | M2PASCL |
| 10 | 0.13ns | 2.15ns | 0.65ns |
| 30 | 0.35ns | 2.6ns | 1ns |
| 50 | 0.5ns | 3ns | 1.35ns |
| 70 | 1ns | 3.4ns | 2.1ns |

It can be observed from Table 3, as the value of load capacitance increases the propagation delay exhibit by each NAND gate increases. It can also be seen that the propagation delay is minimum in static CMOS based NAND gate for all the values of load capacitances. Adiabatic logic based designs offer power savings at expense of increased propagation delay because they rely on the slow charging and discharging of output nodes to preserve power.

Modified 2PASCL based NAND gate exhibit less propagation delay in comparison to the NAND gate based on 2PASCL because of reduced $t_{PHL}$ due to discharging through clamped version of clock.

## 5.3 Comparison on the Basis of Power Delay Product

The power delay product is simply the energy consumed by the gate per switching event and can be considered as a quality measure for a switching gate. It is determined by the product of the average power consumption and the propagation delay.

The PDP of the NAND gates designed with Static CMOS, 2PASCL and M2PASCL are shown in Table 4.

**Table 4. Power Delay Product of NAND gates**

| $C_L$ (Ff) | Power Delay Product (fJ) | | |
|---|---|---|---|
| | Static CMOS | 2PASCL | M2PASCL |
| 10 | 0.020 | 0.058 | 0.019 |
| 30 | 0.140 | 0.276 | 0.115 |
| 50 | 0.334 | 0.646 | 0.314 |
| 70 | 0.941 | 1.178 | 0.791 |

It can be observed from Table 4 that the NAND gate based on M2PASCL shows least power delay product for different values of load capacitances.

## 5.4 Comparison on the Basis of Transistor Count

The fabrication space plays a big role in VLSI designs. In this section the different designs of NAND gates are compared on the basis of number of transistors to implement the NAND gate. The number of transistors used to implement the NAND gate is shown in Table.5.

**Table 5. Transistor Count to Implement NAND gate**

| Logic Family | Transistor Count |
|---|---|
| Static CMOS | 4 |
| 2PASCL | 6 |
| M2PASCL | 6 |

It can be observed from Table 5, that the NAND gates based on 2PASCL and M2PASCL use same number of transistors but NAND gate based on Static CMOS uses less number of transistors to implement a 2 input NAND gate.

# 6. CONCLUSION

After successfully implementing and analyzing the NAND gates designed with Static CMOS, 2PASCL and M2PASCL, one can say that the logic circuits based on adiabatic logic are the potential candidates for low power applications as they tend to consume very less power in comparison to the logic circuits based on static CMOS. The NAND gates designed with 2PASCL and M2PASCL offered up to 82% and 80.3% power saving respectively in comparison to NAND gates designed with Static CMOS. NAND gate based on M2PASCL consume little more power in comparison to NAND gate based on 2PASCL but M2PASCL based circuits have lesser propagation delay and are more robust due to reduction of floating node problem associated with 2PASCL. It is also observed NAND gate based on M2PASCL have least Power Delay Product which justifies its use for low power applications.

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