# Design of Pulse Detectors and Unsigned Sequential Multiplier using Reversible Logic

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## ABSTRACT
International Technology Roadmap for Semiconductors (ITRS) set a road map for More than Moore (MtM). Where device is scaled more than what the moore's law predicts. This MtM scaling will leads to substantially large design in the future and also huge power dissipation due to irreversible logic computation. Since applying low power technique has become tedious and time consuming. The solution is reversible logic computation. It plays an important role in power dissipation reduction. A novel design of reversible pulse detectors and sequential multiplier are proposed in this paper. As far as it is known, this is the first attempt to apply reversible logic to Pulse detectors and sequential multiplier. This paper also proposed a new reversible gate which can be used as full adder or full subtractor.

## Keywords
Low power VLSI, Reversible logic, Reversible pulse detectors, Reversible full adder or full subtractor, Reversible sequentail multiplier.

## 1. INTRODUCTION
Today's integrated circuits capacity has reached more than billion of logic gates and incorporate more number of functionalities than ever before. Reduction of power dissipation remains one of the major goals in the VLSI world for many years.

In early 1960's R. Landuer demonstrated energy dissipation due to information lost in the irreversible logic hardware computation, regardless of the realization techniques [1] and also proved that the loss of each one bit of information in irreversible logic computation dissipates at least KTln2 joules of energy in term of heat, where k is Boltzman's constant and T is the absolute temperature at which operation is carried out [1]. Bennett verified that reversible logic computation have theoretically dissipates zero internal power, since there is no loss of information [2]. The application of reversible logic is quantum computation [3], optical computing [4], ultra low power CMOS design [5] and non-technology [6].

Even though some significant work ([7] – [12], [14]) has been already done in the field of reversible sequential logic design. In this paper, we proposed a novel concept in reversible sequential design which includes pulse detectors and sequential multiplier.


**Fig. 1 Block diagram of Feynman gate**

Rest of the paper is organized as follows. Section II presents the idea of basic and necessary reversible logic gates used in this work. Section III introduces the details about the proposed reversible gate. Section IV provides the optimized reversible full adder and full subtractor using proposed reversible gate. Section V explains the design of reversible pulse detectors. Section VI explains the detail design of reversible registers, shift registers and parallel adder. Section VI explains the design of reversible unsigned sequential multiplier. Section VII review the result obtained from this work. Section VIII concludes this work.

## 2. REVERSIBLE LOGIC GATES
This section describes the reversible logic gates that are being used in the design.

Fig. 1 shows a Feynman Gate [13]. Feynman Gate (FG) is a basic reversible gate having two inputs and two outputs. It can be used as Ex-or gate and copying gate. This gate can be used for duplication of the required output due to fan-out is not allowed in reversible logic Design.

Fig. 2 shows Fredkin Gate [14]. Fredkin Gate (FRG) is a basic reversible gate having there inputs and there outputs. This is the most widely used reversible gate. This gate can be used as two input AND/OR gate and 2:1 multiplexer etc.

Fig. 3 shows Sayem Gate [15]. Sayem Gate (SG) is a reversible gate having four inputs and four outputs. A single Sayem Gate can be used as a D-latch.

Fig. 4 shows realization of D-latch using single sayem gate [15], with the help of pulse detector D-latch can be converted as D-flipflop. Because flipflops are the basic building block of complex sequential circuit such as register, shift register and sequential multiplier in this work.

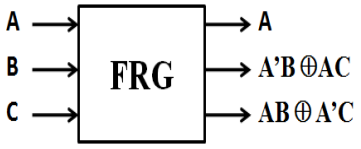


**Fig. 2 Block diagram of Fredkin gate**

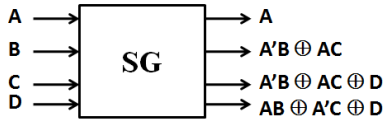


**Fig 3 Block diagram of Sayem gate**

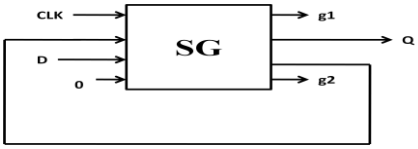


**Fig 4 Reversible clocked D flip flop**

## 3. PROPOSED REVERSIBLE GATE

We have proposed a new reversible gate named NG Gate. This is a four inputs and four outputs reversible gate. The block diagram of the proposed reversible gate is as shown in Fig. 5. Its corresponding Truth Table is shown in Table I. From the truth table we can verify that the input and output vectors are unique and also one to one mapping between them, which satisfies the condition of reversibility.

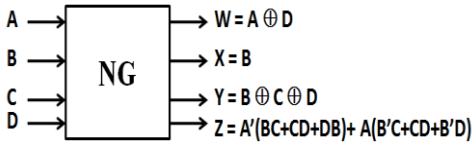


**Fig. 5 Block diagram of proposed reversible RGB gate**

**Table I Truth Table of the Proposed Reversible Gate**

| INPUT | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **W** | **X** | **Y** | **Z** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **1** | **1** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** | **1** |
| **1** | **0** | **1** | **1** | **0** | **0** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **1** | **1** | **0** |
| **1** | **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **0** | **1** | **1** | **1** |

## 4. PROPOSED REVERSIBLE FULL ADDER AND FULL SUBTRACTOR USING NG GATE

Addition and subtraction are the two most commonly used arithmetic operations. Multiplication and division can be done using the processes of repeated addition and subtraction respectively. The full adder and full subtractor are the basic building block of all hardware used to perform the arithmetic operations on binary numbers.

The proposed NG gate can be used as a full adder or full subtractor with the control input A. if A = 0 then NG gate act like a full adder that performs the addition of three binary digits. It has four inputs 0, A, B, C and four outputs g1, g2, X and Y. where X and Y are sum and carry respectively, produced by addition of three input bits A, B and C. The G1 and G2 are garbage outputs as shown in Fig. 6.

$$X = \text{sum} = (A \oplus B) \oplus C$$

$$Y = \text{carry} = AB + C\,(A \oplus B)$$

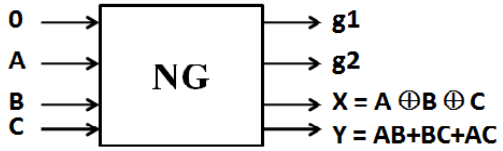


**Fig. 6 Reversible proposed full adder**

If A = 1 then NG gate act like a full subtractor that performer the subtraction of three binary digits. It has four inputs 1, A, B, C and four outputs g1, g2, X, Y. where X and Y are difference and borrow, produced by subtraction of three input bits A, B and C. The G1 and G2 are garbage outputs as shown in Fig. 7.

$$X = \text{Difference} = (A \oplus B) \oplus C$$

$$Y = \text{Borrow} = A'B + C\,(A \oplus B)'$$

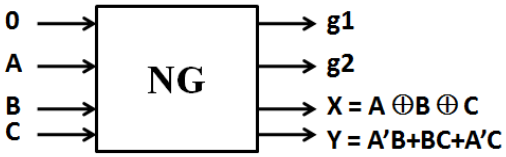


**Fig 7 Reversible proposed full subtractor**

## 5. PROPOSED REVERSIBLE PULSE DETECTORS

A flip-flop is a latch circuits with a pulse detector circuit connected to the enable input, so that it is enabled only for a moment on the rising and/or falling edge of a clock pulse.

### 5.1 Conventional positive and negative edge detector

The conventional positive edge detector is as shown Fig. 8. The inverter delay #tp determines width of the output pulse. The corresponding waveform is as shown in Fig. 9.

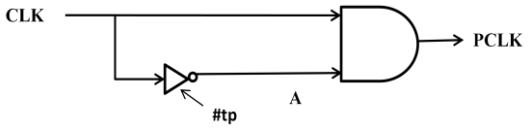


**Fig 8. Conventional positive edge detector**

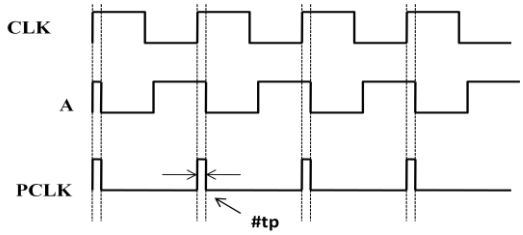


**Fig. 9 Waveform of positive edge detector**

The conventional negative edge detector is as shown Fig. 10. The inverter delay #tp determines width of the output pulse. The corresponding waveform is as shown in Fig. 11.

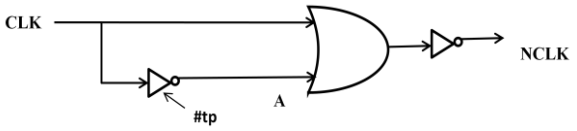


**Fig. 10 Conventional negative edge detector**

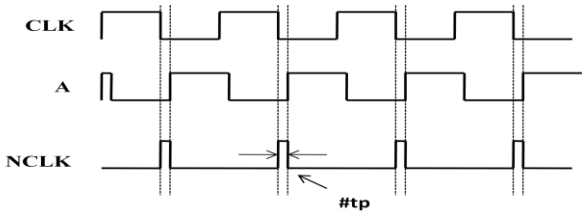


Fig. 11 Waveform of negative edge detector

## 5.2 Reversible Positive and Negative Edge Detector

The fredkin gate (FRG) with two inverters can be used as both positive and negative edge detectors.

The Fig. 12 shows the realization of fredkin gate as a AND gate and OR gate.


**Fig. 12 Proposed AND and OR gate using FRG gate**

The Fig. 13 shows realization of positive and negative edge detector using fredkin gate.

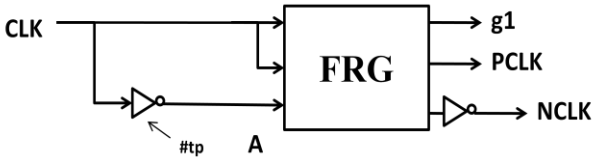


**Fig. 13 Proposed reversible positive and negative edge detector**

Where PCLK is the output of positive edge detector and NCLK is the output of negative edge detector, g1 is the garbage output. The #tp determines the output pulse width.

## 5.3 Conventional Dual Edge Detector

The conventional dual edge detector is as shown Fig. 14. The inverter delay #tp determines width of the output pulse. The corresponding waveform is shown in Fig. 15.

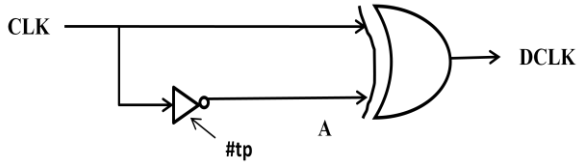


**Fig. 14 Conventional dual edge detector**

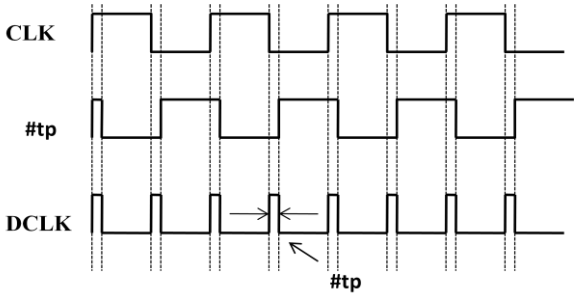


**Fig. 15 Waveform of dual edge detector**

## 5.4 Reversible Dual Edge Detector

The Fig.16 shows the realization of dual edge detector using one feynman gate and inverter.

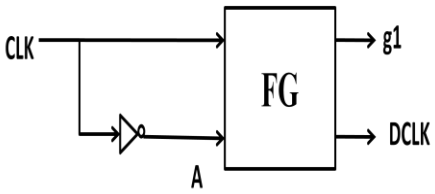


**Fig. 16 proposed reversible dual edge detector**

# 6. PROPOSED REVERSIBLE REGISTER, SHIFT REGISTER AND PARALLEL ADDER

## 6.1 Design of 4-Bit Reversible Register

The four-bit reversible register can be constructed by array of four reversible clocked D flip-flops as shown in Fig. 17.

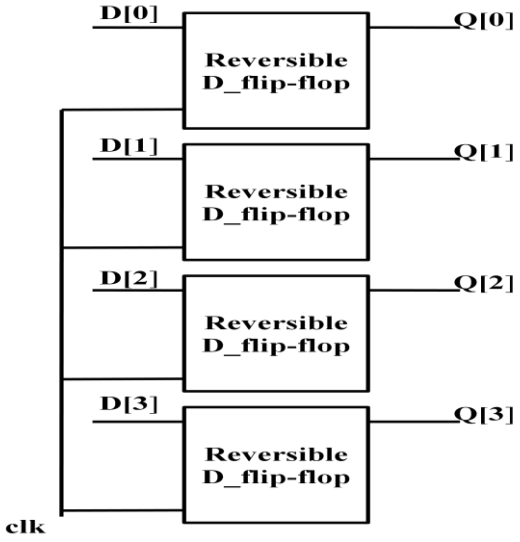


**Fig. 17 Proposed reversible 4-bit register**

The circuit symbol of four-bit reversible register as shown in Fig. 18.

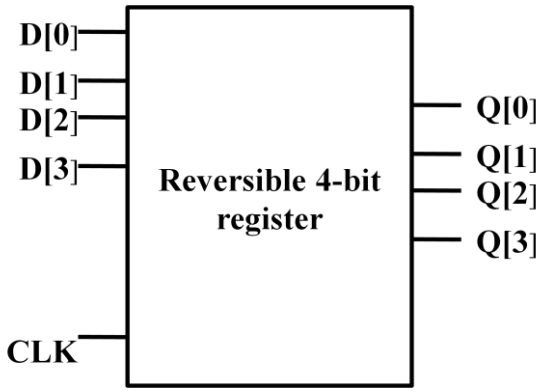


**Fig. 18 Symbol of reversible 4-bit register**

## 6.2 Design of 4-Bit Reversible PISO Shift Registers

PISO shift register takes the data from parallel inputs and shifts it to the next flip-flop when the register is clocked [16]. Fig. 19 shows the reversible implementation of four-bit PISO shift register using four reversible clocked D flip-flops and four Fredkin gates. Fredkin gate is used as multiplier with an enable signal as load. It decides loading the data into register by serially or parallel depending on the enable signal. When enable signal Load is high, the inputs D[0], D[1], D[2] and D[3] are loaded in parallel into the register. Again when enable signal Load is low, the Q output of the flip-flop is shifted to the right by means of Fredkin gate.

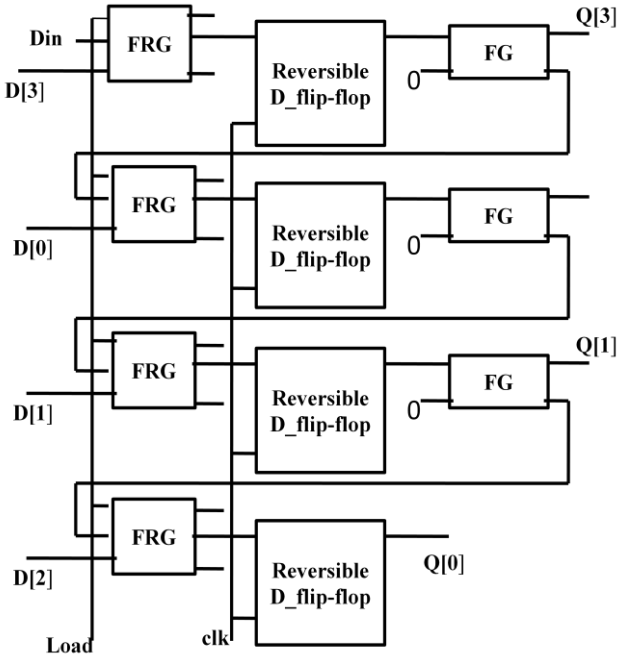


Fig. 19 Proposed reversible shift register (PISO)

The circuit symbol of four-bit reversible shift register with parallel in and serial out (PISO) as shown in Fig. 20.

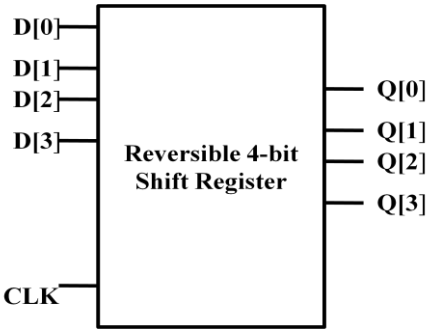


Fig. 20 Symbol of proposed reversible shift register (PISO)

## 6.3 Design of 3-Bit Reversible SIPO Shift Registers

A basic three-bit reversible shift register can be constructed using three reversible clocked D-flip-flops and two feynman gates , as shown in Fig. 21. The operation of the circuit is as follows. The input data is then applied sequentially to the Din input of the first flip-flop on the left. During each clock pulse, one bit is transmitted from left to right. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. Three-bit Reversible Shift Register (SIPO) as shown in Fig. 21.

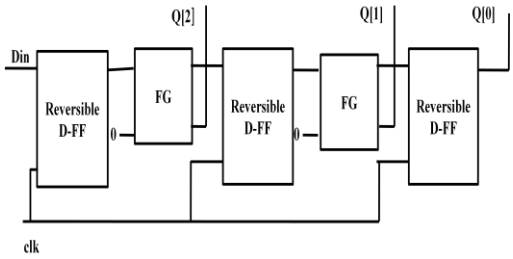


**Fig. 21 Proposed reversible shift register (SIPO)**

The circuit symbol of three-bit reversible shift register with serial in and parallel out (SIPO) as shown in Fig. 22.


**Fig. 22 Symbol of proposed reversible shift register (SIPO)**

## 6.4 Design of 4-Bit Reversible Parallel Adder

The four-bit parallel adder can be constructed by cascading four reversible full adders as shown in Fig. 23.

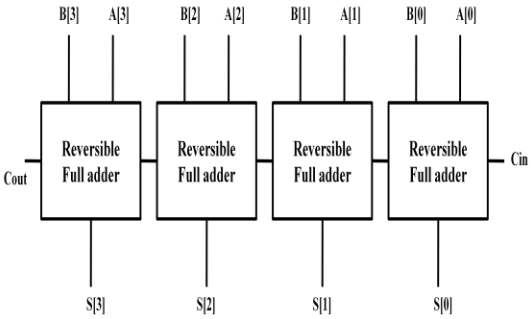


**Fig. 23 Proposed reversible 4-bit parallel adder**

The circuit symbol of four-bit reversible parallel adder as shown in Fig. 24.

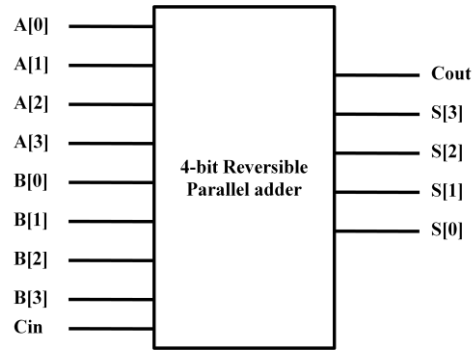


**Fig. 24 Symbol of proposed reversible 4-bit parallel adder**

## 6.5 Design of 4-Bit Reversible Unsigned Sequential Multiplier

The circuit diagram of four-bit reversible unsigned sequential multiplier as shown in Fig. 25. Let us consider X[3:0] and Y[3:0] are 4-bit multiplicand and multiplier respectively. In Fig. 25, construction of a multiplier for two 4-bit operands containing just one adder that adds successive partial products over successive clock cycles [16]. The final product is 8 bits. 4 X 4 multiply over 4 clock cycles, using one adder. Four-bit reversible shift register with parallel in and serial out (PISO) for multiplier bits .Three-bit reversible shift register with serial in and parallel out (SIPO) for LSBs of accumulated product.

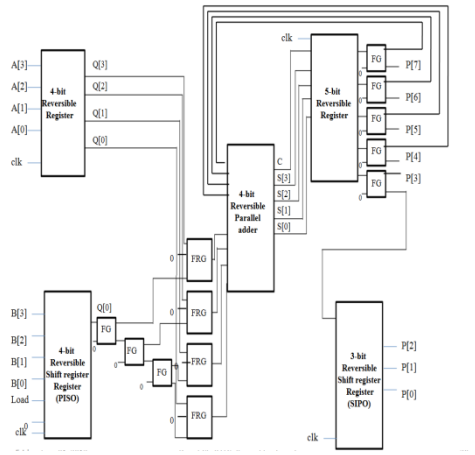


**Fig. 25 Proposed reversible 4-bit unsigned sequential multiplier**

## 7. RESULTS

The number of gates, garbage outputs, constant inputs and delay for designing proposed N-bit unsigned sequential multiplier is as shown in table II.

**Table Ii Parameters Required for Designing N-Bit Unsigned Sequential Multiplier**

| COMPONENTS | NO. OF GATES | NO.OF CONSTANT INPUTS | NO. OF GARBAGE OUTPUTS | DELAY |
|---|---|---|---|---|
| **N BIT REGISTER** | N | N | 2N | N |
| **(N + 1) BIT REGISTER** | N+1 | N+1 | 2N+2 | N+1 |
| **N BIT SHIFT REGISTER (PISO)** | 2N | N | 4N | 2N |
| **(N - 1) BIT REGISTER** | 2N-3 | 2N-3 | 2N-2 | 2N-3 |
| **N BIT PARALLEL ADDER** | N | N | 2N | N |
| **TOTALS** | **7N-2** | **6N-2** | **12N** | **7N-2** |

From this table, N-bit unsigned multiplier parameters are derived shown in table III. Also shown that number of gates,

number of garbage outputs, number of constant inputs and delay for corresponding (4, 8, 16, 32, 64-bit) reversible unsigned sequential multiplier.

**Table Iii Components Required for N-Bit Unsigned Sequential Multiplier**

| No. of bits | No of gates | No of constraint inputs | No of garbage output | Delay |
|---|---|---|---|---|
| **4-bit** | 26 | 22 | 48 | 26 |
| **8-bit** | 54 | 46 | 96 | 54 |
| **16-bit** | 110 | 94 | 192 | 110 |
| **32-bit** | 222 | 190 | 384 | 222 |
| **64-bit** | 446 | 382 | 768 | 446 |

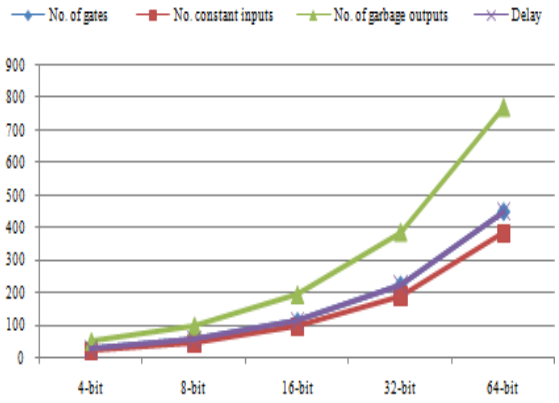


**Fig. 26 Variation of reversible parameter vs variation of bits**

Fig. 26 shows the graph of parameter variation for (4, 8, 16, 32, and 64) bit reversible unsigned sequential multiplier.

## 8. CONCLUSION

In this paper, the reversible realization of pulse detectors and 4-bit reversible unsigned sequential multiplier designed by using proposed reversible NG gate and existing ones. As far as it is known, this is the first attempt to apply reversible logic to pulse detectors and unsigned sequential multiplier design in the literature. We also proposed a new reversible NG gate. This can be used as full adder or full subtractor. The proposed unsigned sequential multiplier design has the application in building reversible ALU, reversible processor etc. This work forms an important move in building complex reversible sequential circuits for quantum computation.

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