Design and Analysis of Dual Edge Triggered D Flip-Flop

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ABSTRACT
Power consumption and energy efficiency plays a vital role in sequential circuit design. Clock gating is a technique that is used to reduce the dynamic power consumption of idle modules. Usage of Dual Edge Triggered Flip-flop (DETFF) is an efficient technique since it consumes half the clock frequency and less power than Single Edge Triggered Flip-flops (SETFF's). Integrating clock gating technique with DETFF reduces the power consumption further, but it leads to asynchronous data sampling problem (change in output between clock edges). In this paper, two methods have been used to eradicate asynchronous data sampling problem and their power analysis has been estimated. In order to reduce the power consumption further, a new design has been proposed for DETFF. Based on the new design, two methods have been implemented using Tanner EDA tool. The performance comparison is made using CMOS 0.18µm technology.

Keywords
Asynchronous data sampling, Clock gating

1. INTRODUCTION
Power efficiency and energy savings are considered to be vital issues for designers. Normally, high-performance chips will have high clock frequency, which leads to high power consumption. Therefore, less power consuming designs are needed. The major source of power consumption in a sequential circuit is clock tree and the timing components.

Flip-flops are the commonly used component in the digital system and are used in computational circuits and registers in pipeline structures to store the data for additional processing. The SETFF is usually designed by cascading two oppositely phased latches and is active on any one of the clock edges(either on the rising edge or on the falling edge). Hence certain clock edges are left idle. To use the idle clock edge, DETFF have been introduced. These flip-flops can operate at half the clock frequency and also maintains the same data throughput as of SETFF's. In other words, the DETFF operates on a lower clock frequency than the SETFF thereby increasing the performance.

Usually flip-flops [2] operate on the active edge of the clock signal, but at times this is not required since the data value is not changed. Timing components such as latches and flip-flops usually consume high power. An efficient technique to reduce the power consumption is by preventing transitions made by the clock. Hence clock-gating technique has been

developed to disable the clock switching when it is not required and when there is no change on the input to the flip-flop. By incorporating clock gating technique with DETFF, power consumption can be reduced further. Though the dynamic power consumption gets reduced, asynchronous data sampling problem is introduced, that is change in output between clock edges. This can be done in two levels, circuit and behavior [3] level.

Clock gating [4] is the technique in which logic power, clock power, signal power and IO power can be reduced. There are certain considerations for clock gating under which the clock supplied to the sequential circuits must be switched off. Hence power can be saved by decreasing the load in the clock network. This can be done by reducing the switching capacitance in the clock network. A design that dissipates minimum static and dynamic power is said to be a low power design. Since clock is made as one of the inputs to the sequential circuits, it consumes high static and dynamic power.

There are two types of DETFF's: 1) Latch-Mux and 2) Pulsed Latches. The Latch-Mux [6] consists of two latches connected in parallel to each other and they are transparent on opposite levels of the clock. This style can be subcategorized into: (a) transmission gate (or pass transistor) Latch-Mux or (b) C^2MOS Latch-Mux. In the Pulsed Latches type, the pulse generator responds both on rising and falling edges and so the latch samples an input for every clock edge. In the Pulsed Latches type, the pulse width should be as long as possible in order to satisfy all the timing requirements.

Power dissipation on the clock tree [1] can be reduced by applying certain clock gating techniques. Clock-gating technique has been prolonged to use with DETFFs in order to reduce the power consumption further. Though the power consumption gets reduced, combining clock-gating and double edge-triggered techniques might create an asynchronous sampling issue.

Gated circuits are controlled by the internal clock signals in a clock-gated system. Global clock signal and internal clock signal is separated from each other during gated periods. If the global clock signal and internal clock signal are not in phase and when the clock signal is made inactive, switching takes place between the two signals to synchronize with each other.

Hence, asynchronous data sampling issue [6] occurs when both these clock signals does not synchronize with each other. It is indicated by the change in output between the two clock edges. Asynchronous data sampling issue will not be present always. There are certain scenarios under which this issue occurs.

Asynchronous data sampling issue is addressed using three gating circuits and three approaches are designed to eradicate the issue. In the first two approaches the connection between the internal and the global clock starts only when they are in phase with each other. In the third approach, internal clock and the global clock are synchronized with each other. Hence asynchronous data sampling issue can be avoided.

In order to reduce the power consumption further, a new design has been proposed. Though several contributions have

been made to design DETFF's, there arises certain circumstance to reduce the power consumption of DETFF's further. The proposed high performance DETFF consumes less average power than the other designs. Hence it is very well suitable for high performance applications.

The paper is organized as follows. Section II describes the basics of clock gated D flip-flop. Section III describes the analysis of asynchronous data sampling issue. Section IV explains the methods to avoid asynchronous sampling issue. Then, the proposed design is explained in Section V. Simulation results and power analysis of the existing and proposed flip-flop is shown in Section VI. Finally, the work is summarized in Section VII.

2. CLOCK GATED D FLIP-FLOP

An assumption is made that all transitions on Q (output data) should be synchronized with an active clock edge. Data miscommunication errors might be caused due to asynchronous data sampling. The CG (clock gating control) signal is activated when there is a transition in D (input data). Flip-flop is triggered when internal clock pulse is given.

The C (internal gated clock) signal maintains its value instead of generating an active edge in the gating mode. C changes after the transition on CLK in the non-gating mode. Asynchronous data transition may occur, if D changes (i.e., it enters the non-gating mode) while C is not equal to CLK and is shown as spikes at the output.

There are certain conditions for the occurrence of asynchronous data sampling problem and it is shown in Table 1.

Table 1. Condition for Asynchronous Data Sampling

Designs	Condition for asynchronous data sampling
G_DETFF	D changes when CLK ≠ C
DET_SRSFF	D changes when CLK = 0
DHSCGFF	D changes when CLK = 0

3. ANALYSIS OF ASYNCHRONOUS DATA SAMPLING IN FLIP-FLOPS

3.1 Asynchronous Sampling in the Gated Double Edge-Triggered Flip-Flop with Transmission Gate (G_DETFF)

The flip-flop is built with the Latch-Mux structure using transmission gates as in Fig 1. The two data paths are connected in parallel. The upper data path transmits data on the rising edge and the lower path transmits data on the falling edge. These two data paths alternatively monitor the input and provide the output, which means that the input is always preloaded into the flip-flop.

Instead of generating a pulse for every transition, the clock-gating part was designed to toggle C, whenever the data input is changed and also to eliminate power consumption for unnecessary transitions. During the gating periods, C preserves the last used value before being gated. When compared to other clock gating techniques, G_DETFF uses the clock signal in a more efficient way that is better suited for DETFF.

3.2 Asynchronous Sampling in Low Power Dual Edge Triggered State Retention Scan Flip-flop (DET_SRSFF)

Asynchronous data sampling issue is present in DET_SRSFF and its schematic diagram is shown in Fig 2. It comprises of a pulse generator and a static latch that has LFB (leakage feedback) to reduce leakage current.

According to the schematic of Fig 2, if there is a pulse during the latch mode when D=1, Q changes from 0 to 1. A pulse generator has been used to attain the double edge triggered capability and to integrate the clock-gating feature. The circuit operates normally for CG=0. Clock edges are detected using pulse generator by connecting a delay element with an XOR gate. This helps in generating a positive pulse for each clock edge.

Asynchronous data transition occurs in DET_SRSFF, when there is an input change while CLK equals 0. Because when there is a change in the input, clock signal is made inactive (de-asserted). Hence in DET_SRSFF, asynchronous data transition can be observed when there is an input change before a rising edge.

DET_SRSFF has no problem related to asynchronous sampling when input does not change or when changes before a falling edge. However, when input changes before a rising edge, an asynchronous pulse will be generated as soon as the gating signal is de-asserted. This extra pulse leads to the asynchronous transition that causes the timing issue within the Clock-Gated DETFF.

3.3 Asynchronous Sampling in the Double Edge-Triggered Half-Static Clock-Gated D-Type Flip-Flop (DHSCGFF)

In DHSCGFF, two flip-flops and a multiplexer are used. On comparing the value of D and Q, a clock gating signal is generated to control the signal path of the global clock to the internal clock.

The design is shown in Fig 3. The upper path transmits data only on the falling edge of Clock signal, while the lower path transmits data on the rising edge of C lock signal. The gated clock signal stays 0 when gated (inactive). So, if the input data gets changed when CLK=0 then the value of C will change to 1 immediately and $\tilde{C}$ will change to 0 and vice versa. Asynchronous data sampling is caused when asynchronous clock edge of C triggers the flip-flop. After each data transition, the gated signal C goes back to 0 and stays low until the next transition.

4. METHODS TO AVOID ADS

4.1 Method A

When the gating signal is de-asserted, connection establishes between CLK and C only when CLK=C, hence avoiding asynchronous data transition. In scheme1 shown in Fig 4, CLK signal is controlled by comparing D and Q. If D has changed since the last clock transition and is different from Q, then CLK will pass to the second comparator to compare with the C.

This CLK & C comparator controls the switch T2 between the C and CLK. The second comparator prevents the asynchronous sampling. Asynchronous sampling occurs when D changes when CLK differs from C. However, with the second CLK & C comparator, the switch T2 will stay OFF when CLK ≠ C and C will synchronize with CLK and it's shown in Fig 5.

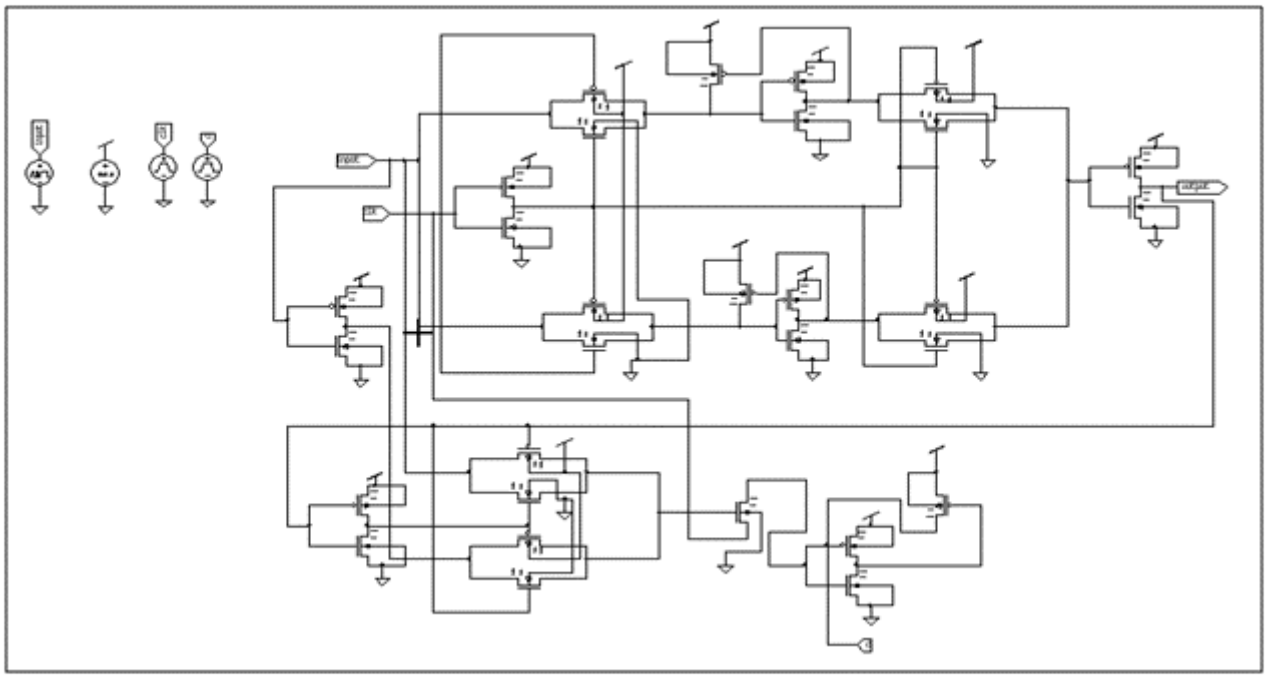


Fig 1: G_DETFF

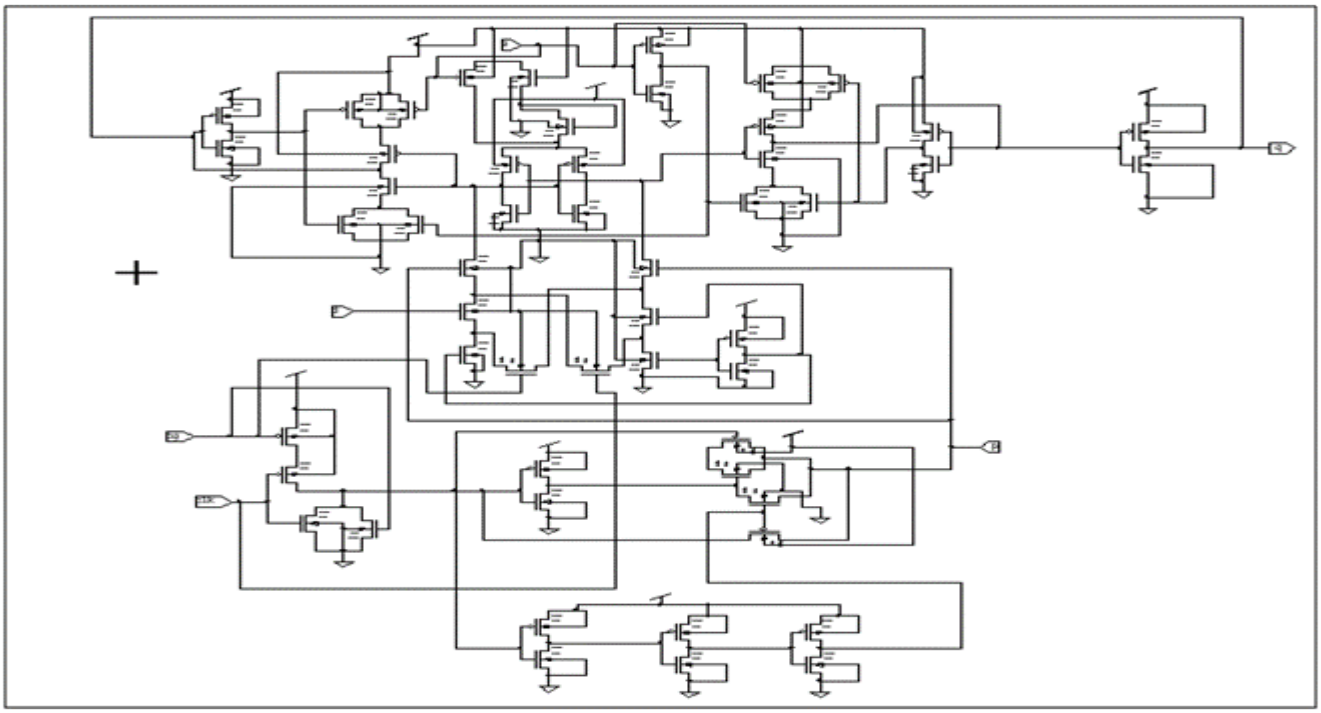


Fig 2: Dual-Edge Triggered State Retention Scan Flip-Flop

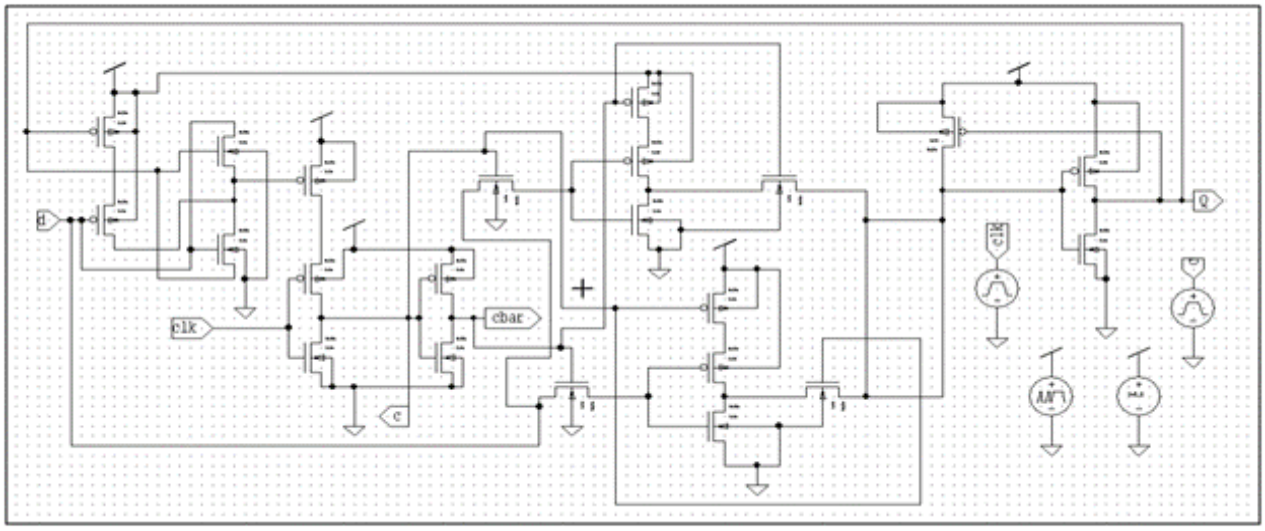


Fig 3: DHSCGFF Design

For Scheme 2, the asynchronous sampling is avoided by the following mechanism. The C normally stays at 0. When D changes while the CLK is 1 transistor P2, the one closer to CLK, will be turned OFF immediately and C will remain the same. When CLK goes back to 0 (a falling edge), P2 is ON and because of the delay element, P1 will stay ON for the time needed to trigger the flip-flop. This is shown in Fig 6.
time implementations. The benefit of Method B is that C only toggles once for every transition.

4.2 Method B

In Method B, whether D changes or not, the comparator's result is ready immediately and T1 gets generated at clock edges. So C and CLK are synchronized with each other and the asynchronous sampling is avoided. Method B has better performance on power consumption.

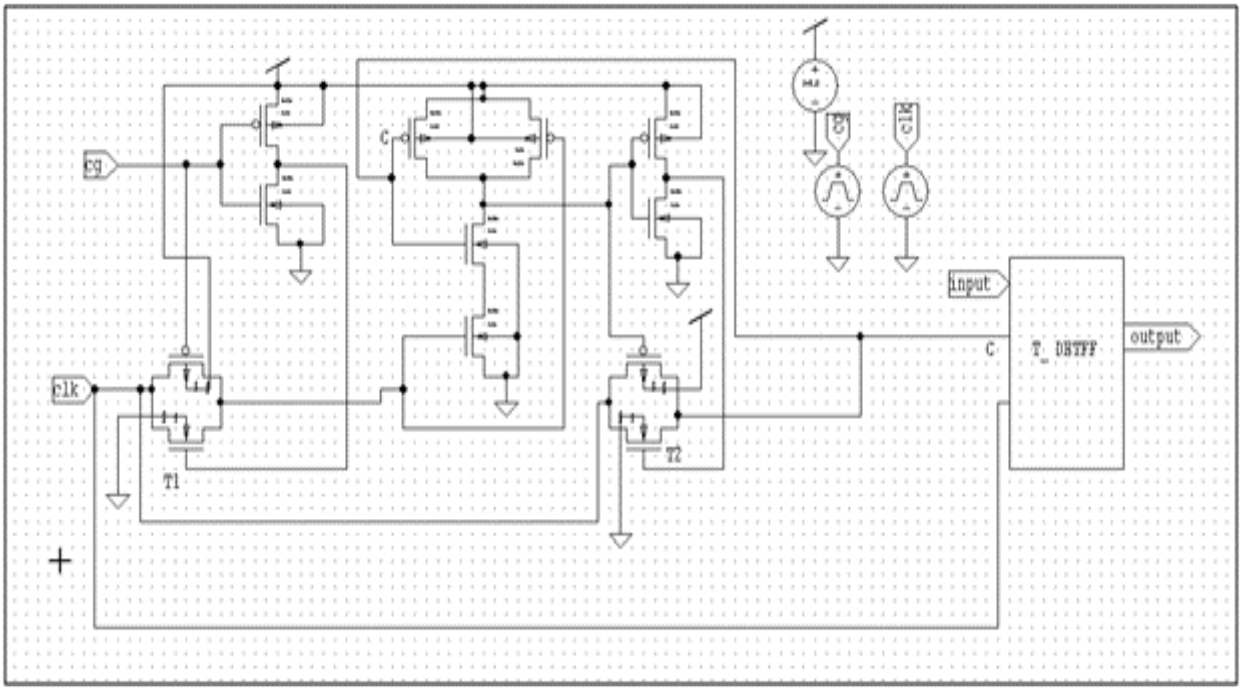


Fig 4: Scheme 1 of Method A

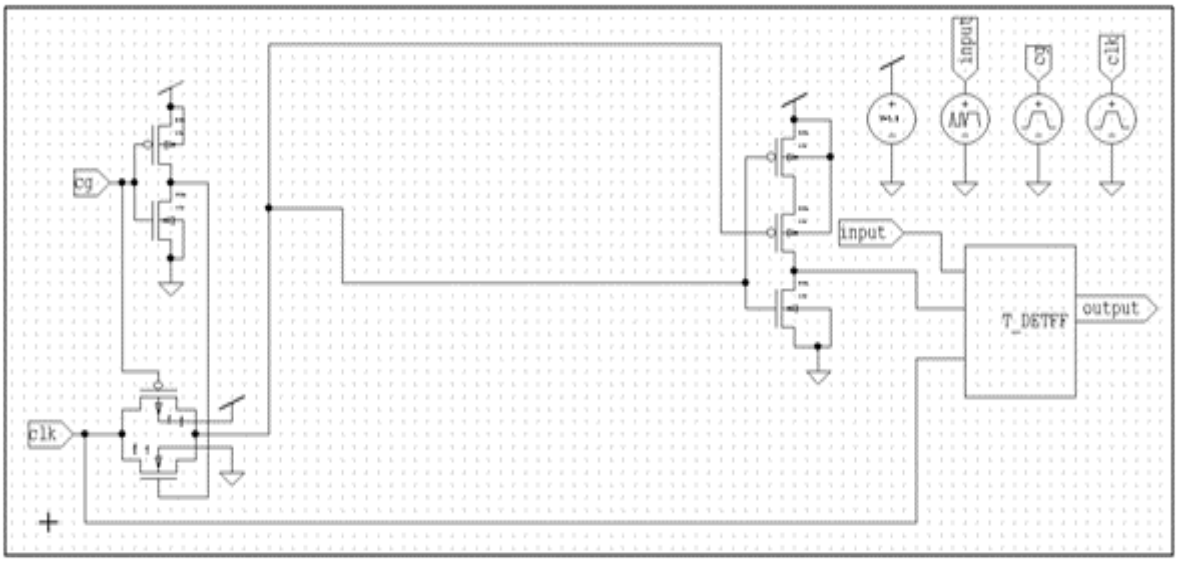


Fig 5: Scheme 2 of Method A

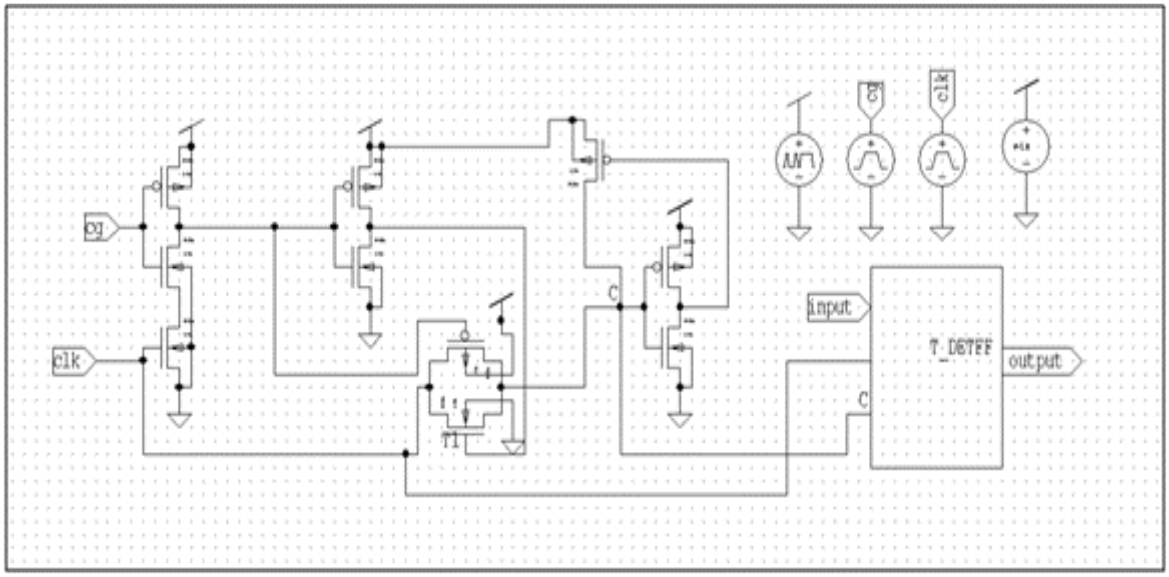


Fig 6: Scheme to implement Method B

5. PROPOSED DESIGN'S

In DETFF, the same throughput of SETFF can be achieved with half the clock frequency. Since DETFF's are edge sensitive devices, data is latched on anyone of the clock edges.

Though several contributions have been made to design DETFF's, there arises certain circumstance to reduce the power consumption of DETFF's further. A high performance DETFF is shown in Fig 7 and it consumes less power than the other designs. Hence the proposed DETFF is very well suitable for high performance applications.

When the gating signal is de-asserted, connection establishes between CLK and C only when CLK=C, hence avoiding asynchronous data transition. In scheme1 of Method A, CLK signal is controlled by comparing D and Q. If D has changed since the last clock transition and is different from Q, then CLK will pass to the second comparator to compare with the C and is shown in Fig 8.

For scheme 2 of Method A, C normally stays at 0. When D changes while the CLK is 1 transistor P2, the one closer to CLK, will be turned OFF immediately and C will remain the same. When CLK goes back to 0 (a falling edge), P2 is ON and because of the delay element, P1 will stay ON for the time needed to trigger the flip-flop and it is shown in Fig 9.

In Method B, whether D changes or not, the comparator's result is ready immediately and T1 gets generated at clock edges. So C and CLK are synchronized with each other and the asynchronous sampling is avoided and is shown in Fig 10.

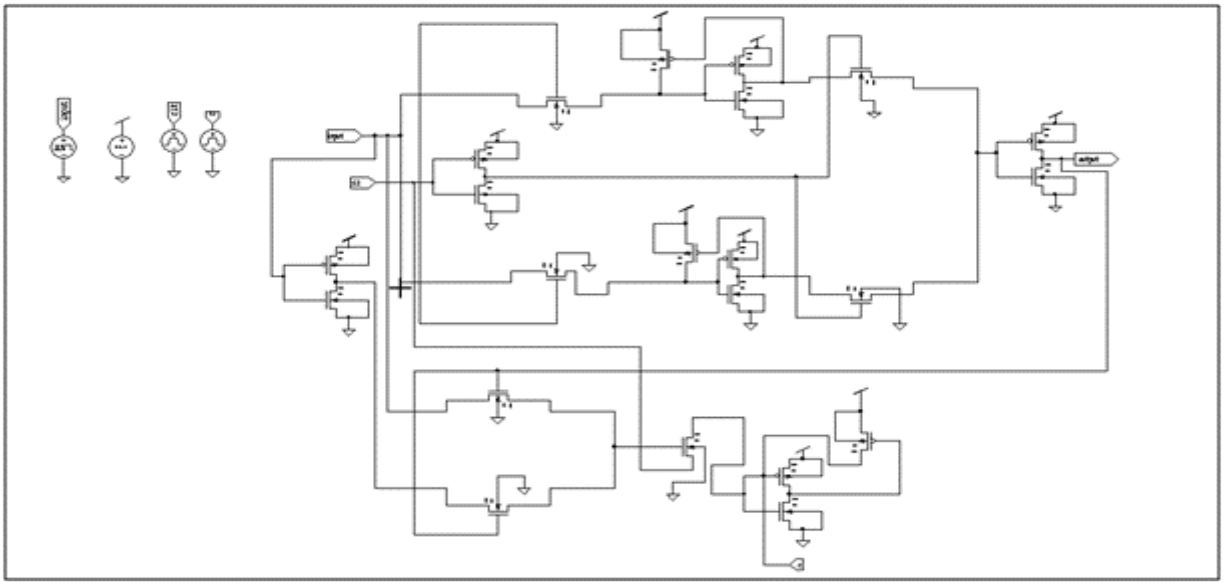


Fig 7: Pass Transistor Based DETFF

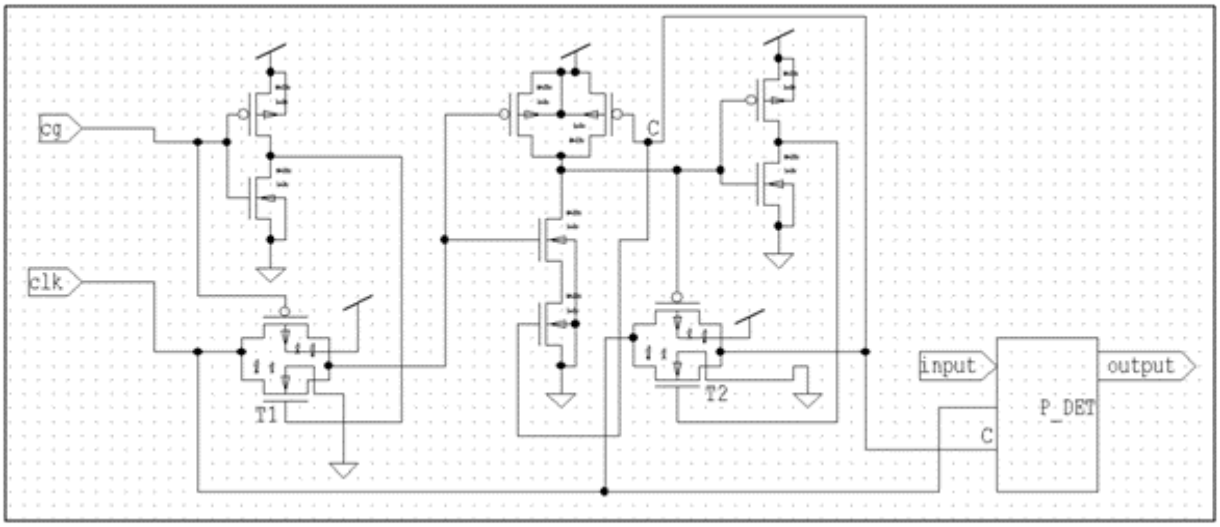


Fig 8: Scheme 1 of Method A 1

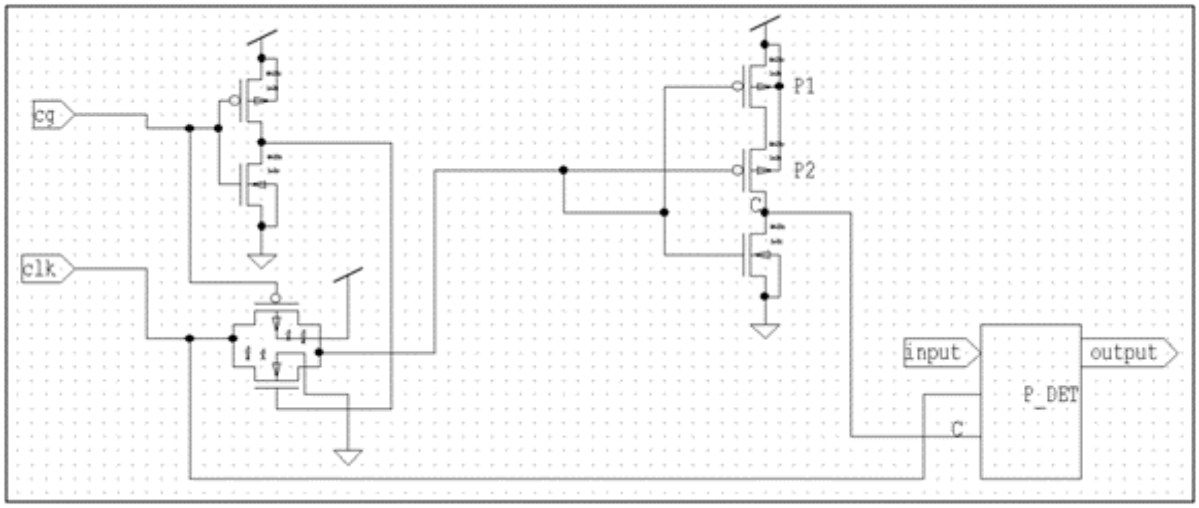


Fig 9: Scheme 2 of Method A 1

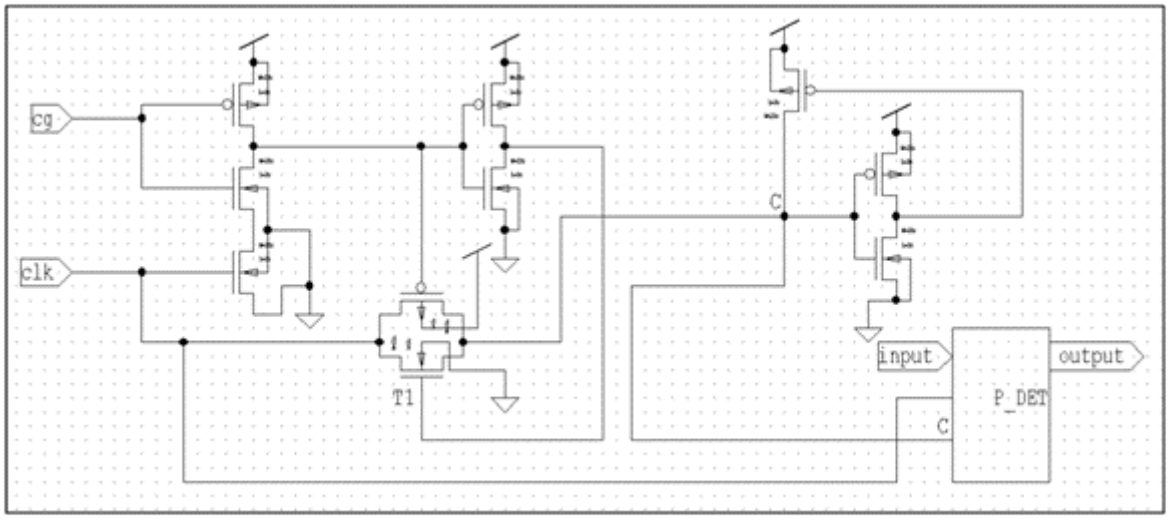


Fig 10: Scheme to implement Method B

6. SIMULATION RESULTS

The simulation results of G_DETFF, DHSCGFF, DET_SRSFF, Method A, Method B and the proposed designs are shown along with their waveforms. Simulation has been done using Tanner tool (S-EDIT) and the power results are shown. Power comparison of the existing and proposed flip-flop's are tabulated and shown.

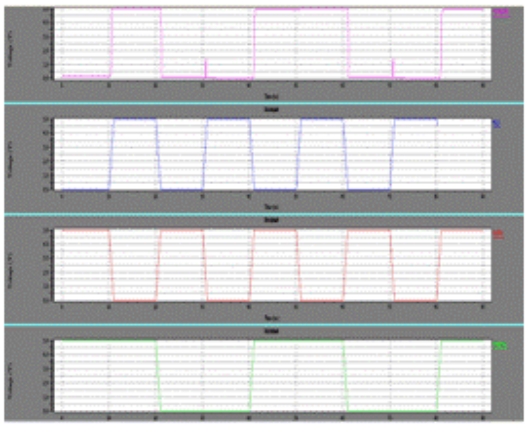


Fig 11: Waveform of Gated DETFF

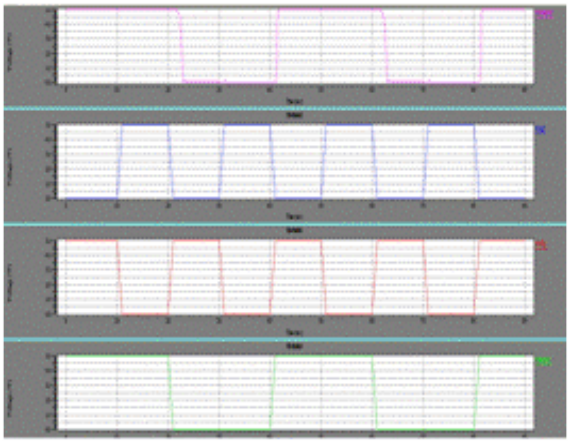


Fig 12: Waveform 1 of Method A

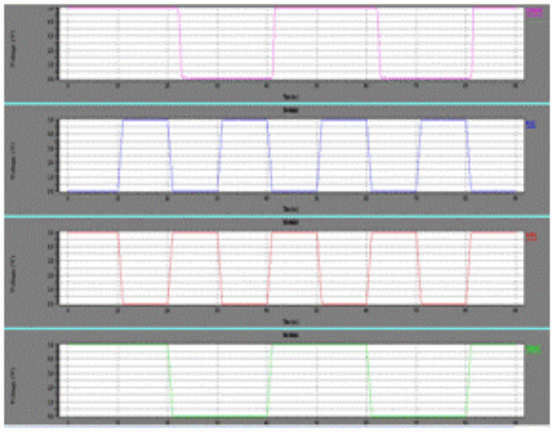


Fig 13: Waveform 2 of Method A

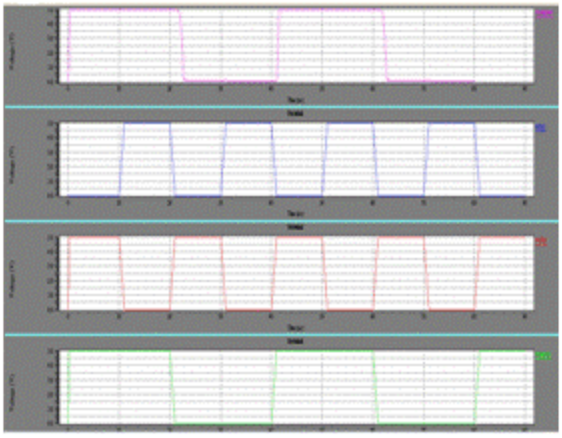


Fig 14: Waveform of Method B

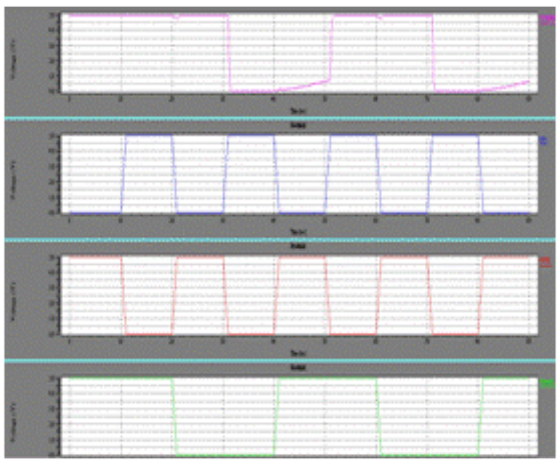


Fig 15: Waveform 1 of Proposed Method 1

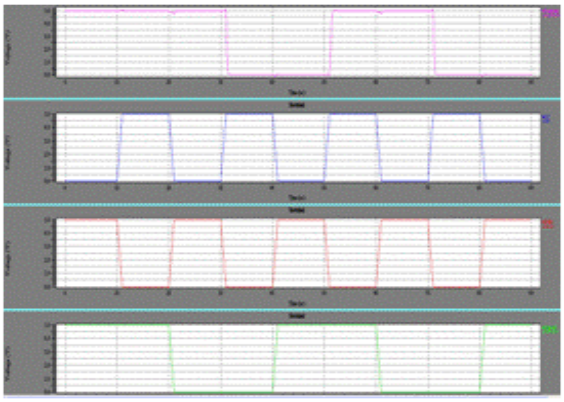


Fig 16: Waveform of Proposed Method 2

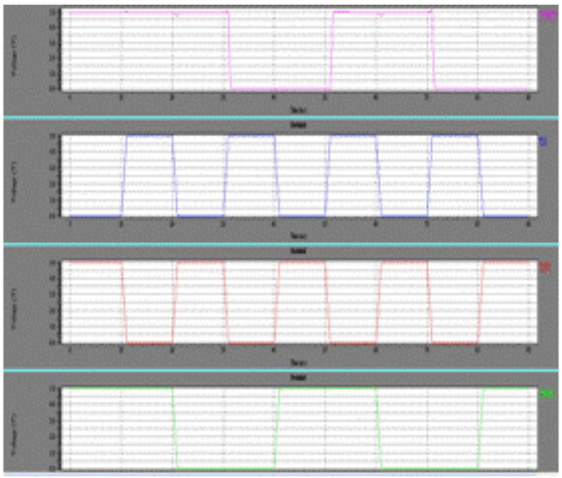


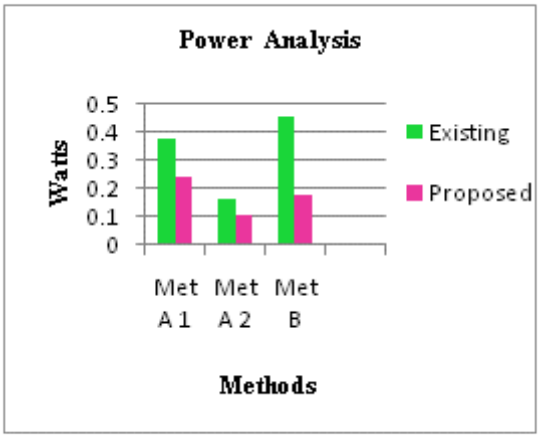
Fig 17: Waveform 2 of Proposed Method 1

The graphs shown denote the power and area analysis of the proposed designs. On comparing with the existing designs, the proposed design consumes low power and occupies less area.

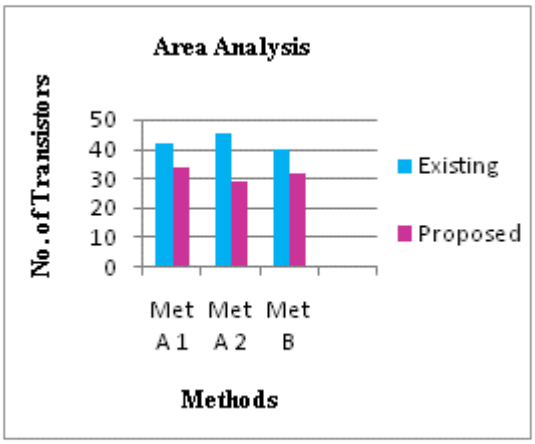
The following table shows the comparison of existing and the proposed designs. When compared to the existing methods, the proposed method consumes less power and area.

Table 2. Comparison of Existing and Proposed Designs

Type of Flip-flop	Maximum power (Watts)	No. of Transistors
G_DETFF	0.485	30
DHSCGFF	1.888	53
DET_SRSFF	0.545	22
Method A 1	0.38	42
Method A 2	0.162	45
Method B	0.46	40
Proposed Method A1	0.24	32
Proposed Method A 2	0.11	29
Proposed Method B	0.18	32



a) Power Analysis



b) Area Analysis

Fig 18: Comparison Graphs

7. CONCLUSION

Various power reduction techniques emerged as a result of high demand in mobile devices. DETFF is an efficient technique for power reduction, when used separately. When clock gating technique is integrated with DETFF, asynchronous data sampling problem arises at the output between two clock edges. This problem has been defined in detail and solutions were given to eradicate it. Three simple approaches were made to reduce the power consumed in DETFF's by eliminating the asynchronous data sampling issue. In order to reduce the power consumption further, a new design has been proposed and based on that, three designs were implemented using Tanner EDA tool.

8. REFERENCES

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