A Novel Analysis on Low-Power High-Performance Flip-Flops

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ABSTRACT

The fast growth of the power density in integrated circuits has made area and power dissipation as the vital design measures. In this paper, several different flip-flop topologies are analyzed and an area, power efficient flip-flop design is proposed. This design overcomes the power dissipation due to the large precharge node capacitance, with reduced number of transistors. The comparative power analysis and performance improvements indicate that the proposed design is suitable for high-performance digital designs where the area and power dissipation is of major concern. The simulation results are verified using tanner v7.0 tool. The performance comparisons are made using CMOS0.18μm technology.

General Terms

Flip-flops, low power, less transistors

Keywords

Precharge node capacitance, power dissipation, high-performance

1. INTRODUCTION

Over the past decade, power consumption of VLSI chips has been continuously increasing. The need for low-power design is becoming a vital parameter in high-performance digital systems. There are numerous techniques being encountered for the design of low power VLSI circuits. Low power has made an important note that power dissipation has a consideration on performance and area. Static power and Dynamic power being the main components determining the power consumption in CMOS circuits. In synchronous systems, high speed has been obtained using advanced pipelining techniques. In modern pipelined architectures, high speed demands a lower pipeline overhead. The overhead is the latency related with the pipeline elements, such as the flip-flops and latches. Latches and flip-flops form the basic components of a finite state machine and as memory elements for data path. The latches are level-sensitive D latches, while the flip-flops are edge-triggered D being widely used. The design methodology and area and timing requirements determine the choice of latches and flip-flops. Latches and flip-flips can be static or dynamic. A dynamic latch or flip-flop loses its content as time increases, while a static one retains its content regardless of elapse time. In the past few decades, lot of work has been done to improve the performance of the flip-flops.

Hybrid Latch Flip-Flop (HLFF) [1] and Semi Dynamic Flip-Flop (SDFF) [2] are assumed as the classic high-performance flip-flops. They consist of a hybrid architecture that includes the merits of dynamic and static structures. In addition, SDFF has a distinctive characteristic of incorporating logic very efficiently, reducing the pipeline overhead since the delay and area along with one or more logic stages of the flip-flop can be eliminated. Several hybrid flip-flop designs have been proposed in the past decade, to reduce power, delay, and area. Recent flip-flop architecture named Cross Charge Control Flip Flop (XCFF) [3], has some advantages over SDFF and HLFF in both power and speed. It reduces the precharge capacitance by means of using split-dynamic node, which causes the large power consumption in most of the existing designs. Some drawbacks of this structure include redundant power dissipation and large hold-time requirement. In the case of Dual Dynamic node hybrid Flip-Flop (DDFF), due to the feedback structure at the output node, the switching of data for more data patterns is inefficient. Also the power dissipation is higher when compared to the Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) based D Flip-Flop (DFF) design. These power efficient architectures avoid the problem of inefficient switching of data for more data patterns. But they have some of the drawbacks such as lower output swing and inefficient structure to embed the logic functions. In the proposed architecture, the inefficient switching of data for more data patterns is avoided by eliminating the feedback logic. It is well known that the feedback logic has the drawback of retaining the data of a specific logic. In addition to this, the proposed flip-flop has reduced number of transistors compared to the DDFF design.

The paper is divided as follows. Section 2 presents the analysis of flip-flop architectures and discusses the disadvantages of the existing flip-flop architectures and challenges in obtaining a better design. In Section 3, the proposed architecture and the power efficient architectures of flip-flop such as PTL and GDI are provided with the design and working principle. In Section I4, the results of various flip-flop topologies with power analysis are provided. Finally, Section 5, concludes with the improvements of the proposed flip-flop design over the existing modern high performance designs.

2. ANALYSIS OF EXISTING FLIP-FLOP ARCHITECTURES

A large number of flip-flops and latches have been designed in the past years. These can be divided into the static and dynamic design styles. The master slave designs, such as the transmission gate based master-slave flip-flop in [4] and the PowerPC 603 master-slave latch [4] comes under static design style. They have lower power dissipation and low clock-to-output (CLK-Q) delay. In a synchronous system, the delay

overhead associated with the latches and flip-flop is given by the data-to-output (D-Q) delay rather than CLK-Q delay [5]. D-Q delay is the sum of CLK-Q delay and the setup-time of the flip-flop. But the static design mentioned has high D-Q delay due to their large positive setup time and are affected by flow-through resulting from CLK overlap. PowerPC 603 (Fig. 1) is one of the most efficient classic static structures. Its advantages include a low-power keeper structure and a low latency direct path. The disadvantage of this design includes large D-Q delay, the large data and CLK node capacitances. Apart from all these shortcomings, static designs provide low power solution when the speed is not of primary importance.
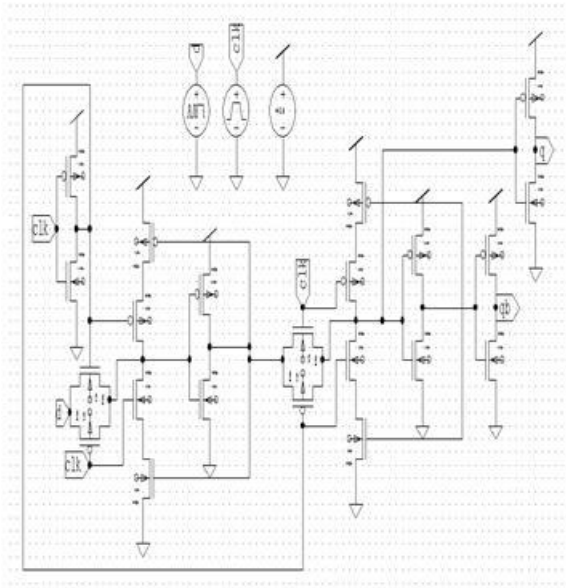

Fig. 1: Power PC 603
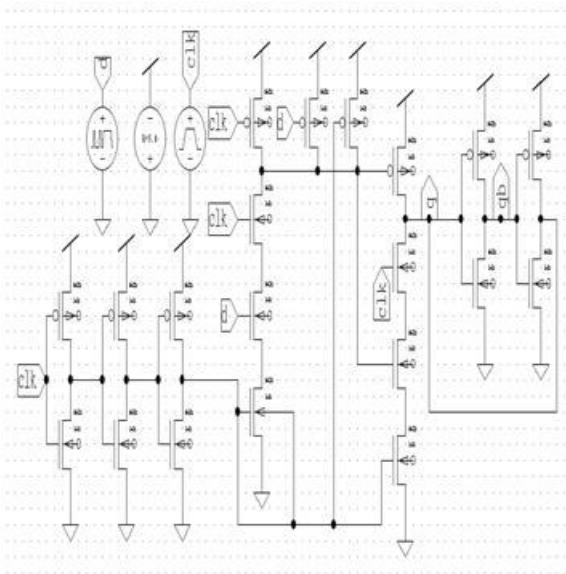
Fig. 2: Hybrid latch flip-flop

The second category, the dynamic flip-flops includes the modern high performance flip-flops [1], [6]. It includes dynamic designs as well as pseudo-dynamic structures. The latter, has an internal precharge structure and a static output, with higher performance improvements. They are called the semi-dynamic or hybrid structures, since they consist of a

dynamic frontend and a static output. HLFF (Fig. 2) and SDFF (Fig. 3) come under this category. They have the benefit of CLK overlap to perform the latching operation. SDFF is the fastest classic hybrid structure, but has high power consumption due to large CLK load and the large precharge capacitance. HLFF is not the fastest but has a lower power consumption compared to the SDFF. The reason is the longer stack of nMOS transistors at the output node (Fig. 2). It also has large positive hold time requirement making the integration of HLFF to complex circuits a difficult process. The major sources of power dissipation in the conventional semi-dynamic designs include redundant data transitions and large precharge capacitance. Many efforts have been made to minimize the redundant data transitions in the flip-flops [4].
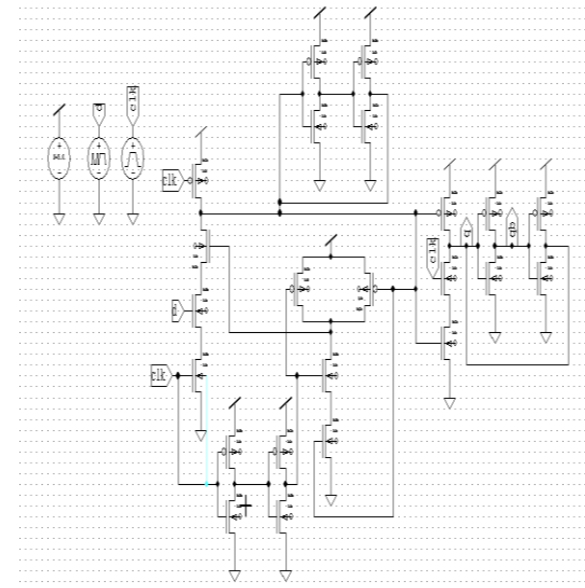

Fig. 3: Semi-dynamic flip-flop

The conditional data mapping flip-flop (CDMFF) shown in Fig. 4 is one of the most efficient design with a feedback structure to conditionally feed the data to the flip-flop. This eradicates the unwanted transitions when a redundant event is encountered. Due to no added transistors in the pull-down nMOS stack, the speed is not much degraded. But due to the three stacked nMOS transistors at the output node and the presence of conditional structures in the critical path tends to increase the hold time requirement and D-Q delay of the flip-flop. Also, this makes the flip-flop bulky and causes an increase in power dissipation. The large precharge-capacitance results when both the output pull-up and the pull-down transistor are driven by the precharge node at a time. These transistors drive large output loads, contributing more capacitance at the precharge node. This shortcoming was considered in the design of XCFF (Fig. 5).

The XCFF reduces the power dissipation in such a way that the pull-up and pull-down transistors at the output side are driven separately as shown in Fig. 5. Due to the switching of one of the two dynamic nodes during one CLK cycle, the total power consumption is reduced without speed degradation and it has lower CLK driving load. The major drawbacks of this design are the redundant precharge and the effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design. The new dual dynamic flip-flop (DDFF) [7] eliminates the drawbacks of XCFF. The new design is free from unwanted transitions resulting when the data input is stable at zero. DDFF presents

a speed, area, and power efficient method to reduce the pipeline overhead. The Fig. 6 shows the DDFF architecture. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when CLK is low. Though the DDFF avoids the problem of redundant data transition and precharge node, the area is still higher when compared to the popular and advanced low power circuit design techniques and the proposed DFF.
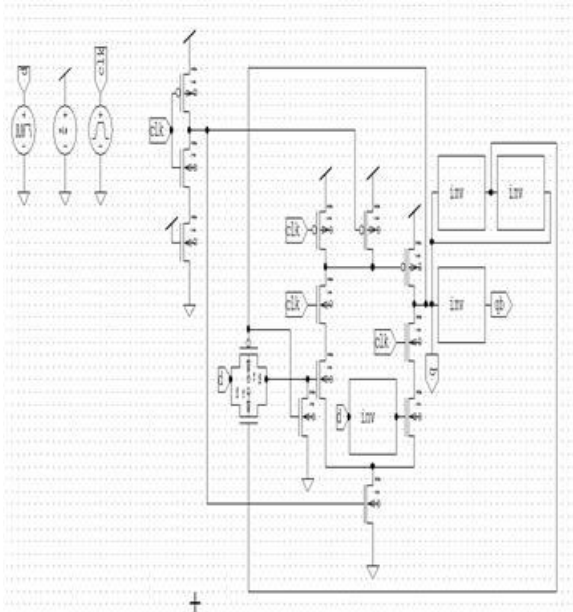
Fig. 4: Conditional data mapping flip-flop
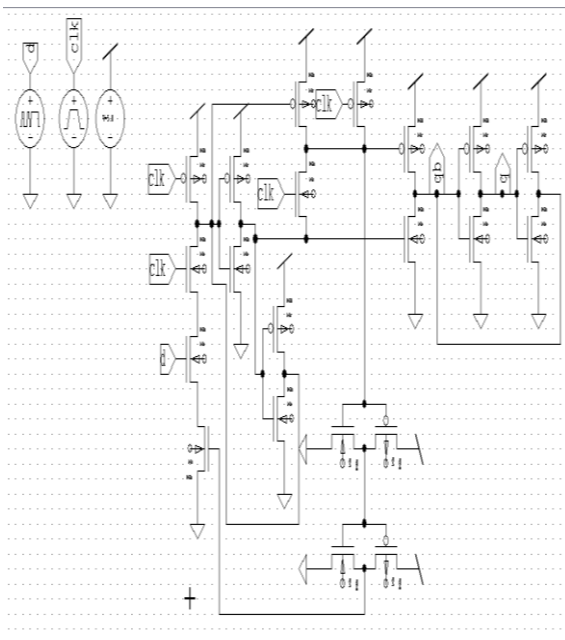
Fig. 5: Cross charge control flip-flop
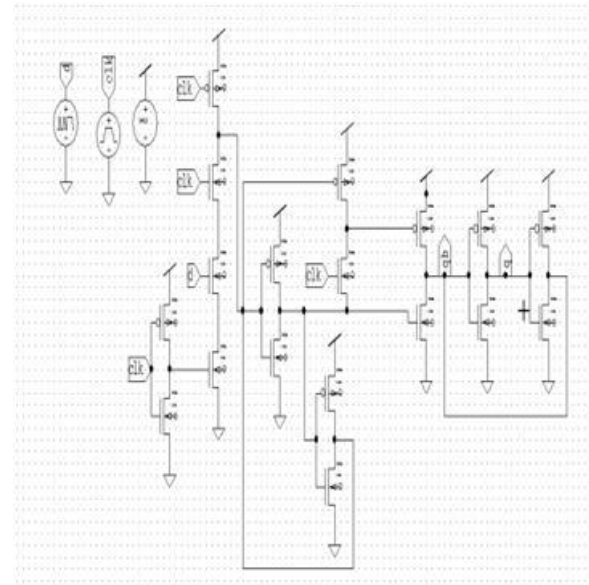
Fig. 6: Dual dynamic node hybrid flip-flop

3. PROPOSED ARCHITECTURE AND POWER EFFICIENT DESIGNS

3.1 Proposed DFF
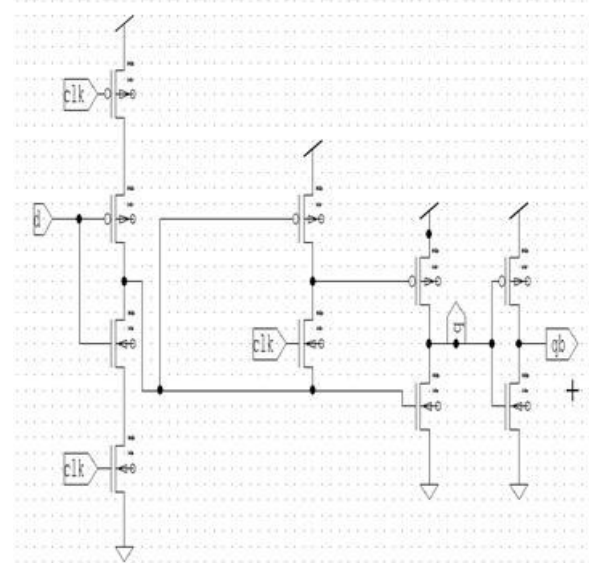
Fig. 7: Proposed DFF

The proposed DFF is designed in such a way that it comes with the reduced area due to lesser number of transistors used for the design. The basic concept behind this structure comes from the overlap based cell and the DDFF design mentioned above. The power dissipation of this flip-flop design is lower than the existing flip-flop designs mentioned above. It also avoids the redundant data transmission that is most prominent in the available flip-flop topologies[8].

3.2 PTL based DFF

One among the promising logic for low power digital system design is Pass Transistor Logic (PTL). It has the advantages of high speed, low area, low power dissipation, lower effect of interconnect compared to the CMOS based logic design. Also this kind of design does not require any feedback data path to

the input. The major drawback of this design that makes it inefficient for digital design is its low swing of output signals. The proposed design avoids the problem of lower output swing. The Fig. 8 shows the design of PTL based D flip-flop.
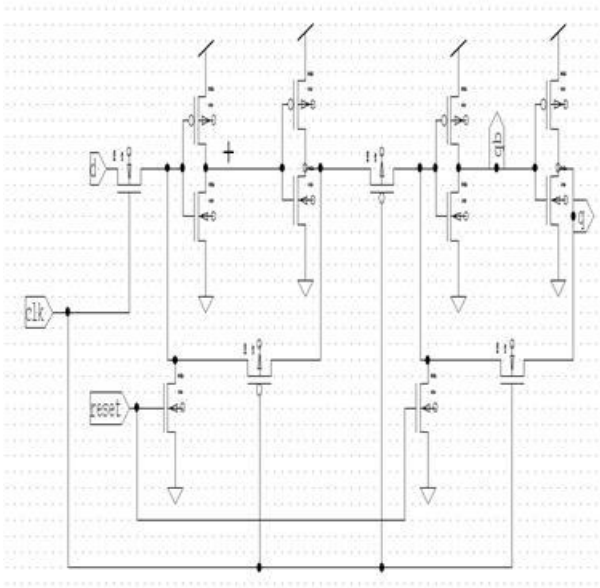
Fig. 8: PTL based DFF

3.3 GDI based DFF
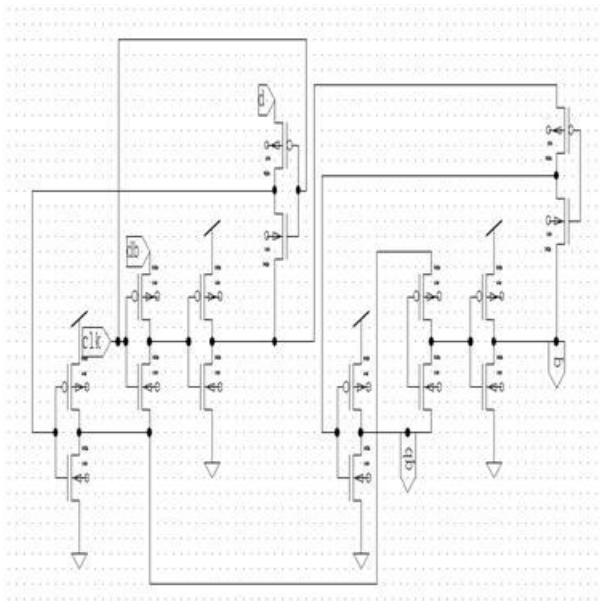
Fig. 9: GDI based DFF

It is an advanced technique for low power design. It has the advantage of fast design of low power circuits with reduced number of transistors. Various logic functions can be implemented using the GDI technique that is compatible with CMOS process. The Fig. 9 shows the D flip-flop implemented using the GDI technique. It uses the concept of two GDI based master slave connections of D-latches. Each of the latches consists of four basic GDI cells. This design requires no level restoring circuits. The waveform analysis and the power results show the efficiency of the design. But this design lacks the structure for embedding logic functions into

it. Whereas in the proposed design, the pull down network paves way for embedding the logic functions.
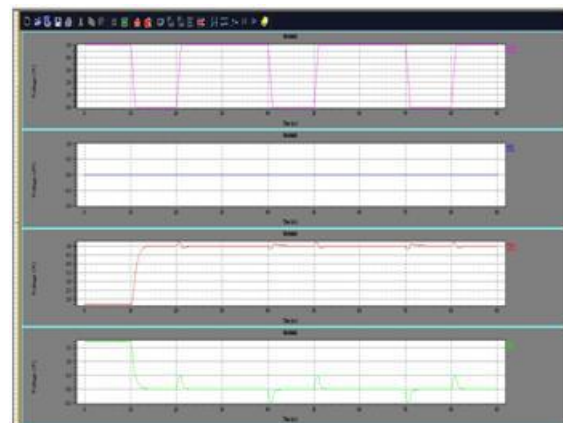
4. RESULTS

The simulation results of existing flip-flop architectures and the proposed design is given below.

The Fig. 10 shows the waveform of PowerPC 603 flip-flop.
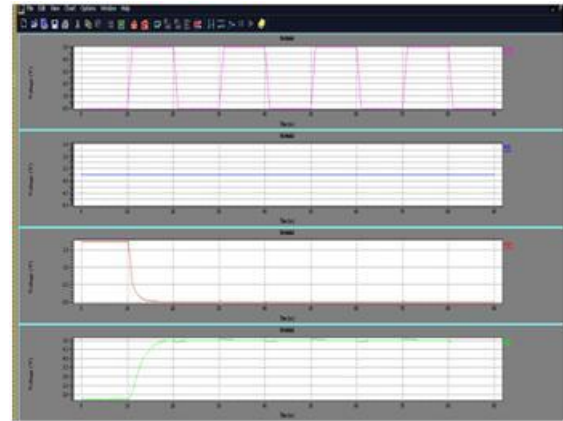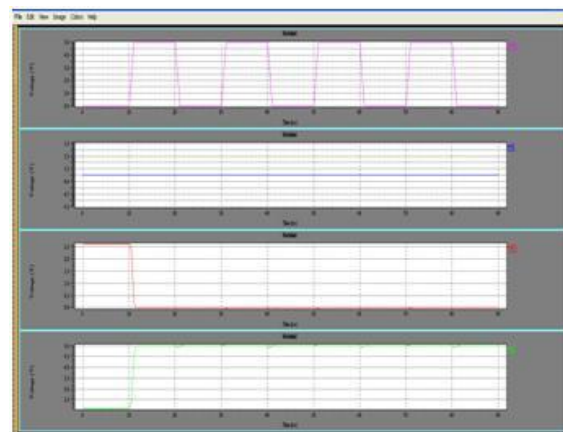

Fig. 10: Waveform of Power PC 603

The Fig. 11 shows the waveform of Hybrid Latch Flip-Flop.

Fig. 11: Waveform of Hybrid Latch Flip-Flop

The Fig. 12 shows the waveform of Semi-Dynamic Flip-Flop.

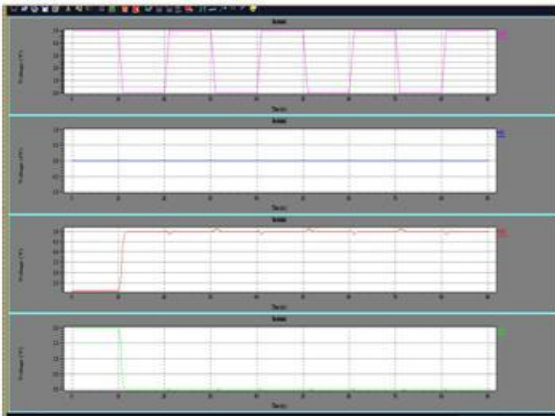
Fig. 12: Waveform of Semi-Dynamic Flip-Flop

The Fig. 13 shows the waveform of Conditional Data Mapping Flip-Flop.
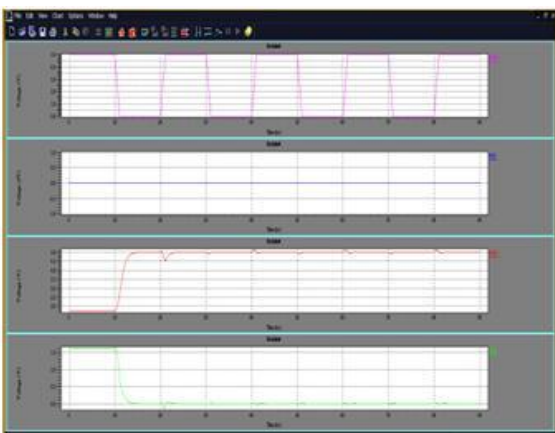

Fig. 13: Waveform of Conditional Data Mapping Flip-Flop

The Fig. 14 shows the waveform of Cross Charge Control Flip-flop.
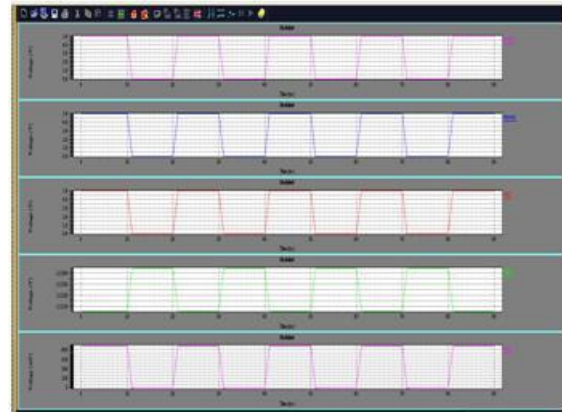

Fig. 14: Waveform of Cross Charge Control Flip-Flop

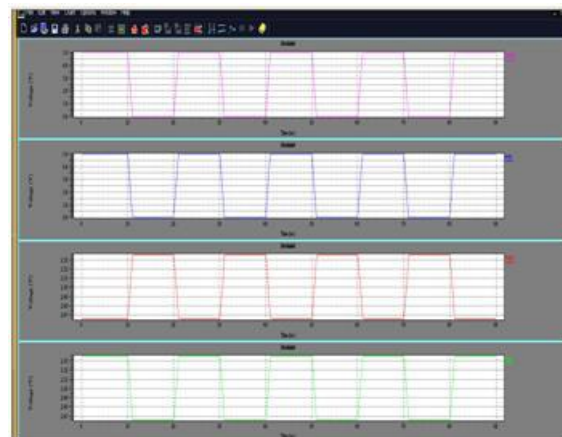The Fig. 15 shows the waveform of Dual Dynamic Node Flip-Flop.

Fig. 15: Waveform of Dual Dynamic Node Flip-Flop

The Fig. 16 shows the waveform of PTL based D Flip-Flop.
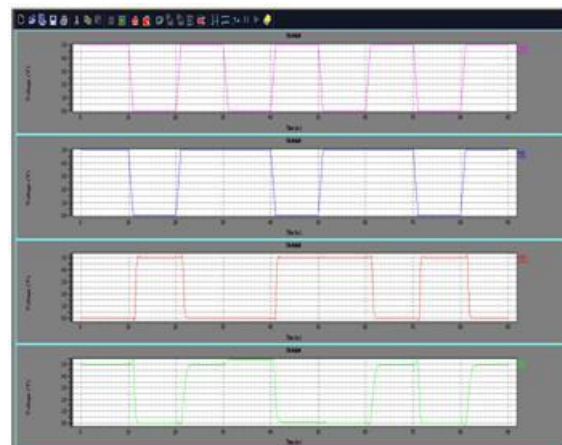

Fig. 16: Waveform of PTL based D Flip-Flop

The Fig. 17 shows the waveform of GDI based D Flip-Flop.

Fig. 17: Waveform of GDI based D Flip-Flop

The Fig. 18 shows the waveform of proposed D Flip-Flop.

Fig. 18: Waveform of Proposed D Flip-Flop

The existing flip-flop topologies are compared against the proposed design in terms of area and power dissipated. The below power comparison table shows that the proposed design is area and power efficient. The Fig. 19 and Fig. 20 give the graphical representation of the power and area analysis of proposed flip-flop against the existing flip-flop topologies.

Table 1. Area and Power Comparison

| Flip-Flop Topology	Number of Transistors	Maximum Power (Watts)	Average Power (Watts)
PowerPC 603	22	0.6070	0.1651
HLFF	20	0.6780	0.2138
SDFF	23	1.2586	0.1582
CDMFF	22	1.1882	0.3509
XCFF	21	0.5048	0.1588
DDFF	18	0.4947	0.1526
PTL-DFF	14	0.332	0.1472
GDI-DFF	16	0.696	0.3584
Proposed DFF	10	0.4736	0.1443

5. CONCLUSION AND FUTURE SCOPE

In this paper, an area and power efficient flip-flop was proposed due to the fast growth of power density in integrated circuits. A comparative analysis of area and power dissipated using tanner v7.0 tool against the existing CMOS, PTL and GDI based D flip-flop architectures proved that the proposed design is suitable for high performance digital designs where area and power dissipation are of major concern.

As a future work, logic functions can be incorporated into the proposed design.
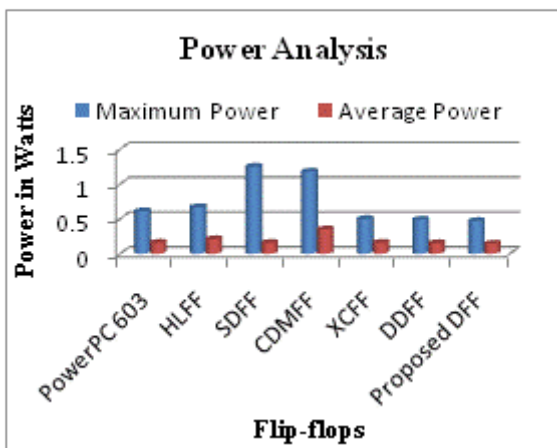
Fig. 19: Power analysis of flip-flops
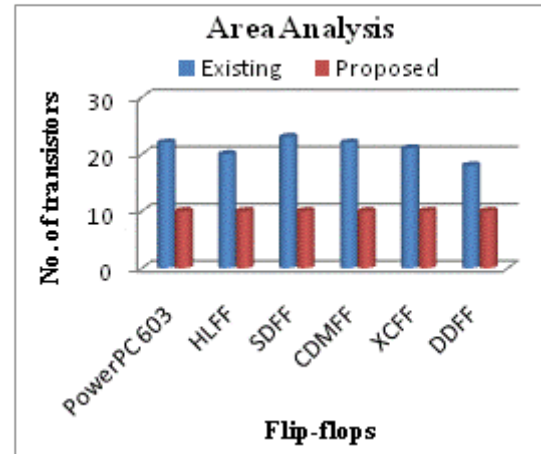
Fig. 20: Area analysis of flip-flops

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