# A Proposed Architecture for Residue Number System based 1D 5/3 Discrete Wavelet Transform using Filter Bank and Lifting Scheme

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## ABSTRACT
This paper presents a novel architecture for a Residue Number System (RNS) based 1D 5/3 Discrete Wavelet Transform (DWT) implementation by using a combination of Filter Bank (FB) and Lifting Scheme (LS). It is designed to modify the architecture of existing binary lifting scheme based 5/3 DWT and RNS based Filter Bank (FB) 5/3 DWT. In this proposed architecture, non-binary RNS arithmetic operations have been used to make sure that the predict and update stages take less amount of time and the complexity is reduced by half as compared to existing binary LS. This paper also addresses the problem of critical modulo RNS division algorithm by using a special ROM based approach. Experimental results show that the proposed architecture is less complex and performs wavelet transforms at good speeds and with high accuracy. The implemented architectures have also been compared with each other to show their own advantages simultaneously.

## General Terms
Processor Architecture, Signal Processing, Wavelet Transform, Optimization.

## Keywords
Modulo adder, Discrete Wavelet Transform (DWT), Residue Number System (RNS), modulo RNS division, bi-orthogonal filter bank, Lifting Scheme (LS).

## 1. INTRODUCTION
The Wavelet transform and multi-resolution signal analysis are basic but important tools that are being used in the fields of applied mathematics, computer vision and signal processing for some time now. The discrete wavelet transform (DWT) provides an efficient representation for a wide range of real world signals. Wavelet transforms are also useful for compression and denoising signals and images [1] [2] [3]. Sweldens developed a lifting scheme for construction of biorthogonal wavelets [4] [5] [6]. This lifting scheme made the implementation of reversible integer wavelet transforms a possibility [7] [8]. Upon comparison with traditional convolution method, LS does not require any kind of complex mathematics. The algorithm to calculate the wavelet coefficient through lifting scheme is much simpler and efficient as it is independent of Fourier transforms. This Lifting scheme is used for designing second-generation wavelets, which are not necessarily translation and dilation of one particular function.

A large integer number can be represented by using a set of smaller integer numbers in Residue domain to make its computation more efficient [9]. This method relies on the Chinese remainder theorem of modular arithmetic for its operation. The idea of remainder theorem itself is ancient and was first described by Sun Tsu Suan-Ching in Master Sun's Arithmetic Manual, written in the 4th century AD. In the field of DSP the residue number system (RNS) and its arithmetic operation are useful for several reasons. The absence of carry propagation in RNS domain makes the realization of high-speed, low-power and efficient systems achievable. This makes its utilization in signal and image processing invaluable. Currently, the VLSI chips are getting small and denser making their full testing costlier and impractical which make fault tolerance and the general area of computational integrity indispensible. RNS finds its application in digital signal processing, communications, computer security (cryptography), image processing, speech processing, and transforms.

This paper discusses the development and implementation of an efficient architecture for RNS based DWT filter banks and RNS based DWT by using lifting scheme. The trend for using wavelets in various signal processing tasks has been increasing at breakneck speed primarily because of two main reasons; Firstly, wavelet transforms can be widely used in various high speed applications such as video and image processing, noise filtering, etc. and secondly, the advanced VLSI technology needs significant decrease in the cost of building practical DSP systems and applications [10] [11] [12] [13]. The main advantage obtained by using RNS is the reduced complexity of arithmetic operations, made possible by converting it into a set of concurrent operations [14]. This paper also solves the problem of implementing the critical RNS divider circuit by using special ROM based approach.

The theoretical background of discrete wavelet transform, filter bank, lifting scheme, modulo adder and modulo divider discussed in this paper and in our scheme is given in section 2. Section 3 elaborates on the proposed architectures, followed by experimental results and conclusions in sections 4 and 5 respectively.

## 2. THEORETICAL BACKGROUND
### 2.1 Discrete Wavelet Transform
The Discrete Wavelet Transform (DWT) is a sampled version of Continuous Wavelet Transform and its computation is significantly faster and consumes lesser resources than CWT. The principle of operation of DWT is based on sub-band coding which yields a faster computation of Wavelet coefficients and is easy to implement with lesser time and resources.

The Discrete Wavelet Transform is in fact, the Continuous Wavelet Transform with discrete scale and translation factors. The DWT is hence, evaluated at discrete scales and translations. The discrete scale is expressed as $s = s_0^{\,i}$, where $i$ is an integer and $s_0 > 1$ is a fixed dilation step. The discrete translation factor is expressed as $\tau = k\ \tau_0\ s_0^{\,i}$, where $k$ is an integer. The translation depends on the dilation step $s_0^{\,i}$. The corresponding discrete wavelets are written as:

$$h_{i,k}(t) = s_0^{\,-i/2}\ h\ (\ s_0^{\,-i}\ (\ t - k\ \tau_0\ s_0^{\,i})) \qquad (1)$$

The discrete wavelet transform with a dyadic scale factor of $s_0 = 2$ is most commonly used in the computer implementation of various algorithms.

## 2.2 Filter Bank

The Filter Bank (FB) method first divides the input data stream into two separate frequency parts for each level of wavelet decomposition. The division is done by passing the signal simultaneously through a low-pass filter $H(z)$ and a high-pass filter $G(z)$ as shown in Fig.1. The subsequent operation is to down sample the high-pass and low-pass components by 2 to generate the low-pass and high-pass outputs s and d respectively. This filter bank method performs DWT based on convolving filter taps $H(z)$ and $G(z)$ can be written in form given in equations 2 and 3.

$$H(z) = h_0 + h_1\ z^{-1} + h_2\ z^{-2} + \ldots + h_N\ z^{-N} \qquad (2)$$

$$G(z) = g_0 + g_1\ z^{-1} + g_2\ z^{-2} + \ldots + g_N\ z^{-N} \qquad (3)$$

Let us consider the Cohen-Daubechies-Feauveau (2,2) wavelet also called CDF (2,2) wavelet as an example. The values of $H(z)$ and $G(z)$ for the aforementioned transform are

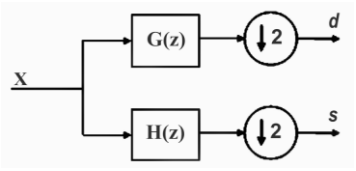


**Figure 1: A block diagram representing one level of wavelet decomposition by DWT.**

given in equations 4 and 5.

$$H(z) = \frac{-1}{4\sqrt{2}}z^2 + \frac{1}{2\sqrt{2}}z + \frac{3}{2\sqrt{2}} + \frac{1}{2\sqrt{2}}z^{-1} + \frac{-1}{4\sqrt{2}}z^{-2} \qquad (4)$$

$$G(z) = \frac{-1}{2\sqrt{2}}z^2 + \frac{1}{2\sqrt{2}}z + \frac{-1}{2\sqrt{2}} \qquad (5)$$

The presence of 5 taps in the low-pass component and 3 taps in the high-pass component gives it the name 5/3 wavelet. The FB structure has many drawbacks, mainly, that it does not provide wavelet transform in the time domain but only in the frequency domain. In addition to this, the floating point nature of the coefficients deems the coefficients unsuitable for hardware implementation. The seemingly large number of arithmetic calculations in this method further complicates matters.

## 2.3 Lifting Scheme

Lifting of biorthogonal wavelets developed by Sweldens, consists of the iterations of three basic operations discussed in the consecutive sub-sections (see fig. 2).

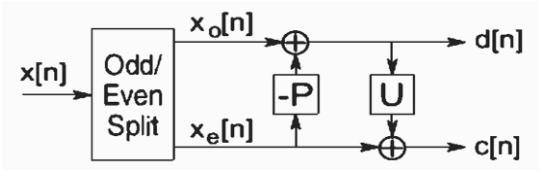


**Figure 2: A block diagram representing the various Lifting stages (Split, Predict & Update)**

### *2.3.1 Split*

This stage splits the entire input data into two frames, one which consists of even samples such as $x_e[n] = x[2n]$ and other consisting of odd samples such as $x_o[n] = x[2n+1]$. In this stage the signal is split into two parts called lazy wavelets because no arithmetic operation is performed.

### *2.3.2 Predict*

This stage generates the wavelet coefficient $d\ [n]$ and it is very easy to predict odd samples from even samples using prediction operator 'P' according to the relation given in equation 6.

$$d[n] = x_0[n] - P(x_e[n]) \qquad (6)$$

### *2.3.3 Update*

In this stage the combination of $x_e[n]$ and $d[n]$ generates scaling coefficient $c[n]$ which represents a coarse approximation of the original signal $x[n]$. This is enhanced by applying an update operator U to the wavelet coefficient and adding to the even samples as given in equation 7 below.

$$c[n] = x_e[n] + U(d[n]) \qquad (7)$$

These three basic stages are called the lifting stage. The inverse of lifting scheme is exactly the same as above and easily calculated, even if P and U are non linear. Rearranging equations (6) and (7), we get,

$$\begin{aligned} x_e[n] &= c[n] - U(d[n]), \\ xo[n] &= d[n] + P(x_e[n]) \end{aligned} \qquad (8)$$

## 2.4 Modulo Adder

The modulo adder is one of the basic arithmetic units in RNS

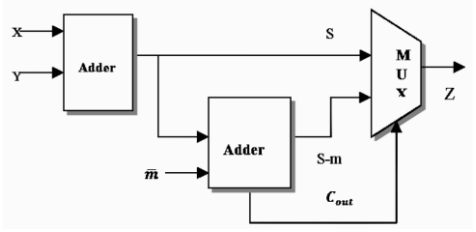


**Figure 3: A basic Modulo Adder circuit**

operation. The design of the adder is invaluable in determining the overall performance of modulo adder. In the modulo adder, the underlying adder is a conventional binary

adder which can have different topologies such as carry-save adder (CSA), carry select adder, ripple carry adder (RCA), carry look-ahead adder (CLA) and so on. For the same word length, a modulo adder is slow and less efficient than the conventional adder because modulo adder needs two conventional adders to perform the modulo addition. The basic idea of modulo addition of any two numbers X and Y with respect to modulus m is

$$\begin{aligned} |X+Y|_m &= X+Y \qquad : X+Y<m \\ &= X+Y-m \qquad : X+Y \geq m \end{aligned} \tag{9}$$

Where, $X \geq 0,\ Y < m$. The basic implementation of equation 9 is shown in fig 3. The result of first addition 'S' is directly connected to the first input of the MUX and also to the input of the second conventional adder whose inputs are S and $\overline{m}$. The output of the second adder 'S-m' is connected to the next input of the previous MUX and carry out of the second adder is directly connected to the select line of this MUX. The whole idea is that if $C_{out}$ is 0 means $X+Y<m$ and if $C_{out}$ is 1, it signifies that $X+Y \geq m$.

## 2.5 Modulo divider

Division technique in RNS has a different approach and suffers from the same drawbacks associated with RNS. The first step in division is to find the multiplicative inverse of the divisor. If the dividend is perfectly divisible by the divisor, the dividend is directly divided. If the number is not perfectly divisible, firstly, the modulus of the dividend is calculated with the moduli and then subtracted from the dividend. The new dividend is used for the division operation.

# 3. IMPLEMENTED ARCHITECTURE

The binary input data stream is firstly converted to RNS data stream by using a ROM based binary to RNS encoder circuit. The output of the encoder circuit is connected to both RNS based filter bank and lifting structure. This output is considered as input for further processing.

## 3.1 RNS based Filter Bank approach for 5/3 DWT

The work described in this paper uses a ROM based modulo multiplier, modulo adder and shift register to perform DWT. The first N/2 bits are taken as mantissa and the next N/2 bits as exponent. This type of input is taken for multiplication because FB filter coefficients are not integer numbers, hence they are not appropriate for hardware implementation; but, by

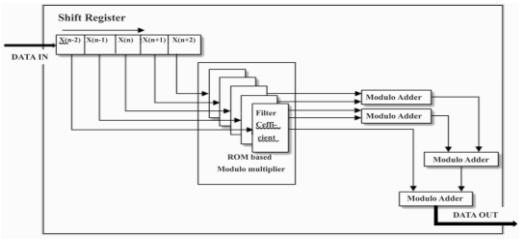


**Figure 4: An FIR Low-pass filter architecture.**

the above technique we can implement FB filters. Figs 4 and 5 illustrate the block diagram for the proposed architecture of a single level of filter bank based DWT. RNS data is first input to the shift register to perform the continuous multiplication of data with different co-efficient, satisfying the conditions laid down in equations 4 and 5. The multiplication of the data with the co-efficient is performed in the ROM based modulo multiplier for faster results. The output is fed to modulo adder that performs the addition as well as the mod operation (figs. 4 and 5).

**Table 1: Filter Co-efficients for the CDF 5/3 filter bank.**

| Low Pass Filter | | High Pass Filter | |
|---|---|---|---|
| H(+2) | -0.176776 | G(+1) | -0.353553 |
| H(+1) | +0.353553 | G(0) | +0.707106 |
| H(0) | +1.060660 | G(-1) | -0.353553 |
| H(-1) | +0.353553 | | |
| H(-2) | -0.176776 | | |

Fig.6 illustrates the block diagram for the floating point multiplier in residue number system. This technique can be

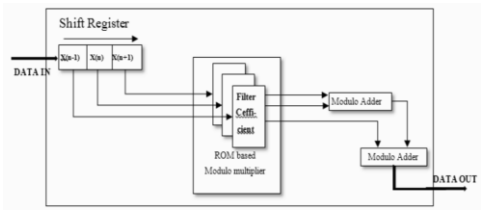


**Figure 5: An FIR High-pass filter architecture.**

implemented on binary number system but at the cost of increased complexity and delay of the circuit.

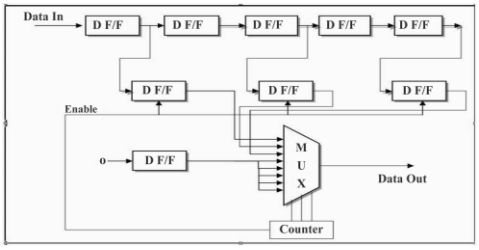


**Figure 6: Architecture for a floating point multiplier.**

Fig. 7 shows the block diagram for down sampling by 2; the counter runs from 0 to 5 where 0 is used as the reset condition. The enable signal will be high when the count reaches 5.

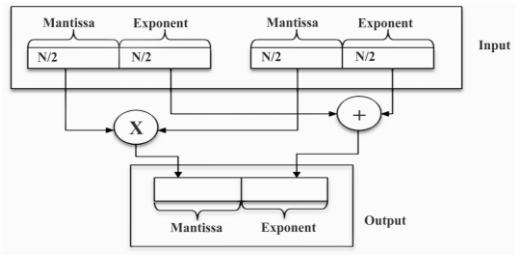


**Figure 7: Architecture for a dyadic down sampler circuit**

## 3.2 RNS based 5/3 DWT based on lifting scheme

In this section, the architecture for 1-level 1-D 5/3 DWT based on lifting scheme has been discussed. In this architecture, there are three basic building blocks which are repeated for multilevel decompositions. Out of these three blocks, the split block is the simplest. The function of this block is to separate the input samples into two parts, namely, even and odd. The block diagram for the 'split' block is shown in fig. 8. The implementation of the other two blocks

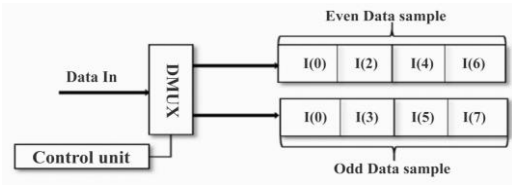


**Figure 8: Architecture for the proposed Split Block**

(predict and update) are more critical than the first one. A new architecture for multilevel 1-D DWT is presented, which is designed by using a pipelined approach.

## 3.3 Implemented architecture of RNS based Predict block for 1-level 1-D 5/3 lifting DWT

The implemented RNS based predict block for 1-level 1-D 5/3 lifting DWT is designed to receive four even input samples and generate four outputs which are the wavelet coefficient. The prediction of odd samples from even samples is based on given four formulae:

$$D1 = D1 - [\frac{1}{2}(S1 + S2) + \frac{1}{2}] \quad (10)$$

$$D2 = D2 - [\frac{1}{2}(S2 + S3) + \frac{1}{2}] \quad (11)$$

$$D3 = D3 - [\frac{1}{2}(S3 + S4) + \frac{1}{2}] \quad (12)$$

$$D4 = D4 - [\frac{1}{2}(S4 + 0) + \frac{1}{2}] \quad (13)$$

Where D1, D2, D3, D4 are odd samples and S1, S2, S3, S4 are even samples which are generated after passing the data stream through the 'split' block.

To implement these basic formulae, 6 shift registers have been used to store even and odd samples for 3 different modules (m1, m2, m3). Each shift register has two outputs which are connected to the modulo adder. The outputs from three of these 4-bit modulo adders are merged to generate a 12-bit unique number. To avoid the critical RNS division, a 12×12 bit ROM is used for implementing D1 and is rounded off to give an integer number. The output from the ROM is connected to the splitter whose primary function is to split the 12 bits into three 4-bit sequences. These 4-bit numbers are again connected to a modulo subtractor (which actually uses modulo 2's complement adder circuit for the subtract operation) whose other input is attached to another shift register, which stores the data in same location. The diagram of the proposed RNS based 'predict' block for lifting scheme is shown in fig 9.

## 3.4 Implemented RNS based Update block for 1-level 1-D 5/3 lifting DWT

The design of the implemented RNS based 'Update' block for 1-level 1-D 5/3 lifting DWT is exactly same as 'Predict'

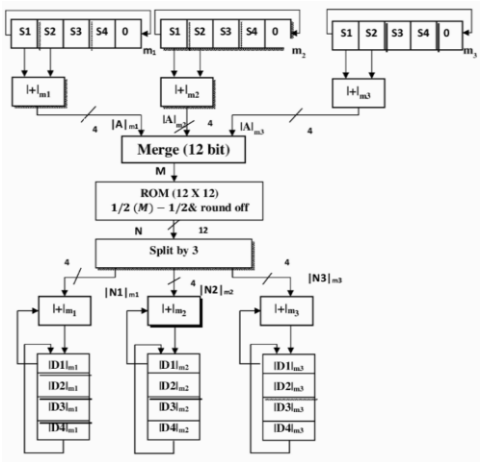


**Figure 9: The proposed RNS based Predict block for lifting scheme.**

block, but this block accepts odd samples and using update operator it generates scaling coefficients for the original signal. The 'predict' block is implemented by using basic four equations to solve 5/3 lifting DWT.

$$S1 = S1 + [\frac{1}{2}(D0 + D1) + \frac{1}{2}] \quad (14)$$

$$S2 = S2 + [\frac{1}{2}(D1 + D2) + \frac{1}{2}] \quad (15)$$

$$S3 = S3 + [\frac{1}{2}(D2 + D3) + \frac{1}{2}] \quad (16)$$

$$S4 = S4 + [\frac{1}{2}(D3 + D4) + \frac{1}{2}] \quad (17)$$

Where D0=0, D1, D2, D3, D4 are odd samples and S1, S2, S3, S4 are even samples which are generated after passing

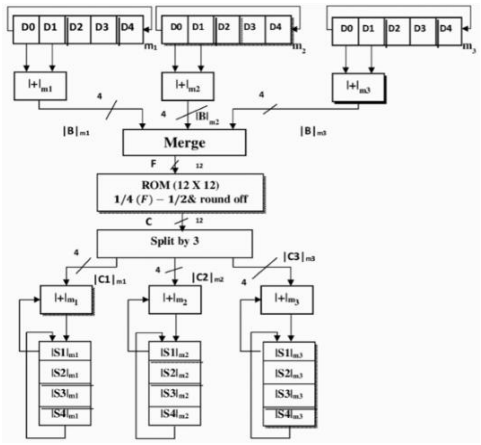


**Figure 10: The proposed RNS based Update block for lifting scheme.**

through the 'split' block.

The operation of this block is exactly the same as 'predict' block but the 12×12 bit ROM evaluates the value of equation

$\frac{1}{2}(D0 + D1) + \frac{1}{2}$ and rounds off the value to make the result an integer. The diagram of the proposed architecture is shown in fig 10.

After level-1 decomposition, the output of the update block again connects to the split block. The rest of blocks are used in the same manner as of the first level. We will get the final output after level-3 decomposition. Finally, the outputs of both filter banks and lifting architecture are again converted by signed RNS to binary decoder circuit using CRT technique.

## 4. EXPERIMENTAL RESULT

In this section, the results are reported for the performance comparison of one level of decomposing RNS based 5/3 DWT using lifting scheme and filter bank architecture. The evaluation is in terms of the number of ROM multipliers, number of adders, shift registers, computational time and consumed power during performance. Firstly, the proposed architecture is analyzed for its performance. The computational time for both circuits has been observed at the same internal clock rate and it can be easily seen that the lifting scheme is more efficient for high speed applications. If we discuss about hardware utilization, the RNS based lifting structure has significantly reduced number of ROM multipliers, mod adders and shift registers. On the other hand, the same lifting scheme is not power efficient when it is again compared with the filter bank scheme. Every module in our proposed architecture has cent percent hardware utilization. The detailed comparison of results are listed in table 2 from which it is clear that our proposed RNS based lifting structure is more efficient than the other scheme in terms of hardware utilization and time delay.

**Table 2: Comparison for the resource utilization and performance summary.**

| Proposed architecture | Mod adders | Shift registers | ROM multiplier | Delay (ns) | Power (w) |
|---|---|---|---|---|---|
| RNS based FB Scheme | 18 | 6 | 24 | 6.332 | 0.586 |
| RNS based Lifting Scheme | 6 | 6 | 1 | 4.180 | 1.332 |

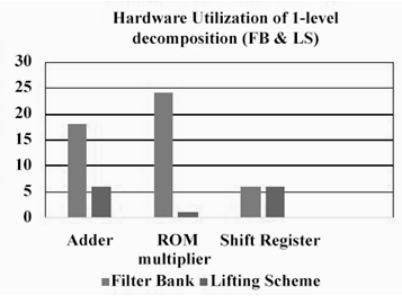


**Figure 11: A comparative chart showing the relative hardware utilization for one level of decomposition of filter bank and lifting scheme.**

## 5. CONCLUSION

In this paper, a new RNS based architecture for lifting scheme and filter bank for DWT has been implemented. The main contribution of the implemented architecture is divided into three parts. First of all, we have implemented an efficient

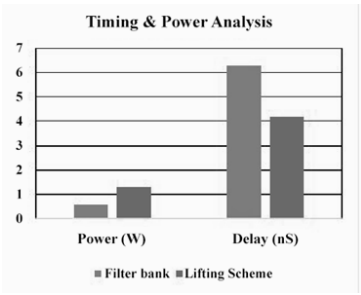


**Figure 12: A comparative chart showing the timing delay and power consumption for filter bank and lifting scheme.**

reconfigurable RNS based filter bank for 5/3 DWT which takes less time and power as compared to binary filter banks. Secondly, we represent a novel architecture for RNS based lifting scheme for 1-D 5/3 DWT. This lifting structure has been designed to modify the existing binary lifting structure in terms of complexity, delay and also solve the problem of implementing the critical RNS divider circuit. Finally, we have compared the two different efficient structures and analyzed their performances.

The experimental results demonstrate that the proposed RNS based lifting structure is better than the RNS based filter bank in terms of speed, power and complexity. These proposed architectures could be very efficient alternatives for high speed and low power DSP, communication based applications and are also suitable for VLSI implementation.

## 6. ACKNOWLEDGMENT

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