Design of Low Power Wake-up Receiver for Wireless Sensor Network

Nikita Patel
Dept. of ECE
Mody University of Sci. & Tech.
Lakshmangarh (Rajasthan), India

Satyajit Anand
Dept. of ECE
Mody University of Sci. & Tech.
Lakshmangarh (Rajasthan), India

P. P. Bhattacharya
Dept. of ECE
Mody University of Sci. & Tech.
Lakshmangarh (Rajasthan), India

ABSTRACT
Wireless Sensor Networks find various applications in different fields. Sensor nodes are small, low-cost and low-powered communication devices. Hence designing a network with low power consumption is a critical issue in WSN. Different schemes are projected for achieving low power communication under short network range. To reduce the use of power and retaining a good lifetime, ultra-low power wake-up receiver is introduced. Energy dissipation is reduced here by maximizing data transceivers sleep time. In this paper, design and simulation of a wake-up receiver is carried out at 90nm and 45nm technology. Results are found to be satisfactory.

Keywords
Wake up receiver, low power, VLSI, sensor node, WSN.

1. INTRODUCTION
Wireless Sensor Network (WSN) consists of a large amount of small battery powered devices which perform tasks like processing, radio transmission-reception, sensing and actuating. Wireless sensor network devices complete large tasks with their limited energy resource. Energy consumption is still remains the limitation of this field. WSN comprises of thousands of nodes which are used to exchange information with the user either directly or through the external base-station (BS).

Sensor node consists of Sensing unit, process unit, transmission unit and electromagnetic unit. These are the four major constituent of sensor nodes appointed with dissimilar jobs. Sensing unit is used to trace the physical environment and tell the CPU to compute and store the data it sensed. Transmission unit is tasked to receive the information from CPU and transmit it to the outside world. Power unit regulate battery power to sensor node [1].

WSN finds a large number of applications. Few of them are listed below.

- **Sensing of Wildfires:**

Sensor nodes equipped with temperature sensors can be deployed randomly in forest to detect fires at an early stage and prevent greater damages. Any change in the temperature is detected by sensor and the packets which contain measurements is broadcasted so that further action can be taken.

- **Building Monitoring and Control:**

Sensor nodes embedded in building can reduce costs of energy by monitoring the temperature and lightening conditions.

- **Industrial Process Control:**

Wireless sensors in fields and factories can monitor the condition of equipments to alert for imminent failures. This reduces the cost of service and maintenance.

- **Sensing Oil Leakage:**

Oil pipelines are generally long and passes through an uninhabited area. So their monitoring is difficult. Suitable sensors can be placed across the pipeline to send information such as pressure or humidity which in turn can help to prevent wastage of oil.

- **Environmental Monitoring:**

Wireless sensor nodes can be used to monitor environmental conditions such as quality of air, types of pollutants or any other natural or man-made disasters [2]. It can also monitor conditions and movement of wild animals and plants where minimal disturbance to the habitat is desired.

In Wireless sensor Networks (WSN) individual node area unit is heavily duty-cycled and thus save a lot of power and nodes stay most of the time in sleep mode. Typically, each node periodically monitors the wireless channel to concentrate for potential incoming traffic. To minimize power consumption in WSN a dedicated wake-up receiver is used within every sensor node which unendingly monitors the channel continuously and activates the node only when requested to send packets [3].

2. DESIGN OF WAKE-UP RECEIVER CIRCUIT
The architecture of wake-up receiver contains bias circuit, envelope detectors, differential amplifier, buffer, RC integrator and 18 bit shift register as shown in Fig 1. The first basic block is bias circuit that provides the desired selectivity. The signal received from bias circuit goes to an envelope detector. The envelope detector is extremely sensitive to temperature and bias variation. Thus two Envelope detectors are used to cancel the effects. The envelope detector works in current mode. After envelope detector signal passes through differential amplifier where it is further amplified. The signal swings once it passes through differential amplifier. The envelope detectors and differential amplifier are biased from constant bias circuit. To form the voltage swing larger (0 to V_{dd}), a buffer is employed that consists of three inverters [4]. High value of R is chosen to induce a high output swing and therefore the C is completed by the input capacitance of following stage (differential amplifier). The filter removes the basic and better harmonics of the input RF carrier. To get an approximately rail-to-rail voltage swing, a buffer consisting of

three CMOS inverter, is used following the differential amplifier. The edge voltages of the inverters are set by proper size of the transistors. The output of the differential amplifier as well as the threshold voltage of the inverters varies with temperature and bias variation [5]. Different types of clock recovery mechanism are studied. These standard clock recovery schemes are power hungry. Thus a replacement methodology has been applied wherever the demodulated signal is used as clock and therefore the information is recovered from it. The bias circuit that has been used provides bias voltage and current to envelope detector and differential amplifier. D flip-flops are used to store the bits. Transmission gate static flip-flops are used which are in master-slave configuration.

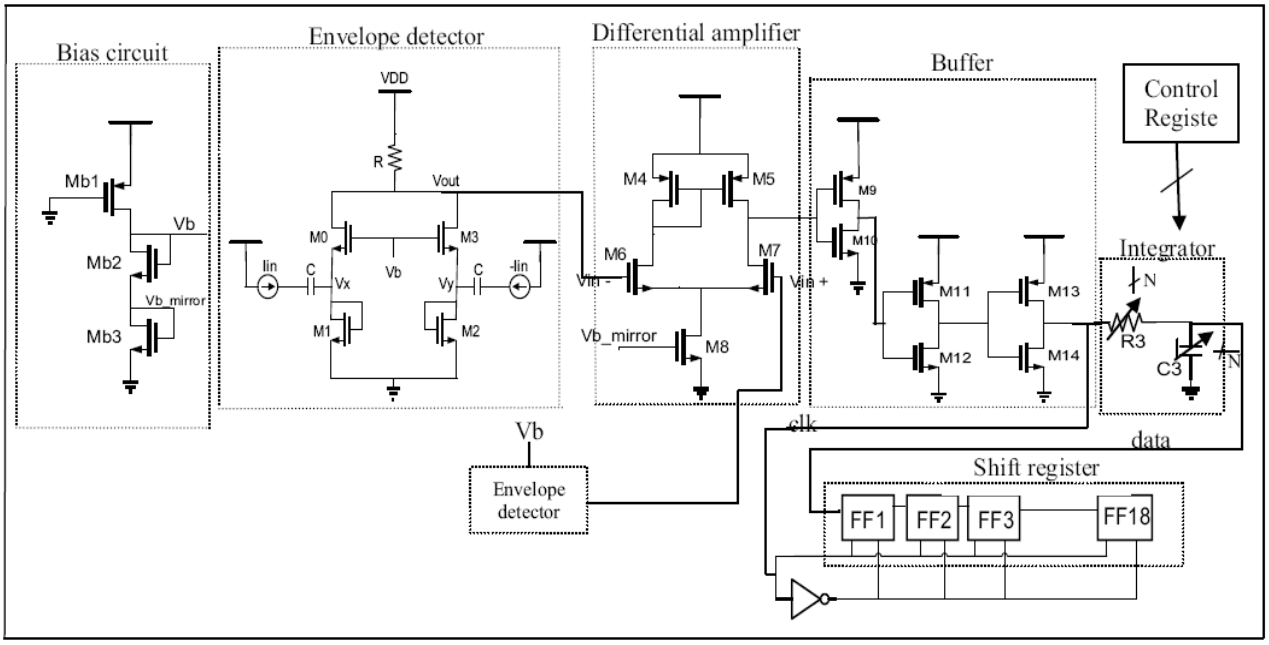


Fig 1: Wake-up receiver

The flips-flops are connected in series to make a shift registers. The first bit is stored in FF18 and the last bit is stored in FF1. The demodulated digital signal itself is used as clock. The clock is integrated, compared and then passed to the series of flip flops. The Flip-flops are transmission gate negative edge Flip-flops.

The proposed architecture contains Bias circuit, envelope detectors, differential amplifier, buffer, RC integrator and 18 bit shift register. Each individual circuit are discussed below.

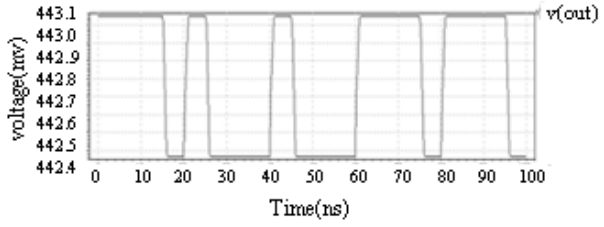
- **Bias circuit:**

The bias V_b is generated from V_{dd} by an external bias circuit. If V_{dd} increases then V_b also increases. Since the envelope detector supports a small amount of current, due to small variation in V_b a large variation in current occurs. The bias circuit provides bias voltage to the two envelope detectors and the differential amplifier. As the temperature varies the threshold voltage also varies. Therefore, the output is little sensitive to temperature variation. The bias V_b is generated from V_{dd} by an external bias circuit. If V_{dd} will increase then V_b additionally will increase. Since the envelope detector supports a small quantity of current, because of little variation in V_b an oversized variation in current happens. The bias circuit provides bias voltage to the two envelope detectors and therefore the differential amplifier. Because the temperature varies the threshold voltage additionally varies. Therefore, the output is small sensitive to temperature variation.

- **Envelope Detector circuit:**

The envelope detector uses an improved version of current mode rectifier described in [6]. The envelope detector circuit works with a differential input current and has a single-ended voltage output. The envelope detector has a high bandwidth due to low parasitic capacitance associated to the input. Since the envelope detector has a symmetric structure, the gain for positive input half-cycle and the gain for negative input half-cycle are equal. To cancel the temperature variation effects, a dummy envelope detector is used, which produces an equal DC voltage at the other input of the differential amplifier under temperature variations. The output of the rectifier is in current domain. The final output of the envelope detector is in voltage domain. The envelope detector is highly sensitive to temperature and bias variation [7].

The Envelope detector circuit has four transistors all biased in saturation region. V_b is the external bias applied to it. C is the decoupling capacitor which is used to remove the dc. The output is taken at the drain of M3. The dc bias current of the structure depends upon V_b and the sizing of the transistors. The value of R is taken high such that we get a higher swing at the output. The waveform of Envelope Detector is shown in Fig 2.



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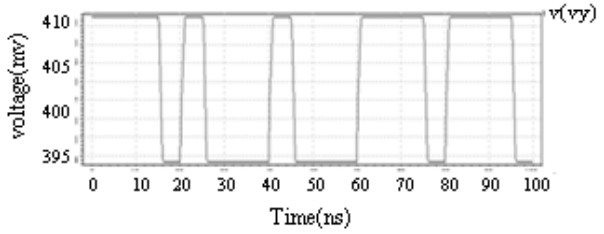

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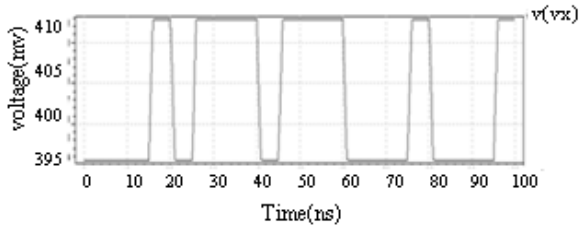


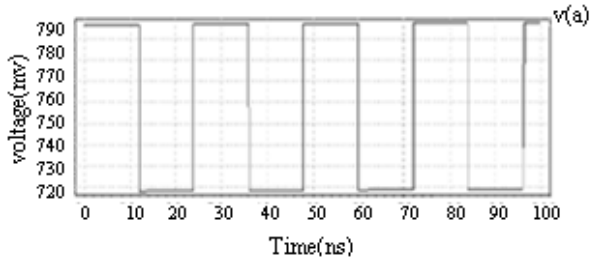
(c)

Fig 2: Envelope Detector waveform (a) output (b) (c) inputs

- **Differential amplifier circuit:**

The envelope detector works with a very low current and it is very sensitive to temperature and bias variation. To overcome this problem, differential amplifier is used. This not only increases the voltage swing but also makes the output less sensitive to temperature, bias and process variation. The differential input is supplied from two envelope detectors and output. The difference signal is further amplified by this differential amplifier.

The differential amplifier consists of two stages. In the first stage the voltage is converted into current and the current is mirrored in the second stage and again it is converted into voltage. Since both the envelope detectors are same, we can assume that same temperature and process variation occurs. So the common mode voltage of the differential amplifier changes and it has no effect on the current flowing in the differential amplifier. Transistors M4, M5, M6, M7, M8, forms the first stage of differential amplifier. M8 is used to flow a particular current in the circuit V_b _mirror is derived from the bias circuit. The input voltage is converted into current through M4 and M5. Then current through M6 is mirrored in buffer and converted into voltage. This circuit is preferred to make the output of differential amplifier less sensitive to temperature and process variation. The waveform of differential amplifier is shown in Fig 3.



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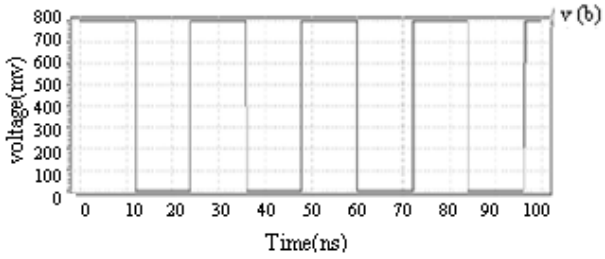

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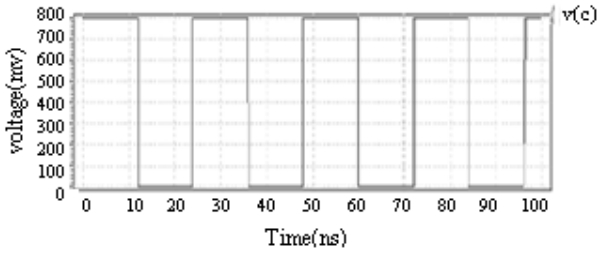
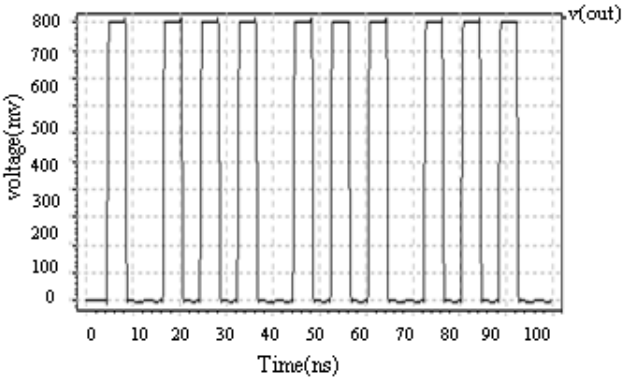


(c)

Fig 3: Differential amplifier waveform (a) output (b) (c) inputs

- **Buffer circuit:**

The output of the differential amplifier is more amplified by the buffer to induce a swing from 0 to V_{dd} as shown in Fig 4. The output of the buffer will directly be used as a clock to the negative-edge triggered shift register. The buffered signal is any integrated to recover the information bits that are sampled by the shift register.



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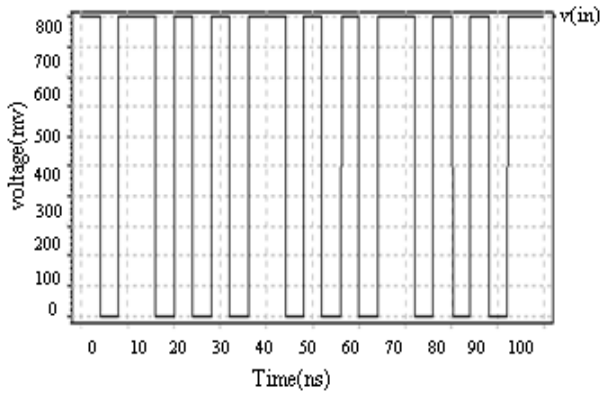
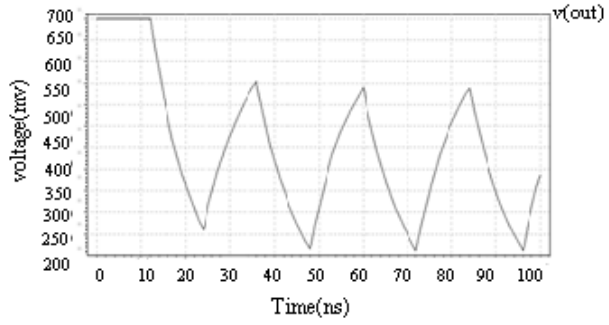


(b)

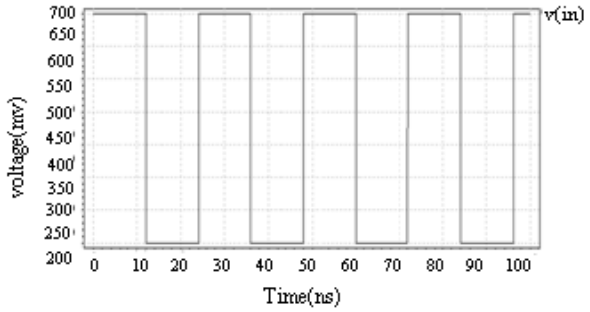
Fig 4: Buffer Waveform (a) output (b) input

- **Integrator circuit:**

The integrator is employed to additional integrate the Buffer signal to recover the information bits that are sampled by the shift register. The input and output waveform are shown in Fig 5. The time constant of integrator is chosen such the bit'1' voltage level and also the bit '0' voltage level are separated out across the switching threshold of the inverter placed with the very initial flip-flop (FF1) of the shift register.



(a)



(b)

Fig 5: Integrator Waveform (a) output (b) input

- **Shift Register circuit:**

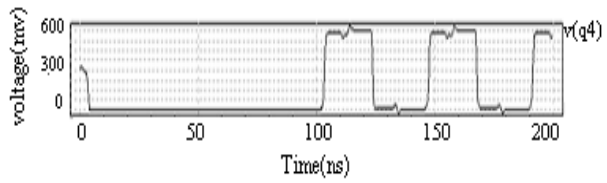
For waking up a specific sensor node, the entranceway sensor node sends a wake-up signal. This signal contains the address of the node and a few additional data. The wake-up signal is demodulated and keeps within the register. The receiver is not in power-down mode throughout absence of signal.

The sensitivity of the circuit is given by the minimum quantity of current needed at the input of the envelope detector so bits area unit detected while not error and area unit keep within the register. For storing the information in register, we want a clock. There is no external clock offered within the system. Clock recovery will be done however it takes lots of power. Therefore a distinct mechanism is applied.

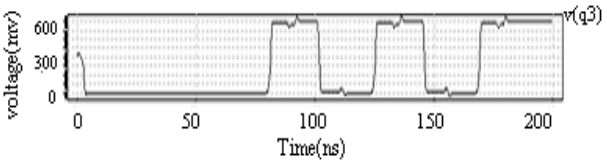
Flip flop Design:

The negative edge triggered flip-flop is realized by cascading a positive level latch and negative level latch. Transmission gate flip-flops area unit used for this. Once clock goes high the master latch is activated. It samples the information and the information is available at the output of latch. At constant time, the slave flip flop is inactive. Once clock goes low the slave becomes active and therefore the master becomes inactive. The input area unit information and clock as shown in Fig 6(e) and Fig 6(f). Therefore the outputs of the register with negative edge triggered D flip-flop with taken inputs area unit shown in Fig 6 (a)-(d).

One of the most constraints of the planning is that it has to be low battery-powered. The current in every device is kept as minimum as potential. The power consumption can depend on the previous bit due to switching of flip-flops. Therefore the power consumption due to 10 and 01 will not be same.



(a)



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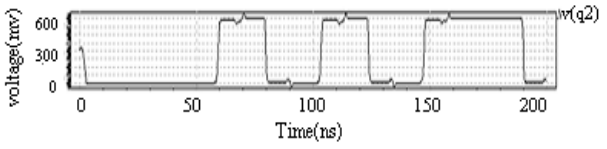

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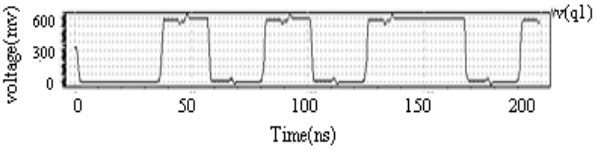

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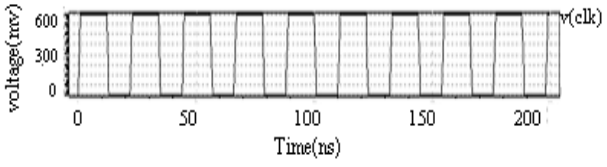

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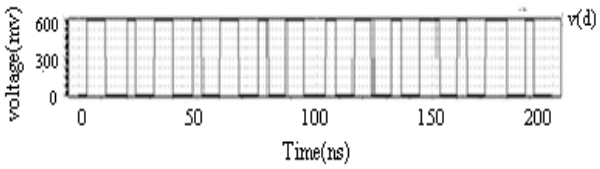

(f)

Fig 6: Negative edge triggered D flip flop waveforms (a) (b) (c) (d) outputs (e) (f) inputs

3. SIMULATION AND RESULTS

The simulation result of the complete wake-up receiver and individual blocks are shown below. The individual blocks were simulated at 90nm technology and wake-up receiver at 90nm and 45nm technology. Table 1 depicts the power consumption of individual blocks of wake-up receiver at 90nm technology (V_{dd} = 0.9V).

TABLE 1. Power Consumption of Individual blocks at 90nm

Wake-up Receiver	**Power** (µW)
Bias	3.47
Envelope detector	13.76
Additional Envelope detector	13.76
Differential amplifier	0.000295
Integrator	0.00000081
Buffer	0.4227
Shift register	32.577
Total power consumption	63.98

Table 2 and Table 3 show the wake-up receiver power consumption, delay, power delay product at 90nm and 45nm technology and getting parameters at each output of the circuit using 0.9v supply voltage.

TABLE 2. Power, Delay and Power Delay Product of Wakeup Receiver at 90nm

Wake-up Receiver	**Power (µW)**	**Delay (ns)**	**PDP (J)**
Differential amplifier	56.3	0.1001	5.639×10^{-15}
Buffer	56.3	0.373	2.099×10^{-14}
Integrator	47.46	0.1202	5.706×10^{-13}

Table 3. Power, Delay and Power Delay Product of Individual Blocks at 45nm

Wake-up Receiver	**Power (µW)**	**Delay (ns)**	**PDP (J)**
Differential amplifier	74.34	0.000034	2.549×10^{-15}
Buffer	74.34	0.0000507	3.7733×10^{-15}
Integrator	65.3	0.0099	6.5276×10^{-13}

The comparison between the power at 90nm and 45nm technology is shown in Table 4.

TABLE 4. Comparison of Power Consumption of Wakeup Receiver at 90nm and 45nm

Wake-up Receiver	**Power (µW) at 90nm**	**Power (µW) at 45nm**
Bias circuit	3.47	7.56
Envelope detector	14.14	33.27
Additional Envelope detector	14.14	33.27
Differential amplifier	56.3	74.34
Buffer	56.3	74.34
Integrator	47.46	65.3
Shift register	101.7	132.1

By analysing the wake up receiver at 90nm and 45nm technology (V_{dd}=0.9V), it may be concluded that power is increased at 45nm as compared to 90nm and therefore delay is reduced at 45nm in comparison to 90nm.

4. CONCLUSION

The wake-up receiver is an additional receiver, which continuously monitors the channel and wakes the rest of the circuit blocks when necessary. In this paper, a wake-up receiver was designed and simulated at 90nm and 45nm technology. The total power consumption at 90nm technology is found to be 63.98 µW. The simulation results show that at 45nm technology, total power consumption in wake-up receiver is more as compared to 90nm technology, whereas delay is less at 45nm as compared to 90nm technology.

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