Modified CPL Adiabatic Gated Logic – MCPLAG based DPET DFF with XOR

Manoj Sharma
Research Scholar, Mewar University, Rajasthan
Dept. of ECE, BVCOE

Arti Noor
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CDAC Noida
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ABSTRACT
The use of Adiabatic Logic in VLSI chip design has certainly promised positive aspects in terms of optimizing the power equations. In the reported work authors have extended their proposed CPLAG based 'XOR' implementation. The modified 'XOR' implementation is further configured to implement a dynamic positive edge triggered D flip flop. Both the reported circuits are functionally verified and found to be satisfactory to a high degree of signal integrity and accuracy. DFF circuit is further examined with different load, temperature range, transistor size and voltage levels. The results obtained from the proposed implementation of hybrid 'XOR' and DFF have showed good results. The average power at 1.5V, 180nm, 25^{o}C, 1fF load is 0.209nW and 23-39nW for 0.8v, 40^{o}C for different run with Pclk_Q delay 0.2ns, input_Q delay 16µs, Qtrise 44.6µs, Qtfall 61µs, Qbtrise 4.54µs, Qbtfall 3µs with 50.9 zepto units PDP. The average power consumption for a conventional semi-adiabatic PFAL DFF is 35mW approx as compared to 0.1µW for the implemented DFF.

General Terms
Low Power, VlSI Design, CPL, Adiabatic Logic. Power delay product, fully adiabatic logic, semi adiabatic logic

Keywords
CPLAG, DPETDFF, XOR, FAL, SAL, PDP

1. INTRODUCTION
With the advancement of the VLSI fabrication technologies the capability related to the circuit integration have driven the engineers, researchers, and circuit designers to implement functionalities satisfying the required power equations. Functionality density have increased tremendously in recent times leading to high power per unit area that need to be removed for proper and reliable functionality.

The increasing demand for portable products further necessitates the requirement of low power circuits. The changing market demands in favour of portability and modularity of different products to ease out daily life and to enhance the comfort level play a major role in compacting different functionalities.

On the other hand the advancements in the battery technology lag the technological advancement in the circuit integration capabilities. The power per unit volume in the batteries has increased many-fold but to fulfill the ever increasing demand these advances becomes insufficient. Frequent battery replacement is not feasible because of different limitations in working environment. Especially for health care products which are implanted into human body it is not feasible to operate the patent for battery replacement.

With the ever increase of the products in daily life globally the environmentalist have expressed their worries about the power dissipation from the electronic products. They consider this issue in two fold. Firstly the direct heat dissipated and secondly the heat dissipated by the electronic appliances installed to remove the heat from the working ecosystem to the environment.

Due to above discussed factors it is very essential to integrate and implement the desired functionality using power aware circuits. Traditionally many low power technologies have been proposed and are used to satisfy the power requirements. And there is no single technique which can address the power issues single handedly. Different techniques are to be used simultaneously for the same. In pursuance of the same some concepts from other science domains are also borrowed into VLSI design domain for achieving the desired power constraints. Adiabatic Logic is one such concept that has been adopted from classical thermo-mechanical systems. The idea of zero heat exchange of the system with the environment have motivated the circuit designers to try and implement this while designing the circuit configurations and topologies for different functionalities [1-3,6-9,11,12] The base work behind the development of adiabatic VLSI processing came from Landaur [4,5] and Benett [5,10]. Adiabatic Logic takes asymptotically zero energy loss.

Broadly adiabatic circuits are classified as fully adiabatic circuits and semi-adiabatic circuits. Full Adiabatic circuit have zero non-adiabatic power loss, leading to an idealist approach while circuit design process. On the other hand semi-adiabatic circuit suffers from some non-adiabatic power loss. Still the power equations are much promising as compared to traditional circuit implementation techniques.

As power $P=CV^2F$, there is inherent tradeoff between power area and timings. As power is optimized using adiabatic circuit design techniques the other two namely area and speed have to be compromised [13 - 17].

2. MODIFIED CPL ADIABATIC GATED LOGIC
Complimentary Pass Transistor (CPL) utilize only NMOS transistors, complementary input signals and produces complementary outputs. In conventional CPL circuits inputs may be applied to 'gate' and/or 'source/drain' terminals of the transistors. As PMOS transistors are not used as functional implementation part in CPL, the parasitics associated are reduced greatly and act in favour of CPL based circuits by increasing the operating speed and reducing the power requirements in transitions process [13-17]. In adiabatic processing a time varying source is used instead of constant

voltage source as depicted in Figure 1. The output, input and the transistor topology remains same.

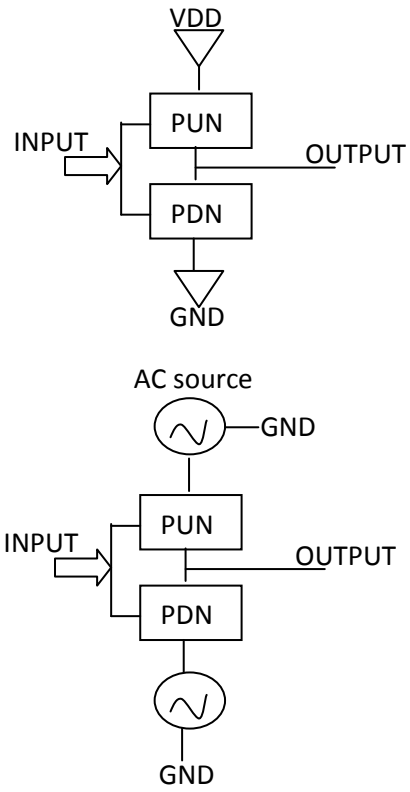

Fig 1: CMOS structure and adiabatic structure outlay

The charging and discharging process of the capacitance determines the power behavior of the two circuits. It can be shown that by increasing the time of logic transfer the power associated can be reduced which is the basic working criteria for the adiabatic logic circuits.

Authors have make use of CPL concept and semi adiabatic approach for implementing the functionality [1]. The data gating is used for implementation to have advantage in synchronizing the combination blocks and deactivating them when not required and hence improving the power equations further.

In the present work authors have modified their previous communicated work of CPLAG 'XOR' and extended this to implement dynamic positive edge triggered D flip flop (DPETDFF). In the proposed methodology authors have targeted to negate the disadvantage of slow operating speed of adiabatic family circuits via using the advantage of fast operating speed of CPL family circuits in favour of power aware design. In the said methodology, threshold voltage manipulation is not required contrary to CPL family helping in retaining the noise impunity associated. This also takes care of susceptibility of transistors to sub-threshold conduction in off mode.

3. MPLAG DPET DFF WITH XOR

3.1 Circuit Description

The implemented circuit is shown in Figure 2. A total of 10 NMOS and 2 PMOS are used which provide complete swing at the output. The circuit is driven by a time variant power source 'Pclk' which is also acting as clock input to the circuit. The use of 'Pclk' enables energy recovery from the circuit. Asynchronous 'rest' functionality is provided which can be converted into synchronous behavior with use of one additional transistor. The Power clock-driven back to back inverter stage maintains the signal integrity at the output providing complete strength for further stages. Same circuit has capability to work as 'Gated XOR' gate and with Dynamic Positive Edge Triggered D Flip Flop with input permutations. Being based upon CPL logic 'XOR' and 'XNOR' functionality is available.

3.2 Circuit Implementation

A four phase power clock as shown in Figure 3 is used to drive the circuit. In the first 'Evaluate phase' the logic of the circuit is evaluated based upon the input values. Second 'Hold phase' hold the evaluated value in the circuit processing. In third 'Recovery phase' the charge from the circuit is recovered back to the reservoir for further utilization in subsequent stages. In fourth 'Ideal phase' the transistor terminals are at same levels leading to no current; and next input levels may be provided in the ideal phase. The implementation parameters are listed into Table 1. The circuit simulation waveforms are shown in Figure 4 and Figure 5.

Table 1. Simulation parameters

Simulation parameters			
Technology	***Value***	***Simulation***	***Value***
Channel Length	.180 microns	Power clock	pulse type with Trise and Tfall
Min. width	.180 microns	Input Signal	Bit type
Max. width	36 microns	Delay calculation	50% points
|Vton|	0.3932664	Data Sequence	8 cycles
TOX	4.10E-09	Power clock Time period	40 micro sec
MOS Gate Capacitance Model:			
capmod=0			
Conditions:			
Voltage	1V to 5 V (+0.5V)		
Temperature	-50, 25, 30, 40, 70, 100, 200		

For simplicity while analyzing the circuit implementation, the best is to use the basic NMOS and PMOS behavior in cut-off, linear and saturation mode of operation. Following are the equations used for the analyzing the NMOS model:

$$Id = {}^{k}/_{2}\,[2(Vgs - Vt)Vds - Vds^2] \quad \ldots 1$$

$$Vgs \geq Vt, Vds \leq Vgs - Vt$$

$$Id = {}^{k}/_{2}\,(Vgs - Vt)^2 \quad \ldots 2$$

$$Vgs \geq Vt, Vds > Vgs - Vt$$

$$Ids = 0\ Vgs < Vt \quad \ldots 3$$

where I_d = Drain to Source current, k = device transconductance ($\mu_n C_{ox} W/L$), V_{gs} = Gate to source voltage, V_{ds} = Drain to source voltage, V_t = Threshold voltage, μ_n = Electron surface mobility, C_{ox}=Gate oxide capacitance per unit area. From these equations, drain current depends upon the biasing, transistor size and threshold voltage. So controlling and analyzing these parameters provide mechanism to control the operation region for the transistors in the said circuit and hence the drain currents.

4. RESULTS

The functional behavior of the circuit is analyzed with different levels of supply voltage, temperature ranges and different load capacitances. The circuit is also analyzed for different transistor width. The increased width is also considered as storage nodes in-between the circuit topology. The charge storage capacity of the larger size transistor also helps in analyzing the timing consideration for the circuits.

The circuit is simulated first for 'XOR' behavior and then for dynamic positive edge triggered D flip-flop. This can be converted into static behavior as well with the feedback mechanism. The simulation results show the correct behavior for the proposed circuit with full swings and signal integrity.

The circuit is analyzed for voltage range of 1V, 1.5V, 2V, 2,5V, 3V, 3.5V, 4V and above. The functional verification for the circuit is made and found to be satisfactorily working for the above said voltage levels. The power delay product variation wrt to supply voltage levels are shown in Figure 6. From PDP curve it is seen that the best operation of the proposed circuit is for voltage range of 1V to 3.5V with PDP ranging from 0.5p unit upto 3.5V; 1p unit at 4V and 15p unit for 4.5V. The Pclk_Q delay, shown in figure 14 is approximately constant with voltage level variation in the said range. Input_Q delay is constant beyond 2V and is in the range of 15µs to 18µs in the voltage range of 1-2V. The maximum limit for the average power consumed from the Pclk is 1.8µW for 5V. For the best PDP in the range of 1-3.5V the average power consumed varies to 0.7µW approximately. The data input sources are used for gating the transistors. The average power consumed for data input source is very less in the range of 0.1µW and practically can be considered as independent of voltage level variation wrt data inputs as in Figure 10. The normalized power fed-back from the circuit is shown in Figure 18. For lower voltage levels major part of the power drawn from the source is fed back approximately. With increase in voltage level the difference in normalized power fed back and normalized power drawn increases. The rise and fall time for the out signals are tabulated in Table no 2. From the data it can be seen that for higher voltage levels the rise time and fall time decreases. The average power at the load ranges from 4.8fW to 12.3pW with voltage variation in the range. The max current for the transistors lies in the range of 1µA.

The said circuit is analyzed for 12 loads namely 1fF, 0.1pF, 0.2pF, 0.3pF, 0.4pF, 0.5pF, 0.6pF, 0.7pF, 0.8pF, 0.9pF, 1pF and 2.3pF. The PDP behavior for the said load is shown in Figure 9. For the loading capacity upto 0.8pF the PDP behavior can be approximated to linear behavior wrt to load. For higher load, the behavior is multi-quadratic in nature. Taking the average input load for majority of the logic blocks at 180nm technology, equivalent to 15fF the proposed circuit can easily drive them with satisfactory PDP for 0.8pF load. Similarly to PDP, the Pclk_Q delay can be approximated to be linear wrt load upto 0.8pF and multi-quadratic for higher loads as shown in Figure 17. The Pclk_Q delay varies from 60ns for 0.8pF and 0.14µs for 1pF. The input_Q delay can be approximated to be constant around 6.25µs still 0.8pF and increases sharply thereof. The average power pertaining to Pclk, shown in Figure 13, varies linearly with load till 1pF in the range of less than 10nW. For load beyond 1pF the average power for Pclk increases sharply. It is around 75nW at 2.3pF. The power for data sources is independent wrt load variation. Normalized power feedback to the source is shown in Figure 21. Approximately 20pW is fed back to the power source out of 70pW drawn. The normalized power fed back to the source can be taken as independent of load variation as shown.

The said circuit is analyzed with 20 different transistor size namely 180nm, 360nm, 540nm, 720nm, 900nm, 10.8µm, 12.6µm, 14.4µm, 16.2µm, 18.0µm, 19.8µm, 21.6µm, 23.4µm, 25.2µm, 27.0µm, 28.8µm, 30.6µm, 32.4µm, 34.2µm, 36µm. The PDP variation for the said range is shown in Figure 8. The PDP for transistor size less then 19.8um can be considered lineally variant and again for larger transistor it can be taken as linearly dependent. From this it can be seen that smaller the size, better the PDP. The Pclk_Q delay can be considered constant wrt transistor size range of 200ps from transistor less then 180um and 0.5nm for larger transistors as shown in Figure 16. The input_Q delay can be taken as constant for transistor variation which is approximately 6.24µs. The average power consumed from the Pclk and data source varies linearly with the transistor size. The contribution in average power for Pclk increases with transistor size. The variation of average power drawn from Pclk and data source varied in convex manner, shown in Figure 12. Similarly the gap between the normalized power drawn from the Pclk and power fed back to power source increases with size. For lower size transistor, a larger part of normalized power is fed back to source. The normalized power distribution is shown in Figure 20.The average power around the load is 5fW for different transistor.

The proposed circuit is simulated for six different temperature ranges namely -50°C, 25°C, 40°C, 70°C, 100°C, and 200°C. The PDP behavior is shown in Figure 7. For higher temperature range beyond 100°C PDP increases sharply. For temperature range from -50°C to 100°C the circuit is verified to work satisfactory. The Pclk_Q delay is in the range of 100ps to 200ps approximately. For temperature beyond 100°C, delay increase sharply as shown in Figure 15. The input_q delay is independent for temperature variation. The input_q is around 6.24µs. With the temperature variation the impedance changes and hence the average power dissipated changes, shown in Figure 11. The variation of average power for Pclk lies in the range of 3nW upto 100°C and increase thereof. The normalized power drawn from the Pclk and fed back to it is shown in Figure 19. A value in the range of 0.2pW to 2.5pW is fed back from the circuit. The ration of the power drawn from the source and the power fed back can be considered independent of temperature variation. The average power for load is in the range of 5.30fW. A comparative table

for the average power dissipation for DFF is shown in Table no 3.

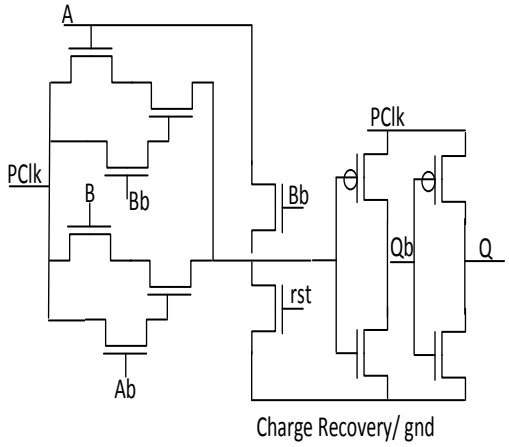

Fig 2: Proposed MCPLAG DPET DFF with adiabatic 'xor'

Table 2. Rise and Fall timings for Q and Qb

Vdd	Qtrise	Qtfall	Qbtrise	Qbtfall
1	46.9 µs	57.6 µs	6.84 µs	6.01 µs
1.5	44.6 µs	61.6 µs	4.54 µs	3.00 µs
2	43.4 µs	63.6 µs	3.40 µs	1.50 µs
2.5	42.8 µs	64.9 µs	2.72 µs	0.603 µs
3	26.3 µs	25.7 µs	2.26 µs	2.82ns
3.5	26.4 µs	26.3 µs	1.94v	1.64ns
4	26.5 µs	26.7 µs	1.69v	0.877ns
4.5	26.5 µs	27.1 µs	1.50 µs	0.633ns
5	26.6 µs	27.3 µs	1.35v	0.701ns

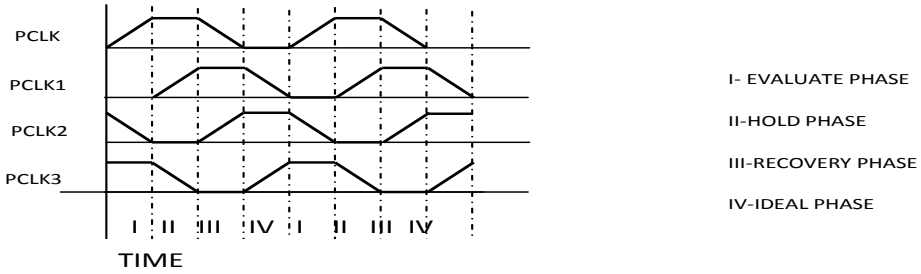

Fig 3: Four Phase power Clock Pclk

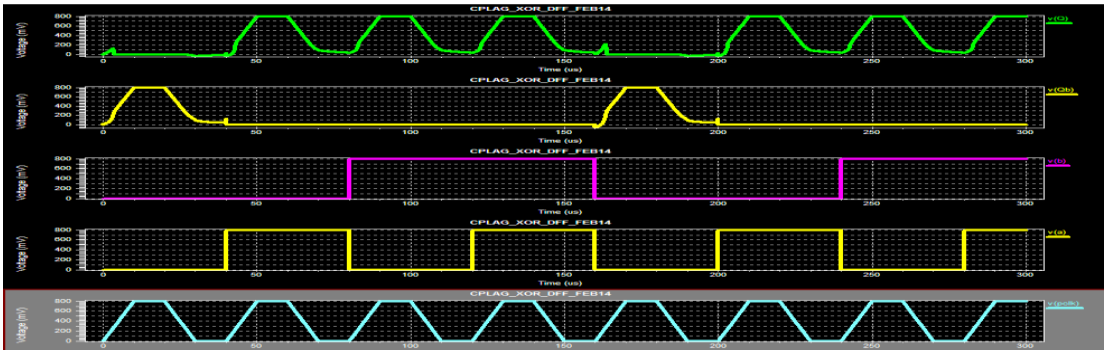

Fig 4: Simulation waveform for Adiabatic 'XOR'

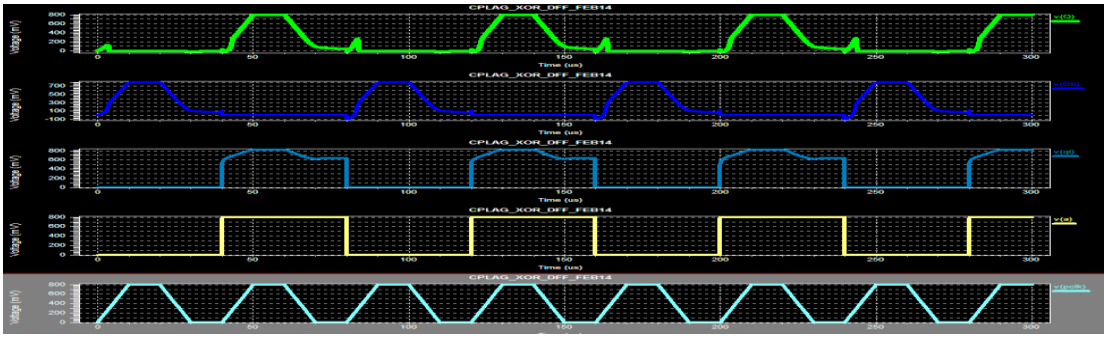

Fig 5: Simulation waveform for Adiabatic 'DPET DFF

Table 3. Average Power comparison

Power Results D FF	
Vpulse_voltage : 4 phase trapezoidal source	
Average power consumed [2]	35mW
Average power consumed Proposed design	0.1µW

5. CONCLUSION

In the reported work authors have modified their previous reported CPLAG 'XOR' gate. The reported MCPLAG based DFF with 'XOR' gate is functionally verified to work satisfactory using 180nm technology. The proposed circuit functions as dynamic positive edge triggered adiabatic flip flop and adiabatic 'XOR' gate with input permutations. The said circuit can be converted into static positive edge triggered adiabatic flip flop with an inclusion of feed back stage. The implemented flip flop has asynchronous rest capability which can be converted into synchronous behavior with the help of one extra transistor. The signal integrity and swing levels are maintained both for DPETDFF and 'XOR' gate. A total of 10 NMOS and 2 PMOS are used for the said implementation. The proposed circuit is analyzed with a) 10 different voltage levels (0.8V, 1V, 1.5V, 2V,2.5V,3V 3.5V, 4V,4.5V and 5V); b) 12 loads (1fF, 0.1pF, 0.2pF, 0.3pF, 0.4pF, 0.5pF, 0.6pF, 0.7pF, 0.8pF, 0.9pF, 1pF and 2.3pF); c) 20 different transistor sizes (180nm, 360nm, 540nm, 720nm, 900nm, 10.8µm, 12.6µm, 14.4µm, 16.2µm, 18.0µm, 19.8µm, 21.6µm, 23.4µm, 25.2µm, 27.0µm, 28.8µm, 30.6µm, 32.4µm, 34.2µm, 36µm) and d) six different temperature range (-50^{o}C, 25^{o}C, 40^{o}C, 70^{o}C, 100^{o}C, and 200^{o}C). For all these the circuit is analyzed for a) average power from Pclk, data inputs; b) Pclk_Q delay; c) Input_Q delay; d) power delay product; e) Normalized power drawn and fed back to Pclk source; f) average power for cload; i) transistor current. From the PDP variation 0.8V to 3.5V voltage range, at -50^{o}C to 100^{o}C, with load of 0.8pf, working with 180nm technology is best suited for circuit working. The average power at 1.5V 180nm 25 ^{o}C, 1fF load is 0.209nW and 23-39nW for 0.8V, 40 ^{o}C for different run with Pclk_Q delay 0.2ns, input_Q delay 16µs, Qtrise=44.6µs, Qtfall=61µs, Qbtrise=4.54µs, Qbtfall=3µs with 50.9 zepto units PDP. The improvement in the average power drawn is very much evident while comparing the implemented DFF with conventional semi-adiabatic PFAL DFF. The average power consumption for a conventional semi-adiabatic PFAL DFF is 35mW approx as compared to 0.1µW for the implemented DFF.

6. ACKNOWLEDGMENTS

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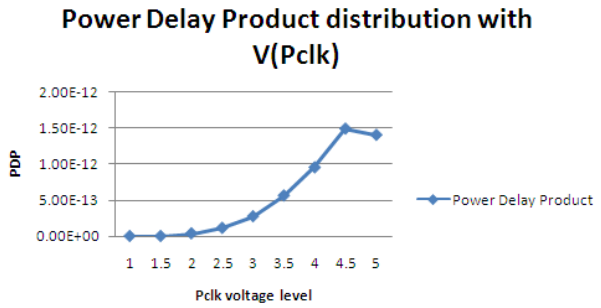

Fig 6: PDP for voltage variation

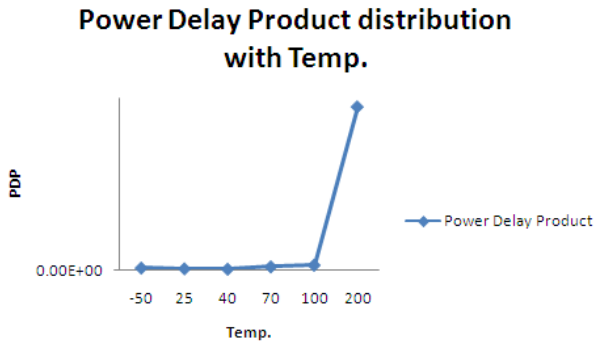

Fig 7: PDP for temp. Variation

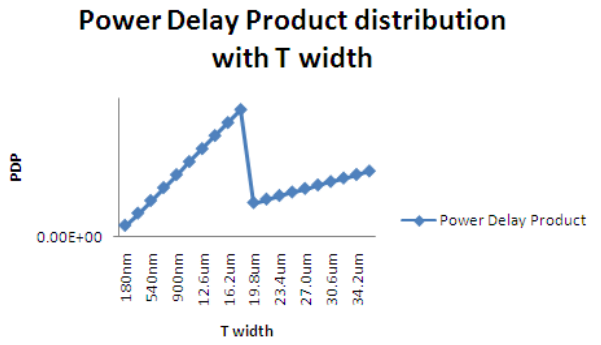

Fig 8: PDP for T size variation

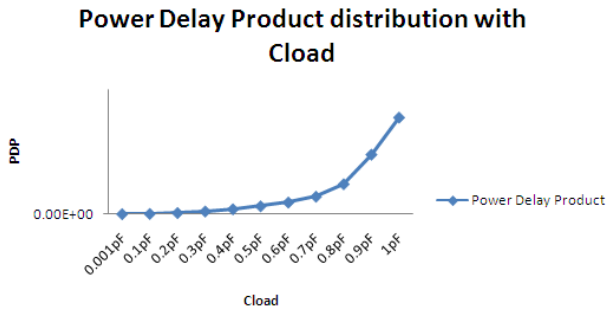

Fig 9: PDP for load variation

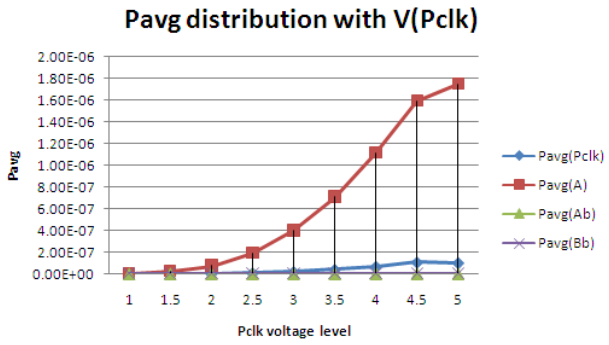

Fig 10: Average Power distribution for voltage variation

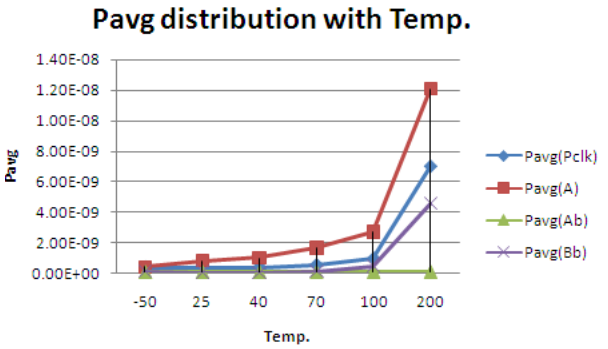

Fig 11: Average Power distribution for Temp variation

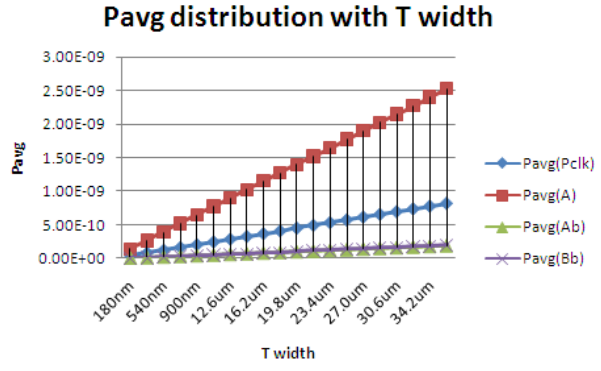

Fig 12: Average Power distribution for T size variation

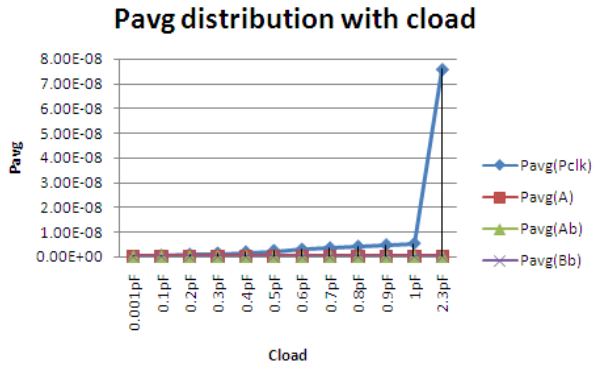

Fig 13: Average Power distribution for load variation

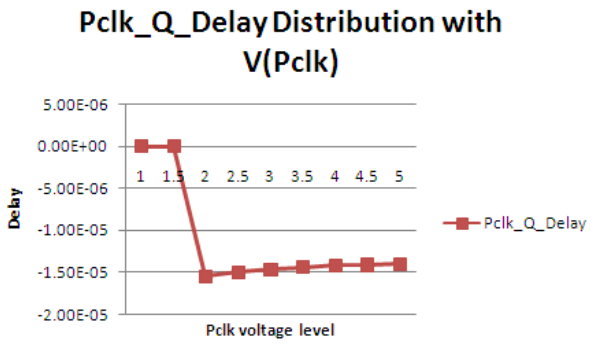

Fig 14: Pclk to Q delay for voltage variation

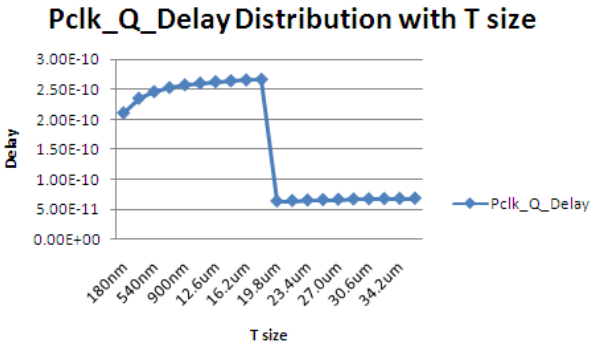

Fig 16: Pclk to Q delay for T size variation

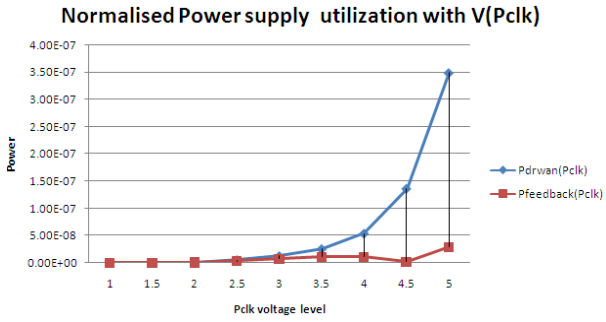

Fig 18: Normalized Power drawn and fed back for voltage variation

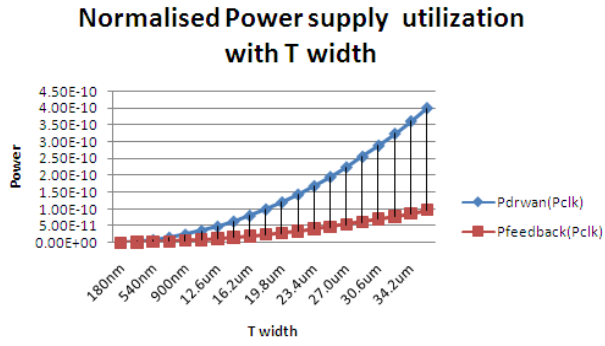

Fig 20: Normalized Power drawn and fed back for T size variation

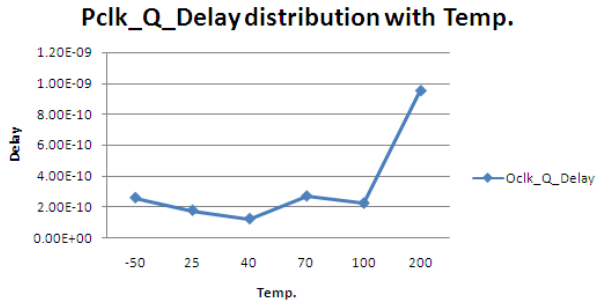

Fig 15: Pclk to Q delay for Temp variation

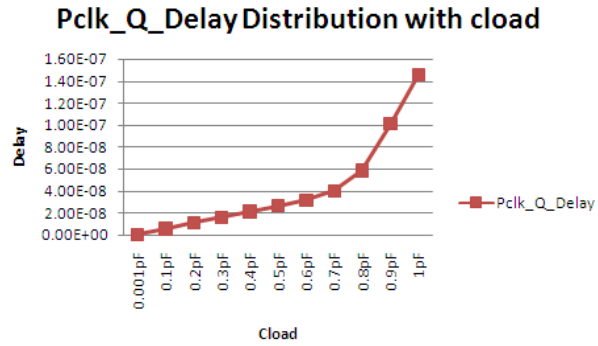

Fig 17: Pclk to Q delay for load variation

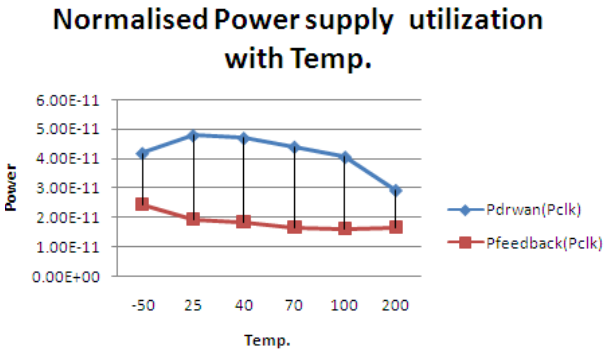

Fig 19: Normalized Power drawn and fed back for Temp variation

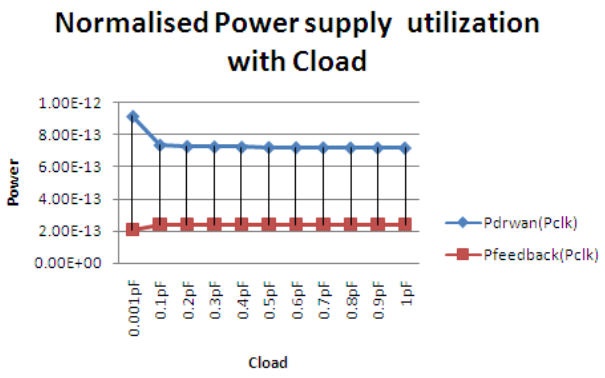

Fig 21: Normalized Power drawn and fed back for load variation