Analysis of Active Feedback and its Influence on UWB Low Noise Amplifier

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ABSTRACT
In this paper, various active feedback techniques for Ultra-Wide Band (UWB) CMOS Low Noise Amplifier (LNA) are proposed. First, an LNA consisting of Common Gate (CG) stage for input matching, cascode with interstage current reuse as core stage and Common Drain (CD) stage for output matching is presented. Three feedback techniques such as global feedback, local full feedback and local partial feedback techniques are employed in this LNA. The analysis is made for the different feedback networks consisting of resistive, common source, common gate and common drain. The proposed LNA is designed with 90 nm technology and its performance is analyzed with Agilent's ADS simulator. Among the analyzed LNA's, CG partial active feedback and CD partial active feedback achieves power gain of 23.8 dB and 23.75 and noise figure of 6.1-6.3 dB and 4.6-5.8 dB respectively.

General Terms
Low Noise Amplifier, Noise Figure, Linearity.

Keywords
Global feedback, Local full feedback, Local partial feedback.

1. INTRODUCTION
UWB is an unlicensed wireless technology that coexists with other licensed wireless technologies. FCC has allocated 7500 MHz bandwidth for UWB applications in the 3.1–10.6 GHz. Low-energy and extremely short duration impulses are used over a wide spectrum of frequencies. The average power spectral density limit is –41dBm/MHz or 75nW/MHz. Therefore UWB technology provides a promising solution to the RF spectrum drought by allowing new services to coexist with current radio systems with minimal or no interference [1]. This revolutionary technology is intended to provide an efficient use of scarce radio bandwidth while enabling both high data rate short range applications and low data rate longer-range applications.

With several advantages and restrictions in UWB technologies, many challenges exist in designing receiver front end circuits. Low Noise Amplifier (LNA) is the first block in any receiver system. The main purpose of the LNA is to amplify the weak signal without adding much noise of its own. Therefore the LNA design has many challenges because of its need to achieve high gain, low noise figure (NF), good input and output matching, stability and better linearity. According to Friis' formula, the overall noise factor of the system is dominated by the first stage in the receiver system if the gain of the successive stage is made high. Hence, the main design consideration for the LNA is low NF. Several noise reduction techniques are discussed in the literature survey.

The paper is arranged as follows. Section 2 discusses about the existing noise reduction techniques. Section 3 discusses about the basic LNA taken for analysis. Section 4 discusses about noise cancellation principle in global feedback, local full feedback and local partial feedback. Section 5 deals with the results obtained from the simulations and finally the conclusions are provided in section 6.

2. LITERATURE SURVEY
A feedforward noise reduction is discussed in [2] and it addresses the problem of noise reduction with broadband impedance matching. The feedforward path is designed such that it constructively adds the signal but reduces the noise. A noise cancelling technique with current reuse configuration is found in [3]. It consists of CS-CG with series resonated topology contributing less power and good noise performance. The drawback is that it achieves only gain up to 15 dB. In [4], Chin-Fu Li et al., proposed a signal nulled feedback technique that consists of an additional loop with capacitance and a transistor such that it suppresses the noise but the drawback in this technique is the reduction of gain.

In [5], the LNA is designed with CG input matching and CD output matching, cascade gain stage and shunt series peaking with interstage current reuse is proposed and the circuit offers moderate gain with low power. A folded LC cascaded topology with multigated transistor is found in [6] and it linearizes the output transconductance non-linearities and it achieves better linearity and good noise figure.

In [7], noise reduction and linearity improvement techniques for differential LNA have been discussed. It uses cascade differential LNA and the inductor is connected at the gate of the cascode transistor and it uses a strategy called capacitive cross coupling to reduce noise and improve linearity. But the drawback is increased area and power consumption. In this paper in order to reduce noise, several noise reduction feedback techniques are proposed and their performances are analyzed.

3. BASIC LNA

The LNA circuit found in [5] consists of 3 stages as shown in figure 1. The first stage is the Common Gate (CG) input stage which is used for input matching for the entire UWB band of 3.1 -11.6 GHz. The second stage is the core stage consisting of cascode LNA with interstage current reuse. The interstage current reuse is used to increase the gain without increasing the power consumption. The shunt-series peaking in this stage enhances the bandwidth. The third stage is the Common Drain (CD) stage used for output matching. This circuit is taken as the basic circuit and proposed feedback techniques are implemented in this circuit and the performances are analyzed.

The CG input stage is devoid of miller capacitance. A very good input matching is achieved by the resister R_1 and the inductor L_1. The inter stage current reuse network is formed by the inductors L_5, L_4 and C_1 and it is used to bias the transistor M_3 and therefore it drives less power from the supply. At high frequencies, a low impedance path is created through C_1 as the impedance of L_3 becomes large. This results in gain flatness. The shunt series peaking used may cause peaking of gain at certain frequencies leading to less stability. This can be overcomed by the interstage peaking inductor. The common drain amplifier is used as a buffer to enable easy output matching. The output impedance can be easily matched by adjusting the width of M_4,

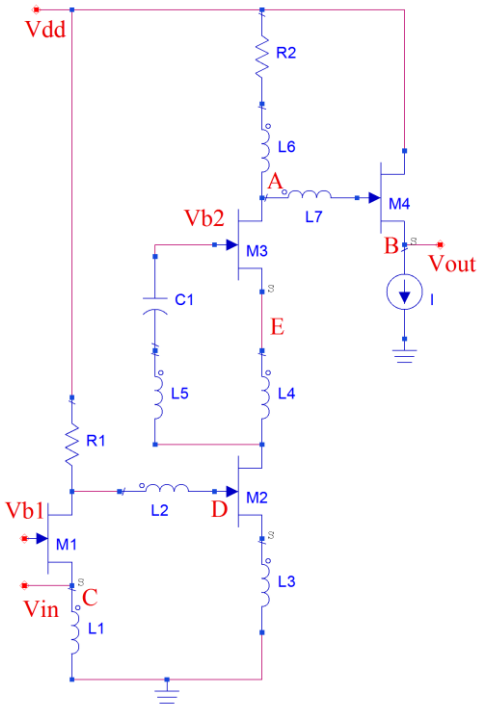


Fig 1: Basic LNA

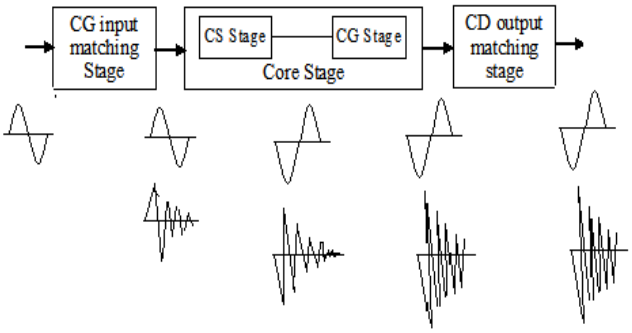


Fig 2: Analysis of basic LNA

The schematic representation of the noise analysis of the basic LNA is shown in figure 2.The noise figure (NF) of the three stages are given by the equations 1, 2 and 3. The total noise factor is obtained by using the Frii's formula and it is given by the equation 10. The gain of the three stages is given by the equations 3, 7 and 8 respectively. The total gain is given by the equation 9. When the gain is increased, the net noise figure will get reduced.

$$NF_1 = 1 + \frac{\gamma}{g_{m1} R_s} + \frac{R_S}{R_1}\left(1 + \frac{1}{g_{m1} R_s}\right)^2 \quad (1)$$

$$NF_2 = 1 + \frac{2}{3}\frac{1}{g_{m2} R_s^2} + \left(\frac{f}{f_T}\right)^2 \frac{2}{3}\frac{1}{g_{m2} R_S} \quad (2)$$

$$NF_3 = 1 + \frac{\gamma\left(\frac{1}{g_{m4}}\right)^2}{R_S\left(\frac{g_{m4} r_{04}}{1 + g_{m4} r_{04}}\right)} \quad (3)$$

$$A_{V1} \approx g_{m1} R_1 \quad (4)$$

$$A_{V21} = g_{m2}\left(\left(S L_4 + \frac{1}{SC_1} + S L_5\right) \| \frac{1}{S C_{gs3}}\right) \quad (5)$$

$$A_{V22} = g_{m3}\left(\left(SL_6 + R_2 + SL_7\right) \| \frac{1}{S C_{gs4}}\right) \quad (6)$$

$$A_{V2} = A_{V21} A_{V22} \quad (7)$$

$$A_{V3} = \frac{g_{m4} r_{04}}{1 + g_{m4} r_{04}} \quad (8)$$

$$A_V = A_{V1} A_{V2} A_{V3} \quad (9)$$

$$NF_{tot} = NF_1 + \frac{NF_2}{A_{V1}} + \frac{NF_3}{A_{V1} A_{V2}} \quad (10)$$

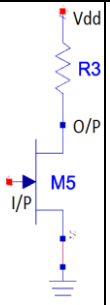
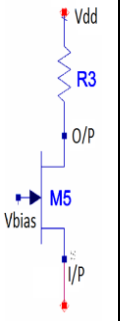
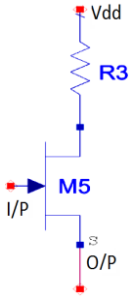
where g_{m1}, g_{m2}, g_{m3} and g_{m4} are the transconductance of M_1, M_2, M_3 and M_4 respectively. R_S is the source resistance, f_T is the transition frequency, r_{04} is the output resistance.

4. PROPOSED ACTIVE FEEDBACK TOPOLOGIES AND FEEBACK NETWORKS

A physical understanding of both intrinsic and extrinsic noise mechanisms in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is necessary while designing LNA [8]. The different sources of noise in LNA are channel thermal noise, gate induced noise, flicker noise, shot noise and substrate noise. In order to reduce the NF of the LNA, different feedback techniques are employed in this basic circuit. A Feedback amplifier is the one in which part of the output signal is fed back to the input. There are four different feedback topologies. They are shunt-shunt feedback, series-shunt feedback, series-series feedback, shunt-series feedback. In this work, shunt-shunt feedback technique which is also called as transresistance is employed. The shunt-shunt feedback is employed in three ways. From the figure 1, when the feedback is taken from the point B and given to the point C, it is called as global feedback and its block diagram representation is shown in figure 3 and 4. When the feedback is taken from the point A and given to the point D, it is called as local full feedback and its block diagram representation is shown in figure 5 and 6. When the feedback is taken from the point E and given to the point D, it is called as local partial feedback and its block diagram representation is shown in figure 7 and 8.

The feedback network may be passive or active. The passive feedback network consists of resistor and the active feedback network consists of CG, CS and CD configurations. The global feedback, local full and local partial feedback with the different feedback network as mentioned above are simulated and analyzed and the conceptual representation of how noise gets reduced are analyzed. The different feedback network and its feedback factor (β) are shown in the table 1.

Table 1. Feedback Network and its feedback factor (β)

	R	CS	CG	CD
Feedback network				
Feedback factor(β)	$\beta = \frac{1}{R_3}$	$\beta = g_{m5}$	$\beta = g_{m5} + \frac{1}{r_0}$	$\beta = g_{m5}(\frac{R_3}{r_0 + R_3})$

4.1 Global Feedback

In global feedback, the feedback is taken from the output stage and given to the input stage. The feedback may be positive or negative. The input signal is given to the CG input stage and is amplified by the cascode stage in which CS in the cascode stage causes an 180^0 phase shift and the output stage does not cause any further phase shift. Hence if the feedback network causes a phase shift of 180^0, it will be a positive feedback otherwise the feedback will be negative feedback. Therefore, if the feedback network consists of CS network, it will be positive feedback and for the other feedback networks, the feedback will be negative.

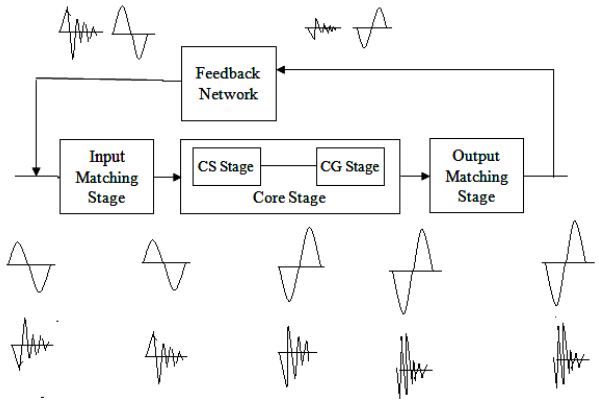


Fig 3: Analysis of global feedback with CS network

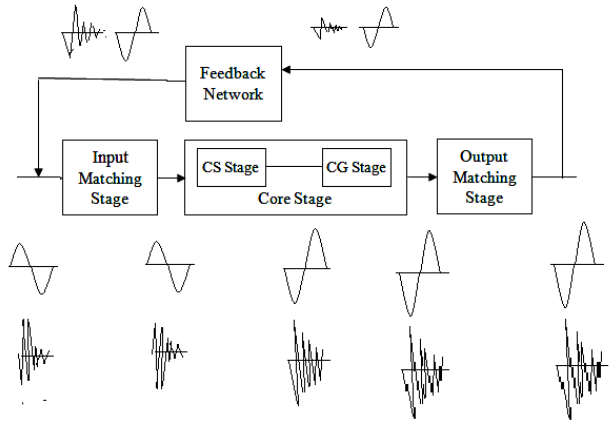


Fig 4: Analysis of global feedback with CG/CD/R network

The conceptual representation of signal and noise voltages at various stages of global feedback with CS network is shown in figure 4. From the figure 4, the input signal is applied to the CG input stage. The CG configuration has noise voltages which are equal in magnitude and opposite in phase at source and drain terminal.

The CS stage will amplify this signal causing a phase shift of 180^0 and also the noise from the CS stage will get added. As the phase of the noise signal is arbitrary, if the noise voltage from CS stage is in phase with the noise from the previous stages, then the total noise will increase and if the noise voltage from CS stage is out of phase with the noise from the previous stages, then the total noise will decrease. Let us consider the worst case possibility that the noise voltages are in phase so that the total noise voltage is increased. The amplified signal with the increased noise is given to the CG stage. As the noise voltages at the source and drain terminal of CG stage are out of phase, the noise added at the input terminal of CG stage will get cancelled at the drain terminal of the CG stage. Thus, the total gain and noise figure of the cascode stage is dominated by the CS stage. The signal along with the noise is then given to the CD stage. The CD stage has gain less than unity and hence the signal will not be amplified

and noise will get increased due to the internal noise of CD stage. A part of this output is given as the feedback to the input stage. When the feedback network is resistive or CG or CD, the feedback is positive. The feedback signal will get amplified and noise from the feedback network also gets added up. At the input stage, the feedback noise and the input noise are in phase and hence the noise will get added up.

The conceptual representation of signal and noise voltages at various stages of global feedback with CG/CD/resistive is shown in figure 5. When the feedback is CS, the feedback will be negative. The feedback signal will get amplified with a phase shift of 180^0 and noise from the feedback network also gets added up. At the input stage, the feedback noise and the input noise are out of phase and hence the noise will get reduced. The total noise factor will get reduced by factor of $(1+A_v\beta)$ for CS feedback and it get increased by factor of $(1+A_v\beta)$ for other feedback network as given by the equation 11 and 12 respectively.

$$NF = \frac{NF_{tot}}{(1+A_v\beta)} \tag{11}$$

$$NF = NF_{tot}(1+A_v\beta) \tag{12}$$

4.2 Local Feedback

In local full feedback, the feedback is taken from the output of the CG stage and given to the input of the CS stage. In local partial feedback, the feedback is taken from the output of the CS stage and given to the input of the CS stage.

The conceptual representation of signal and noise voltages at various stages of local full feedback with CD/CG/R network is shown in figure 5.The analysis of the signal and the noise voltages at the various stages without the feedback are same as the global feedback. As the feedback is taken at output of the CG stage and given at the input of the CS stage, the feedback noise voltage will be out of phase with the noise voltage at the input of the CS stage and hence the noise gets reduced when the feedback network is CD/CG/R.

The conceptual representation of signal and noise voltages at various stages of local full feedback with CS network is shown in figure 6. As the feedback network with CS causes a phase shift of 180^0, the feedback noise voltage will be in phase with the noise voltage at the input of the CS stage and hence the noise gets increased for the local full feedback with CS network.

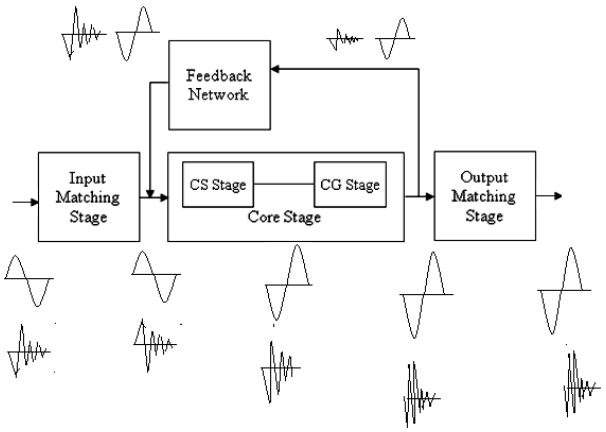


Fig 5: Analysis of local full feedback with CG/CD/R network

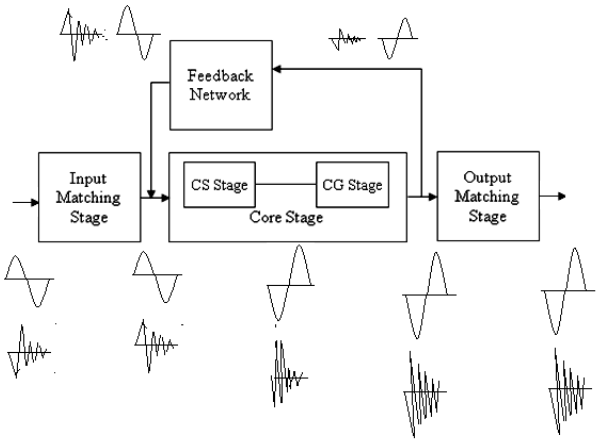


Fig 6: Analysis of local full feedback with CS network

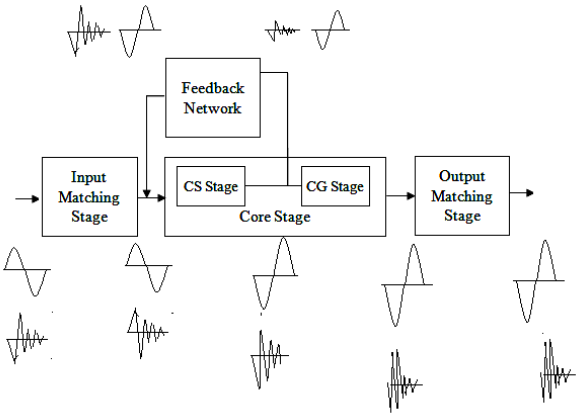


Fig 7: Analysis of local partial feedback with CG/CD/R network

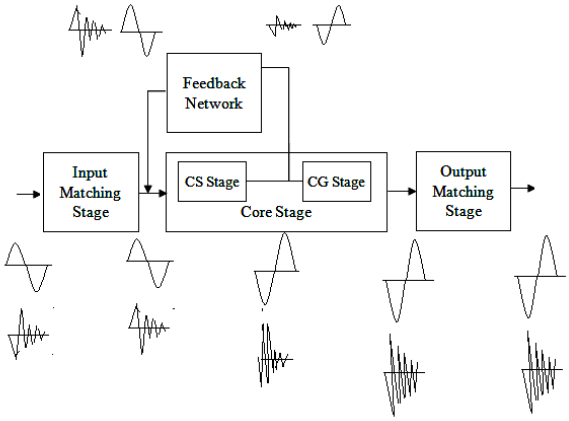


Fig 8: Analysis of local partial feedback with CS network

The conceptual representation of signal and noise voltages at various stages of local partial feedback with CD/CG/R network is shown in figure 7. As the total noise at the output of the CS stage consists of the noise contributed by the CG stage of the cascode stage, the noise at the output of the CS stage will be more when compared to the noise at the output of the CG stage. The feedback noise voltage will be out of phase with the noise voltage at the input of the CS stage and

hence the noise gets reduced for the local partial negative feedback. The noise cancelled will be more when compared to the local full feedback with CD/CG/R network.

The conceptual representation of signal and noise voltages at various stages of local partial feedback with CS network is shown in figure 8. As the feedback network with CS causes a phase shift of 180^0, the feedback noise voltage will be in phase with the noise voltage at the input of the CS stage and hence the noise gets increased for the local partial feedback with CS network. The noise factor of the second stage will get reduced by factor of $(1+A_{v2}\beta)$ for CG/CD/R feedback and it get increased by factor of $(1+A_{v2}\beta)$ for CS feedback network as given by the equation 13 and 14 respectively.

$$NF = \frac{NF_2}{(1+A_{V2}\beta)} \quad (13)$$

$$NF = NF_2(1+A_{V2}\beta) \quad (14)$$

5. RESULTS AND DISCUSSION

The simulation results of the proposed LNA are obtained using Agilent's ADS simulator. Post layout simulations are also carried out. A 90 nm CMOS technology file is used for the simulation purposes. The results are elaborated in the following sections and are summarized and shown in table 2. Along with the proposed topologies results, already existing topologies such as signal nulled feedback, feedforward and global resistive feedback concepts are taken and implemented in basic circuit and the results are compared.

Basic Circuit
Local full resistive fb
Local partial resistive fb
Local full CS fb
Local partial CS fb
Local full CG fb
Local partial CG fb
Local full CD fb
Local partial CD fb
Global CS fb
Global CG fb
Global CD fb

5.1 Power Gain (S21)

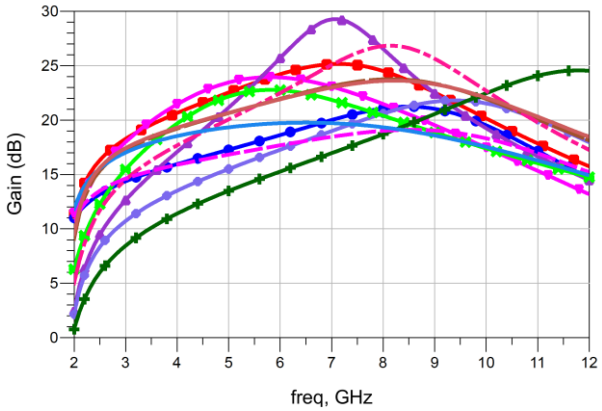


Fig 9: Power Gain (S21)

For the LNA to have better performance, power gain should be high so that the noise added at the subsequent stages will have less effect. It can be inferred from the figure 9 that full CS feedback has peak gain of 29.2 dB due to positive feedback but it has poor noise performance. The local partial CD and CG feedback has peak gain of 23.75 and 23.8 dB with reduction in gain of around 1.5 dB from the base circuit due to negative feedback but it has good noise performance.

5.2 Noise Figure

In the proposed techniques, the global feedback with CS network has less noise figure of 5.7-6.7 dB when compared to the global feedback with CG network noise figure of 9.7-10.2 dB as seen in figure 10. It can be seen that partial CG feedback has NF in the range 6.1-6.3 dB and partial CD feedback has NF in the range 4.6-5.8 dB. All the other techniques except the feedback with CS network have NF in the range 7.1-7.4 dB.

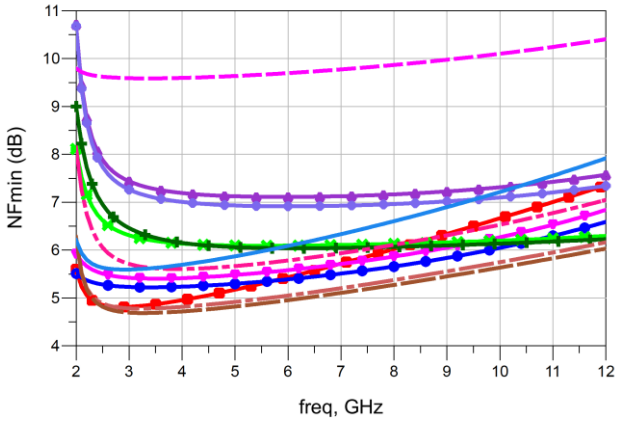


Fig 10: Noise Figure (NFmin)

5.3 Input matching and Output matching

All the techniques has good input matching with input reflection coefficient < -7.5 dB as seen from the figure 11. From the figure 12, the output reflection coefficient of all the topologies except CS network and global CG network are less than < -7.2 dB.

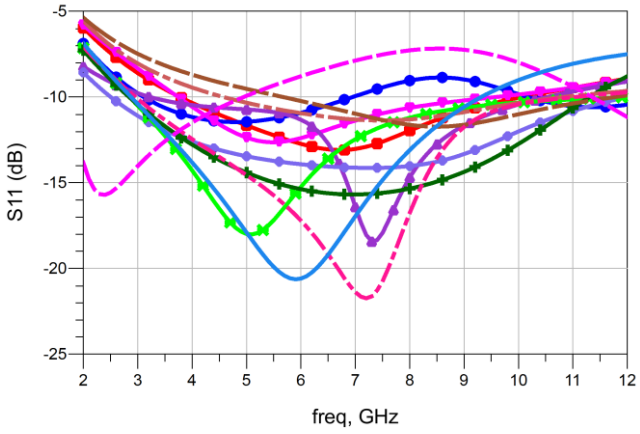


Fig 11: Input reflection coefficient

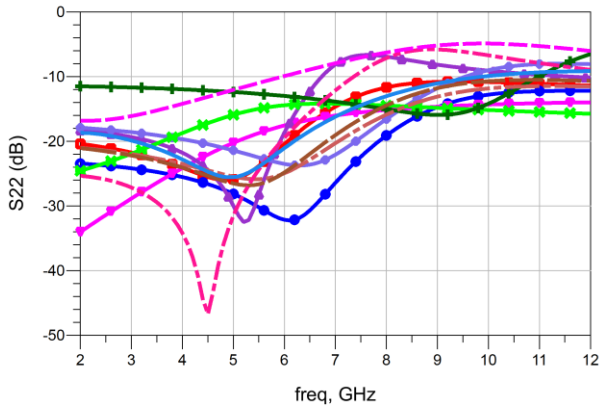


Fig 12: Output reflection coefficient

5.4 Stability factor k and Δ

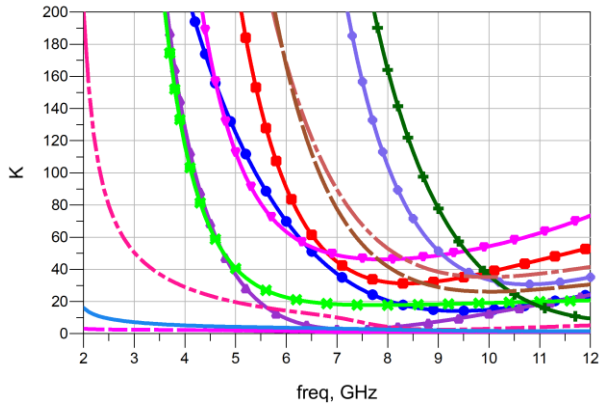


Fig 13: Stability factor, k

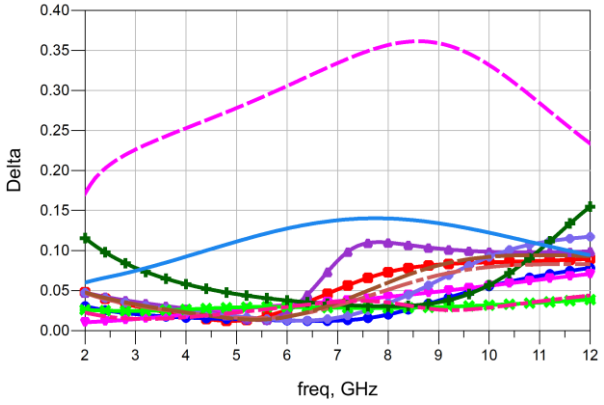


Fig 14: Stability factor, Δ

The stability of an amplifier is an important constraint while designing an amplifier. The stability factor is determined from the S parameter. The Rollett's stability condition states that k should be greater than 1 and Δ should be less than 1.These topologies are stable as k>1 and Δ<1 as seen from the figure 13 and 14.

5.5 Linearity (IIP3)

From the figure 15, all these topologies have linear response as the signal power is limited to only -41.3 dBm. Thus, by comparing the existing and the proposed topologies, proposed partial CG and CD active feedback has better performance.

Table 2. Comparison results and analysis

		BW (GHz)	S21 in dB	Nfmin in dB	S11 in dB	S22 in dB	IIP3 in dBm
Base circuit [5]		3-11	25.163	4.8-7	<-8.6	<-10	-12.5
Global resistive feedback [3]		3-11	15.174	4.7-7.2	<7.7	<-7.7	-14.5
Global signal nulled feedback [4]		3-11	12.268	4.2-7.9	<-9	<-7.2	-12.5
Feed forward [2]		3-11	18.111	4.2-7.8	<-10	<-7.8	-11
Proposed techniques	Local full resistive feedback	3-11	21.228	5.2-6.2	<-9	<-12	-18
	Local partial resistive feedback	3-11	23.945	5.4-6.5	<-8	<-14	-15
	Local full CS feedback	3-11	29.203	7.1-7.4	<-9.6	<-6.6	1.25
	Local partial CS feedback	3-11	21.8	7-7.2	<-10	<-8	4
	Local CG feedback	3-11	22.7	6.1-6.3	<-10	<-15	2.9
	Local partial CG feedback	3-11	23.8	6.1-6.3	<-10	<-10	-12.7
	Local full CD feedback	3-11	23.5	4.7-5.9	<-8	<-11	-11.125
	Local partial CD feedback	3-11	23.75	4.6-5.8	<-7.5	<-10	-12
	Global CS feedback	3-11	26.837	5.7-6.7	<-10	<-5.8	-15
	Global CG feedback	3-11	19.105	9.7-10.2	<-7.5	<-5	-8.375
	Global CD feedback	3-11	19.763	5.5-7.5	<-7.8	<-9.1	-15

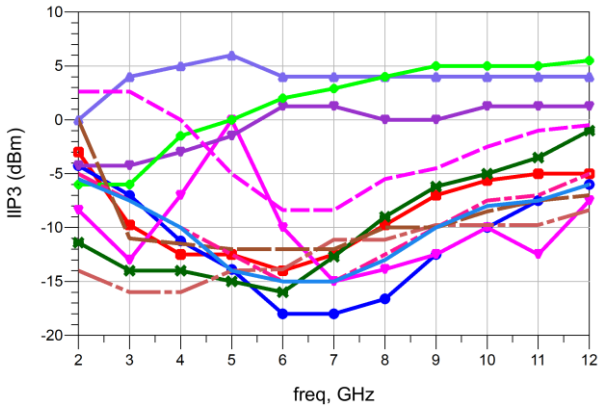


Fig 15: Linearity, IIP3

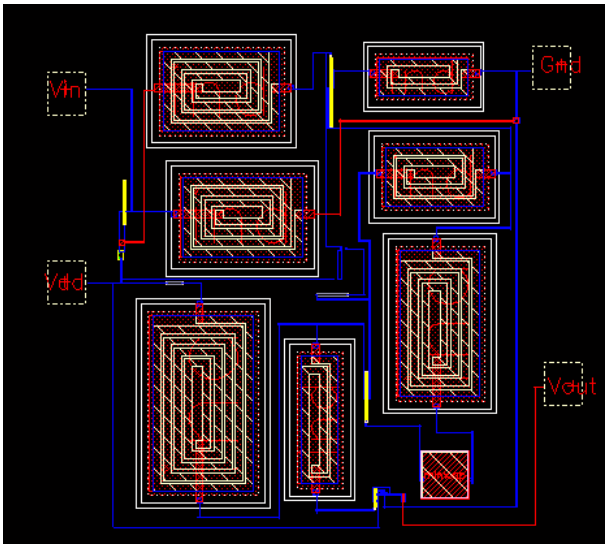


Fig 16: Layout of partial CD feedback

The Layout of the partial CD feedback is shown in figure 16. Similarly the layouts for other configurations are drawn and simulated. The area occupied is .344 x .321 mm^2.

6. CONCLUSION

In the proposed topologies, local feedback techniques such as CG and CD partial active feedback give better noise performance. CG partial active feedback gives noise factor of 6.1-6.3 dB and gain of around 23.8 dB where as partial CD feedback gives the noise factor of 4.6-5.8 dB, gain of around 23.75 dB. All the techniques has good input matching with input reflection coefficient < -7.5 dB and the output reflection coefficient of all the topologies except CS network and global CG feedback are less than < -7.2 dB. From the analysis, it is found that proposed topologies have good stability and moderate linearity.

7. REFERENCES

[1] Stephen Wood and Roberto Aiello, "Essentials of UWB", Cambridge Univ. Press, 2008.

[2] Chao-Shiun Wang, Chorng-Kuang Wang, "A 90nm CMOS Low Noise Amplifier Using Noise Neutralizing for 3.1-10.6GHz UWB System" Proc. of 32nd European Solid State Circuit Conf., pp. 251-254,2006..

[3] Jianyun Hu, Yunliang Zhu, and Hui Wu, "An Ultra-wide Band Resistive feedback Low noise amplifier with noise cancellation in 0.18µm Digital CMOS", IEEE Topical meeting on Silicon monolithic integrated circuits in RF system, pp. 218-221,2008.

[4] Chin-Fu Li *et al.*, "A Power-Efficient Noise Suppression Technique Using Signal-Nulled Feedback for Low Noise Wideband Amplifiers", IEEE Transactions on Circuits And Systems-II: Express Briefs, Vol. 59, No. 1, pp. 1-5, 2012.

[5] Vaithianathan Venkatesan, Raja Janakiraman and Srinivasan Raj, "A 90nm CMOS Low Noise Amplifier with Shunt –Series Peaking for Ultra Wide Band Communication Systems", International Journal of Electrical Engineering, Vol. 5, No. 4, pp. 489-500, 2012.

[6] Yeo Myung Kim, Honggul Han and Tae Wook Kim, "A 0.6-V +4 dBm IIP3 LC Folded Cascode CMOS LNA With gm Linearization", IEEE Transactions on Circuits and Systems—ii: Express Briefs, Vol. 60, No. 3, pp. 122-126, 2013.

[7] Xiaohua Fan, Heng Zhang and Edgar Sánchez-Sinencio, "A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA", IEEE Journal of Solid-State Circuits, Vol. 43, No. 3,pp. 588-599,2008.

[8] Renuka P. Jindal,"Compact Noise Models for MOSFETs', IEEE Transactions on Electron Devices, Vol. 53, No. 9, pp. 2051-2061,2006.