Design of Low Transition Pseudo-Random Pattern Generator for BIST Applications

Lubna Naim
M.Tech Student
Electronics Circuit and System
Integral University

Tarana A. Chandel
Jr. Associate Professor
Department of Electronics & Communication
Integral University

ABSTRACT
Built in self testing (BIST) is most attractive technique to test different kind of circuits. In BIST, test patterns are generated by different techniques of test pattern generation and applied to the circuit under test (CUT). In pseudorandom BIST architecture, test patterns are generated by Linear Feedback Shift Register (LFSR). Due to high Switching in pattern generation by conventional LFSR, power dissipation is high in conventional LFSR. Power is an important constraint in VLSI (Very Large Scale Integration) testing.
This paper presents a modification in LFSR to generate pattern for BIST applications with reduced power requirement. This new technique represent low transition pattern pseudorandom generator (LT-PRG) for Test-per-Clock and Test-per-Scan BIST applications. The LT-PRPG is designed with the use of a LFSR and a 2x1 multiplexer. Experimental results show that the implementation of Bit-Swapping LFSR can reduce the internal transition activity probability which directly affect the dissipation of power in CUT without affecting the fault coverage.

Keywords
Built-in-Self-Test(BIST), Bit-Swapping LFSR(BS-LFSR), Weighted Switching activity, Test pattern generation, Transition, Low Power

1. INTRODUCTION
In Modern age, the greatest challenge is to design low power reliable designs of Very Large Scale Integration (VLSI) Integration. There are many techniques introduced to reduce the power consumption in normal mode operation. However power dissipation in test mode operation is not predominant concern. However power dissipation is much higher in test mode operation than normal mode operation because of internal switching of CUT nodes [1]-[3].

2. BIST SCHEMES
BIST schemes can be divided into two main types according to the way in which test patterns are applied to the CUT, the two schemes are the test-per-clock and the test-per- scan [4].

2.1 Test-per-clock
Basically BIST uses same process of testing as off-line testing using ATE where the test pattern generator and test response analyzer are on-chip circuitry (instead of equipment). Designers need to design a circuit for compressed implementation of test pattern generator and response analyzer due to replacement of equipment by circuitry [5]. Figure 1 shows the basic architecture of Test-per-clock. In this architecture LFSR is used as a test pattern generator .For normal mode operation multiplexer is used to allow normal inputs to the circuit, on the other side when this architecture is work in test mode LFSR generate test input for testing. Central test controller is responsible for the generation of test inputs of multiplexer. Output Response Compacter (ORC) performs compression of the outputs of CUT.ORC shows losses in compression. For testing we compare actual results with expected results as here in BIST we compare the outputs of CUT with expected result (called golden signature). The actual result should match expected result, if it is not matched with each other than fault is detected. Compacted CUT response is compared with golden signature, which is stored in ROM.

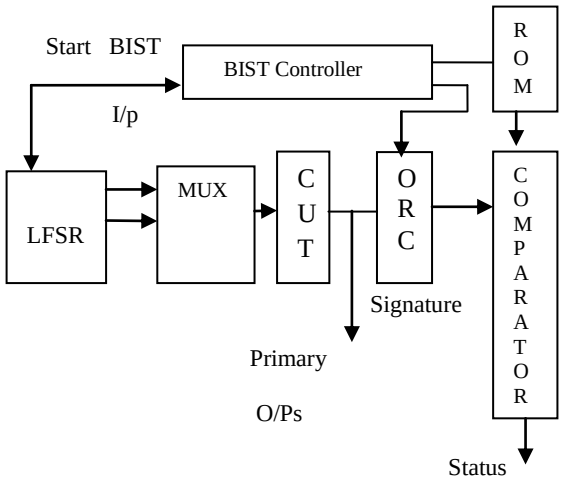


Figure 1 Basic architecture

2.2 Test-per-scan
Here we discussed modified Test-per-Scan scheme [6], which is based on Low Transition Random Pattern Generator (LT-PRG). LT-PRG reduces transition at scan inputs during scan shift operation of BIST. Figure 2 shows the architecture of LT-PRG. This architecture is designed by using r stage LFSR, a K-input AND gate, and a T flip-flop. Either normal or inverting outputs of LFSR stages are connected to each of K inputs of the AND gate. If we increase the no of K then it will increase the length of test sequence and decrease the fault coverage so in this architecture we used the value of K= 2 or 3. T flip-flop remains in its state and hold the previous value as long as the input of the T flip-flop is set at 1. T flip-flop changes its state in every few clock cycles because in most of the cases output of the AND gate is zero (input of T flip-flop), so in scan chain have same value for most of the cases. In result of this transition probability in CUT will decrease.

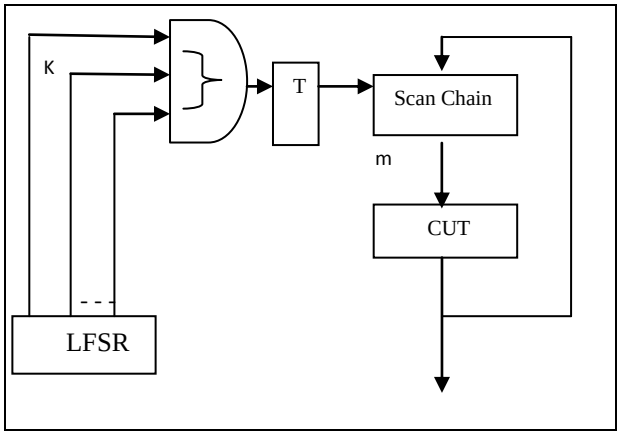


Figure 2 Test-per-scan

3. MODIFIED TEST PATTERN GENERATOR

Basically bit-swapping LFSR in figure 3 is a modified form of conventional LFSR, which generate Pseudo-Random pattern at output of LFSR with reduced transition between 0 and 1 that occur in the output stream of LFSR. Due to reduction of internal switching activity Bit-Swapping LFSR is useful for reduction of average power dissipated by CUT. Bit-Swapping LFSR can be implemented either in Test-per-Scan or Test-per-Clock scheme for reduction of power. Internal reduction of switching directly affects the consumed power by CUT.

3.1 General architecture of BS-LFSR

Figure 3 shows Implementation of general architecture of Bit Swapping LFSR, which reduces the average and instantaneous, weighted switching activity (WSA) during test operation by reducing the number of transition.

Design of Bit Swapping LFSR is based on some lemmas which are used to describe the Transition activity in Bit Swapping LFSR. With the help of these lemmas we can easily define how the switching and transition of bits take place in pattern generation. These lemmas give the surprisingly good results in order to save power. For the test-per clock and test-per-scan we have different lemmas. A next section introduces lemmas about Bit Swapping LFSR in test-per clock and test-per scan schemes.

There are several techniques to reduced power consumption. There is direct technique, if we used reduced frequency during testing it will reduced power dissipation. In this direct technique there is no requirement of extra hardware [25, 26]. Second direct technique to reduced power consumption is to apply appropriate testing planning by doing portioning of CUT into block.

These direct techniques increase the timing of testing and are not applicable for reduction peak power. In contrast to the other techniques Bit-Swapping LFSR reduce average and peak power dissipated by CUT.

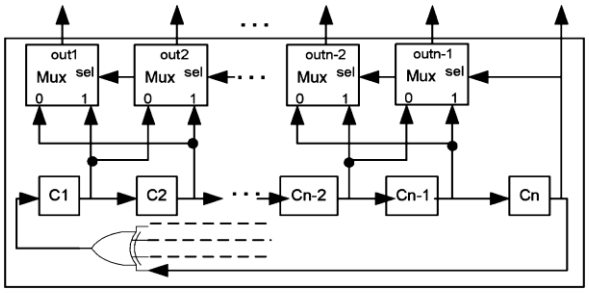


Figure 3 General architecture of Bit swapping LFSR

4. GENERAL OBSERVATION FOR BS-LFSR

Bit-Swapping LFSR is based on some observations depending upon number of transition produced by LFSR at the output. In modified form of normal LFSR we used swapping property between every pair of adjacent cells of normal LFSR to design Bit-Swapping LFSR [21,22].

General observation for LFSR- For any n-bit maximal-length LFSR that starts with any seed and runs for 2^n clock cycles until it returns to the starting seed value, then the total number of transitions T_{total} that occurs is given by the formula in equation (1):

$$T_{total} = n \times 2^{(n-1)} \quad (1)$$

Observation for swapping Bits in BS-LFSR- If we take an example of any n-bit maximal length LFSR (n>2) and modified this LFSR for swapping arrangement, we consider one of its outputs (say bit n-the last bit) to be a selection line that will swap two neighboring bits elsewhere in the LFSR at specific value of selection line. If we set the value of selection line at 0 for swapping then n is odd and bit n =0, bit 1 will be swapped with bit 2, bit 3 with bit 4…bit n-2 with bit n-1. If n is even and bit n =0, then bit will be swapped with bit 2, bit 3 with bit 4,……bit n-3 with bit n-2, in all cases the selection line (n bit) has no effect on swapping operation. If bit n =1, then no swapping is performed. In this case:

1. Modified LFSR will be generate exactly same as normal (unmodified) LFSR. Order of generated test pattern by modified LFSR will be different.

2. Swapping arrangement will save a number of transitions, swapped bits will save number of transition equal to $T_{Saved} = 2^{(n-2)}$. In contrast, in general observation two bits (un-swapped bits) originally produced $2 \times 2^{(n-1)}$ so after swapping the swap bit will therefore save $T_{Saved} = 2^{(n-2)}/(2 \times 2^{(n-1)} = 25\%$.

5. IMPLEMENTATION OF BIST ARCHITECTURE (WITH BS-LFSR)

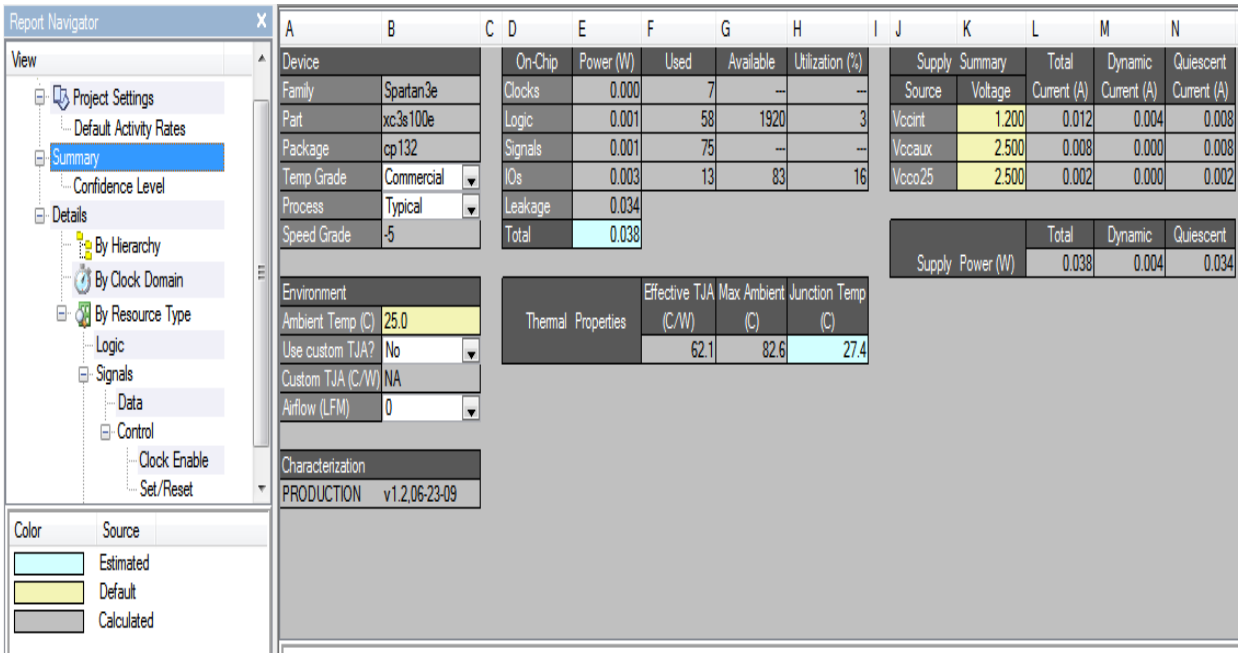
In implementation of Test-per-Clock and Test-per-Scan BIST architectures, we replaced conventional LFSR with Bit-Swapping LFSR in figure 1 and figure 2. Implemented architectures show reduction in power consumption by CUT during testing operation.

6. EXPERIMENTAL RESULTS

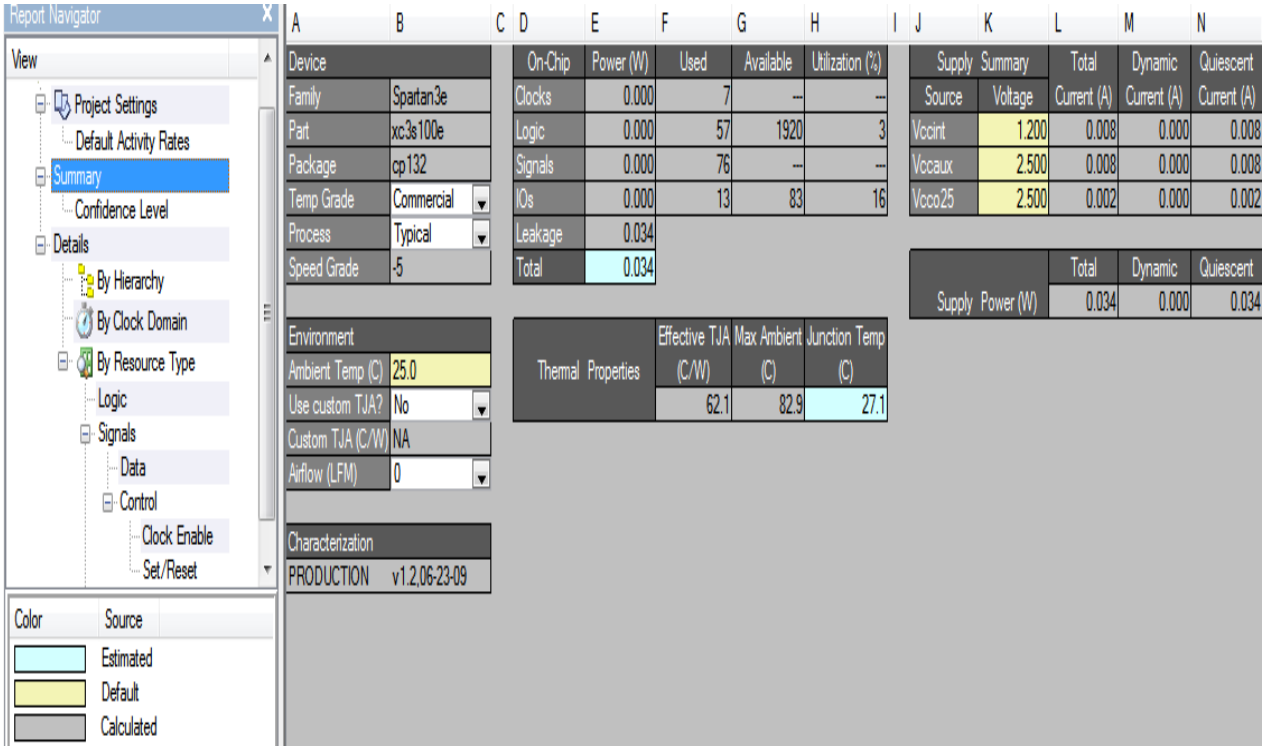
We used VHDL and xillinx tool for simulation of Test-per-Clock and Test-per-Scan BIST schemes. We used S27 sequential circuit (ISCAS 89 Family) as a Circuit under Test (CUT).

5.1 Test-per-clock BIST power results

5.1.1. with Normal LFSR

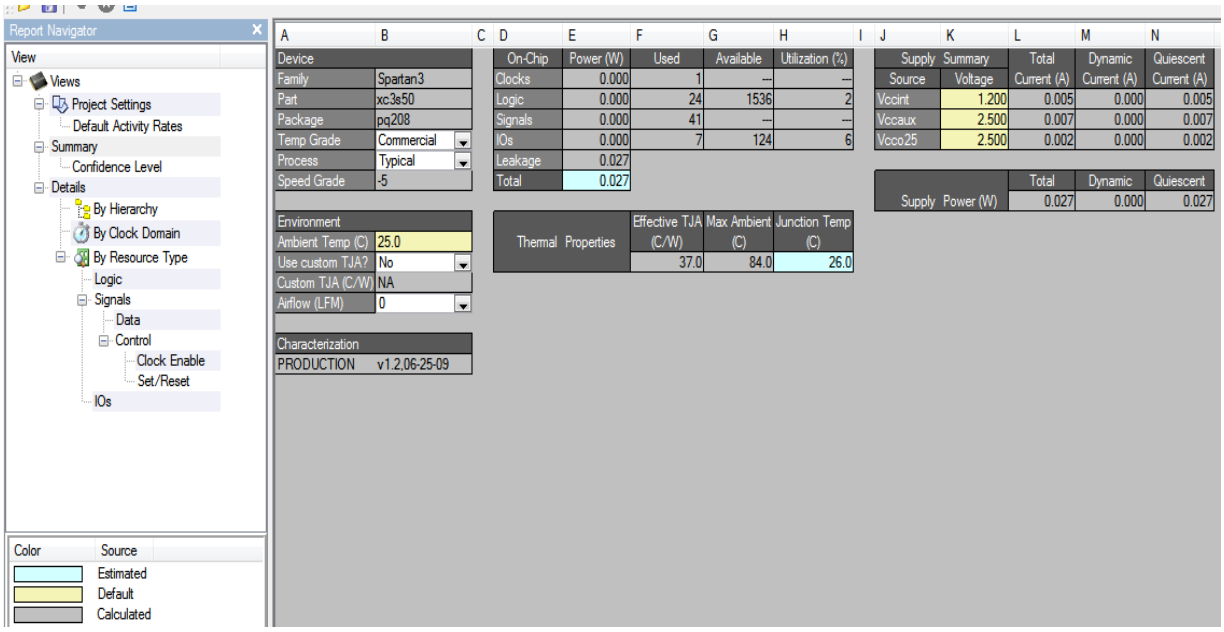


5.1.2 with BS-LFSR

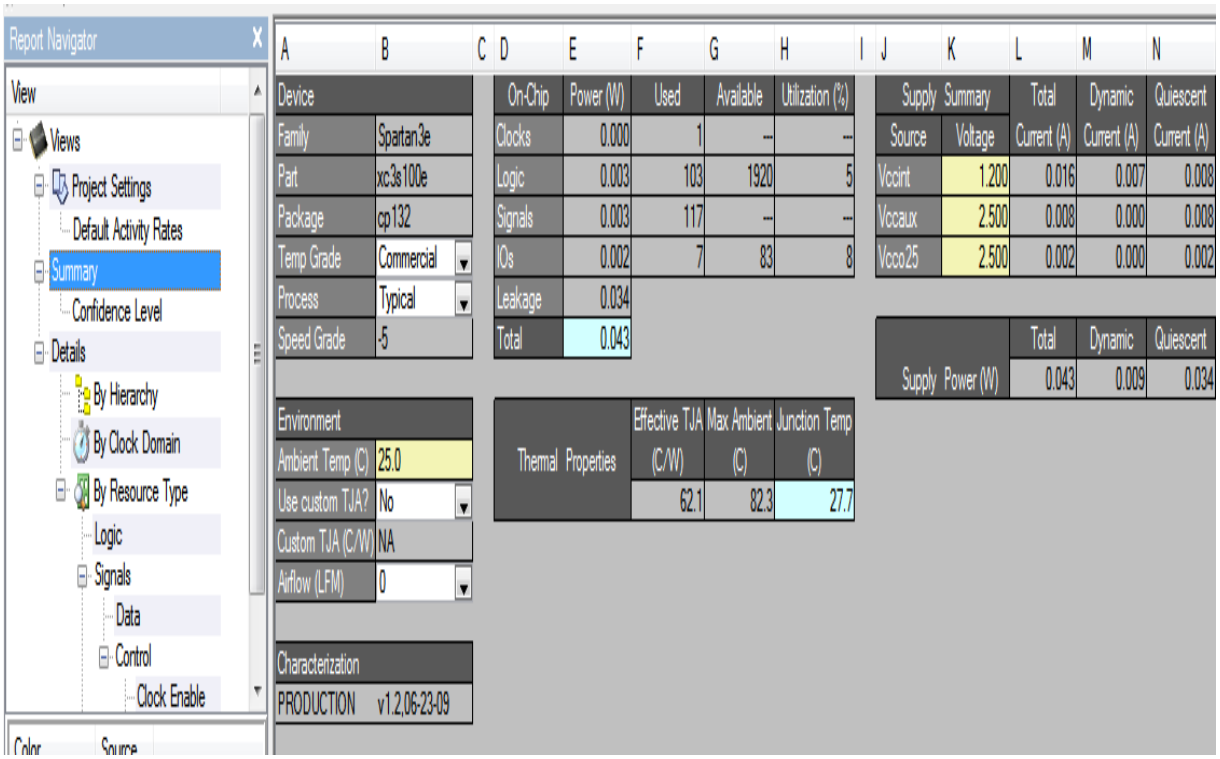


5.2 Test-per-Scan BIST power results

5.2.1 with Bit-Swapping LFSR



5.2.2 With Normal LFSR



7. CONCLUSION

Comparisons between the implemented design and conventional architectures show that the implemented design can achieve better results for most tested benchmark circuits. Bit Swapping LFSR reduces transition activity which reduces weighted switching activity and shows good results for power consumption.

8. FUTURE SCOPE

To improve power dissipation in testing mode we can use this technique of pattern generation as called Bit Swapping LFSR with other techniques of transition reduction. In future we can investigate the properties of LFSR to improve the test pattern generation.

9. REFERENCES

[1] Y. Zorian, ―A distributed BIST control scheme for complex VLSI devices in Proc. 11th IEEE VTS, Apr. 1993, pp. 4-9.

[2] A. Hertwig and H. J. Wunderlich, ―Low power serial built-in self-test in Proc. IEEE Eur. Test Workshop, May 1998, pp. 49-53.

[3] P. H. Bardell, W. H. McAnney, and J. Savir, Built-in Test for VLSI: Pseudorandom Techniques. New York: Wiley, 1997

[4] M. Bushnell and V. Agrawal, Essentials of Electronic Testing for Digital, Memory, and Mixed Signal VLSI Circuits, Kluwer Academic Publishers (2002).

[5] Ajit Kumar Mohanty, Biswanath Pratap Sahu, Chandan Patnaik, S. S. Mahato.”Low Power Test Pattern Generator for System on Chip Architecture”, International Conference on Computing, Communication and Sensor Network (CCSN)

[6] S. Wang and S. K. Gupta, ‘‘LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation” *University* of *Southern California Computer Engineering Technical Report CENG*- 99-05, 1999.

[7] Seagmoon Wang ,, “ A BIST TGP for low power dissipation and high fault coverage”, IEE transaction on very large scale integration (VLSI) system, vol.15, no.7 july 2007

[8] P. Girard, "Survey of low-power testing of VLSI circuits", IEEE Design and Test of Computers, 19(3), pp. 80-90, June 2002. P. Girard, X. Wen, and N. Touba, Low power testing, in System On Chip Test Architectures, L.-T. Wang, C.A. Stroud, and N. Touba, Editors, Morgan Kaufmann. pp. 307-350, 2008.

[9] P. Girard, "Survey of low-power testing of VLSI circuits", IEEE Design and Test of Computers, 19(3), pp. 80-90, June 2002

[10] M. Bushnell and V. Agrawal, Essentials of Electronic Testing for Digital A Memory, and Mixed Signal VLSI Circuits, Kluwer Academic Publishers, 2002.

[11] V. Agrawal, C.R. Kime, and K. Saluja, "A tutorial on built-in self-test - part 1: principles", IEEE Design and Test of Computers, 10(1), pp. 73-82, March 1993.

[12] V. Agrawal, C.R. Kime, and K.K. Saluja, "A tutorial on built-in self test - part 2: applications", IEEE Design and Test of Computers, 10(1), pp. 69-77, June 1993.

[13] V. Agrawal, C.-J. Lin, P.W. Rutkowski, S. Wu, and Y. Zorian, "Built-in self-test for digital integrated circuits", AT&T Technical Journal, pp. 30-39, March 1994

[14] P.H. Bardell, W.H. McAnney, and J. Savir, Built-in test for VLSI: pseudorandom techniques, John Wiley & Sons, 1987.

[15] R. Aitken, "Nanometer technology effects on fault models for IC testing", Computer, 32(11), pp. 46-51, November 1999.

[16] R. Garcia, "Rethink fault models for submicron-IC test", Test and Measurement World, 21(12), pp. 35-40, October 2001.

[17] H.K. Lee and D.S. Ha, "An efficient forward fault simulation algorithm based on the parallel pattern single fault propagation", Proceedings of the 1999 International Test Conference, pp. 946-955, October 1991.

[18] 18. P.H. Bardell and W.H. McAnney, "Pseudorandom arrays for built-in test", IEEE Transactions on Computers, C-35(7), pp. 653-658, July 1986.

[19] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low power CMOS digital design", IEEE Journal of Solid-State Circuits 27(4), pp. 473-484, April 1992.

[20] M. Pedram, "Power minimization in IC design: Principles and applications", ACM Transactions on Design Automation of Electronic Systems (TODAES), 1(1), pp. 3-56, January 1996.

[21] P.H. Bardell, W.H. McAnney, and J. Savir, *Built-in test for VLSI: pseudorandom techniques*, John Wiley & Sons, 1987.

[22] R. David, *Random Testing of Digital Circuits, Theory and Applications*, Marcel Dekker Inc., 1998.

[23] A.S. Abu-Issa and S.F. Quigley, “Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak and Average Power Reduction in Scan-Based BIST”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 28(5), May 2009, pp. 755-759.

[24] A.S. Abu-Issa and S.F.Quigley, “Bit-Swapping LFSR for Low Power BIST”, Electronics Letters, 44(6), March 2008, pp. 401- 403.

[25] J. Monzel, S. C hakravarty, V. Agrawal, R. Aitken, J. Braden, J. Figueras, S. Kumar, H. Wunderlich, and Y. Zorian, "Power dissipation during testing: Should we worry about it?" *15th IEEE VLSI Test Symposium*, pp. Panel Session, April 1997.

[26] J. Saxena, K.M. Butler, and L. Whetsel, "An Analysis of power reduction techniques in scan testing", *Proceedings of International Test Conference*, pp. 670-677, October 2001.