ABSTRACT
Built in self testing (BIST) is most attractive technique to test different kind of circuits. In BIST, test patterns are generated by different techniques of test pattern generation and applied to the circuit under test (CUT). In pseudorandom BIST architecture, test patterns are generated by Linear Feedback Shift Register (LFSR). Due to high Switching in pattern generation by conventional LFSR, power dissipation is high in conventional LFSR. Power is an important constraint in VLSI (Very Large Scale Integration) testing.
This paper presents a modification in LFSR to generate pattern for BIST applications with reduced power requirement. This new technique represent low transition pattern pseudorandom generator (LT-PRG) for Test-per-Clock and Test-per-Scan BIST applications. The LT-PRG is designed with the use of a LFSR and a 2x1 multiplexer. Experimental results show that the implementation of Bit-Swapping LFSR can reduce the internal transition activity probability which directly affect the dissipation of power in CUT without affecting the fault coverage.

Keywords
Built-in-Self-Test(BIST), Bit-Swapping LFSR(BS-LFSR), Weighted Switching activity, Test pattern generation, Transition, Low Power

1. INTRODUCTION
In Modern age, the greatest challenge is to design low power reliable designs of Very Large Scale Integration (VLSI) Integration. There are many techniques introduced to reduce the power consumption in normal mode operation. However power dissipation in test mode operation is not predominant concern. However power dissipation is much higher in test mode operation than normal mode operation because of internal switching of CUT nodes [1]-[3].

2. BIST SCHEMES
BIST schemes can be divided into two main types according to the way in which test patterns are applied to the CUT, the two schemes are the test-per-clock and the test-per-scan [4].

2.1 Test-per-clock
Basically BIST uses same process of testing as off-line testing using ATE where the test pattern generator and test response analyzer are on-chip circuitry (instead of equipment). Designers need to design a circuit for compressed implementation of test pattern generator and response analyzer due to replacement of equipment by circuitry [5]. Figure 1 shows the basic architecture of Test-per-clock. In this architecture LFSR is used as a test pattern generator. For normal mode operation multiplexer is used to allow normal inputs to the circuit, on the other side when this architecture is work in test mode LFSR generate test input for testing. Central test controller is responsible for the generation of test inputs of multiplexer. Output Response Compacter (ORC) performs compression of the outputs of CUT.ORC shows losses in compression. For testing we compare actual results with expected results as here in BIST we compare the outputs of CUT with expected result (called golden signature). The actual result should match expected result, if it is not matched with each other than fault is detected. Compacted CUT response is compared with golden signature, which is stored in ROM.

![Figure 1](BIST_Schematic.png)

2.2 Test-per-scan
Here we discussed modified Test-per-Scan scheme [6], which is based on Low Transition Random Pattern Generator (LT-PRG). LT-PRG reduces transition at scan inputs during scan shift operation of BIST. Figure 2 shows the architecture of LT-PRG. This architecture is designed by using r stage LFSR, a K-input AND gate, and a T flip-flop. Either normal or inverting outputs of LFSR stages are connected to each of K inputs of the AND gate. If we increase the no of K then it will increase the length of test sequence and decrease the fault coverage so in this architecture we used the value of K= 2 or 3. T flip-flop remains in its state and hold the previous value as long as the input of the T flip-flop is set at 1. T flip-flop changes its state in every few clock cycles because in most of the cases output of the AND gate is zero (input of T flip-flop), so in scan chain have same value for most of the cases. In result of this transition probability in CUT will decrease.
3. MODIFIED TEST PATTERN GENERATOR

Basically bit-swapping LFSR in figure 3 is a modified form of conventional LFSR, which generates a pseudo-random pattern at the output of LFSR with reduced transition between 0 and 1 that occur in the output stream of LFSR. Due to the reduction of internal switching activity, Bit-Swapping LFSR is useful for reduction of average power dissipation by CUT. Bit-Swapping LFSR can be implemented either in Test-per-Scan or Test-per-Clock scheme for reduction of power. Internal reduction of switching directly affects the consumed power by CUT.

3.1 General architecture of BS-LFSR

Figure 3 shows implementation of general architecture of Bit Swapping LFSR, which reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transition.

Design of Bit Swapping LFSR is based on some lemmas which are used to describe the transition activity in Bit Swapping LFSR. With the help of these lemmas, we can easily define how the switching and transition of bits take place in pattern generation. These lemmas give the surprisingly good results in order to save power. For the test-per-clock and test-per-scan we have different lemmas. A next section introduces lemmas about Bit Swapping LFSR in test-per-clock and test-per-scan schemes.

There are several techniques to reduce power consumption. There is direct technique, if we used reduced frequency during testing it will reduced power dissipation. In this direct technique there is no requirement of extra hardware [25, 26]. Second direct technique to reduce power consumption is to apply appropriate testing planning by doing portioning of CUT into block.

These direct techniques increase the timing of testing and are not applicable for reduction peak power. In contrast to the other techniques, Bit-Swapping LFSR reduce average and peak power dissipated by CUT.

4. GENERAL OBSERVATION FOR BS-LFSR

Bit-Swapping LFSR is based on some observations depending upon number of transition produced by LFSR at the output. In modified form of normal LFSR we used swapping property between every pair of adjacent cells of normal LFSR to design Bit-Swapping LFSR [21, 22].

General observation for LFSR- For any n-bit maximal-length LFSR that starts with any seed and runs for 2 \(^{n-1} \) clock cycles until it returns to the starting seed value, then the total number of transitions \( T \) that occurs is given by the formula in equation (1):

\[
T_{\text{total}} = n \times 2^{(n-1)} \quad (1)
\]

Observation for swapping Bits in BS-LFSR- If we take an example of any n-bit maximal-length LFSR (n>2) and modified this LFSR for swapping arrangement, we consider one of its outputs (say bit n-1) as the selection line that will swap two neighboring bits elsewhere in the LFSR at specific value of selection line. If we set the value of selection line at 0 for swapping then bit n is odd and bit n =0, bit 1 will be swapped with bit 2, bit 3 with bit 4, ..., bit n-2 with bit n-1. If n is even and bit n =0, then bit n will be swapped with bit 2, bit 3 with bit 4, ..., bit n-3 with bit n-2, in all cases the selection line (n bit) has no effect on swapping operation. If bit n 1, then no swapping is performed. In this case:

1. Modified LFSR will be generated exactly same as normal (unmodified) LFSR. Order of generated test pattern by modified LFSR will be different.

2. Swapping arrangement will save a number of transitions, swapped bits will save number of transition equal to \( T_{\text{saved}} = 2^{(n-2)} \). In contrast, in general observation two bits (un-swapped bits) originally produced \( 2 \times 2^{(n-1)} \) so after swapping the swap bit will therefore save \( T_{\text{saved}} = 2^{(n-2)} (2x2^{(n-1)}=25\%)

5. IMPLEMENTATION OF BIST ARCHITECTURE (WITH BS-LFSR)

In implementation of Test-per-Clock and Test-per-Scan BIST architectures, we replaced conventional LFSR with Bit-Swapping LFSR in figure 1 and figure 2. Implemented architectures show reduction in power consumption by CUT during testing operation.

6. EXPERIMENTAL RESULTS

We used VHDL and xilinx tool for simulation of Test-per-Clock and Test-per-Scan BIST schemes. We used S27 sequential circuit (ISCAS 89 Family) as a Circuit under Test (CUT).
5.1 Test-per-clock BIST power results

5.1.1. with Normal LFSR

5.1.2 with BS-LFSR
5.2 Test-per-Scan BIST power results

5.2.1 with Bit-Swapping LFSR

5.2.2 With Normal LFSR
7. CONCLUSION
Comparisons between the implemented design and conventional architectures show that the implemented design can achieve better results for most tested benchmark circuits. Bit Swapping LFSR reduces transition activity which reduces weighted switching activity and shows good results for power consumption.

8. FUTURE SCOPE
To improve power dissipation in testing mode we can use this technique of pattern generation as called Bit Swapping LFSR with other techniques of transition reduction. In future we can investigate the properties of LFSR to improve the test pattern generation.

9. REFERENCES
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