Design of Efficient Reversible Multiply Accumulate (MAC) Unit

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ABSTRACT
The multiplication and accumulation are the vital operations involved in almost all the Digital Signal Processing applications. Consequently, there is a demand for high speed processors having dedicated hardware to enhance the speed with which these multiplications and accumulations are performed. In the present conventional circuits, the multiply accumulate unit multiplies the two operands, adds the product to the previously accumulated result and stores back the new result in the accumulator all in a single clock cycle. On the other hand, using reversible logic the implementation of digital circuits is gaining popularity with the arrival of quantum computing and reversible logic. In this paper, a novel reversible multiply accumulate unit is proposed. the comparison of various possible implementations of the reversible multiply accumulate unit in terms of gate count, quantum cost, constant inputs and number of garbage outputs is carried out.

Keywords
Reversible Multiply Accumulate Unit, Digital Signal Processors, Reversible Shift Register, Reversible Adder, Reversible Multiplier, Quantum Cost.

1. INTRODUCTION
In irreversible logic, according to Landauer's [1] research, heat dissipation of kTln2 joules takes place on erasing a bit (k is the Boltzmann's constant and T is the absolute temperature of environment). A one to one mapping exists between the input and output vectors in reversible logic and according to Bennett [2], the operations performed in reversible logic will not dissipate kTln2 joules of heat energy. Reversible logic gates constitute reversible logic circuits and their major application can be seen in quantum computing. Each quantum logic gate performs an elementary unitary operation on one, two or more two-state quantum system called qubits. In the design of reversible circuits, fan-out and loops are not permitted.

From the point of view of reversible circuit design, there are three parameters for determining the complexity and performance of circuits: Quantum cost (QC): The number of 1x1 or 2x2 reversible gates which are used in circuit. Constant inputs (CIs): the inputs which are used as control inputs and are connected to logical zero or one. Garbage outputs (GOs): The number of dummy (unused) outputs which are made to appear in order to make the circuit reversible. Gate count: The number of 1x1 or 2x2 reversible gates which are used in the design.

A reversible circuit designer always looks to optimize on these four parameters. All Digital Signal Processing (DSP) algorithms extensively use Multiply-Accumulate (MAC) operation for high performance digital processing system. This operation eases the computation of convolution which is needed in filters, Fourier Transforms, etc. A MAC unit comprises of a multiplier, an adder and an accumulator. The multiplier multiplies the inputs and gives the result to the adder, which adds the multiplier result to the previously accumulated result.

Contribution: In this paper, a novel reversible MAC unit is proposed. The reversible multiplier is implemented by the combination of reversible half adders, full adders and Peres gates. The reversible adder is used as the adder and the reversible accumulator is designed using the reversible shift register. A reversible MAC unit is also built and compared with other possible implementations unit in terms of gate count, quantum cost, constant input and garbage output of the circuit.

Organization: The rest of the paper is organized as follows: Section 2 explains the basics of reversible gates. Section 3 presents the background work. The proposed design of reversible MAC unit is discussed in section 4. Section 5 shows the performance analysis of the proposed MAC unit and section 6 provides the conclusions.

2. BASIC REVERSIBLE GATES
The simplest reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 reversible gates such as Fredkin (F), Toffoli (TG), Peres (PG) and TR gate. The quantum cost of 1*1 reversible gates is zero, and quantum cost of 2*2 reversible gates is one. Any reversible gate can be realized by using 1*1 NOT and 2*2 CNOT reversible gates, such as V, V^+ (V is square root of NOT gate and V^+ is its hermitian) and Feynman gate which is also known as CNOT gate. The V and V^+ quantum gates have the property given in the Equations 1, 2 and 3.

$$V * V = NOT \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V * V^+ = V^+ * V = I \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$V^+ * V^+ = NOT \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

The quantum cost of a design using reversible logic is calculated by counting the number of V, V^+ and CNOT gates.

2.1 NOT Gate

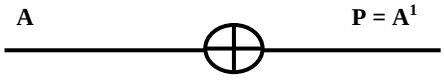

Figure 1. NOT gate

The reversible 1*1 gate is NOT gate with zero quantum cost is as shown in the figure 1.

2.2 Feynman / CNOT Gate

The reversible 2*2 gate with quantum cost of one having mapping input (A, B) to output (P = A, Q = A ⊕ B) is as shown in the figure 2.

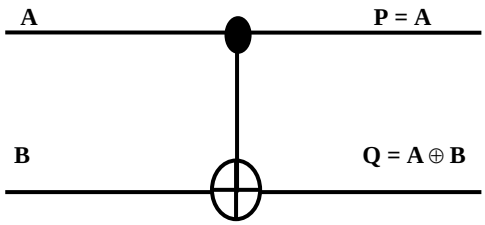

Figure 2. Feynman/CNOT gate [4]

2.3 Toffoli Gate

The 3*3 reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P = A, Q = B, R = A.B ⊕ C) is as shown in the figure 3.

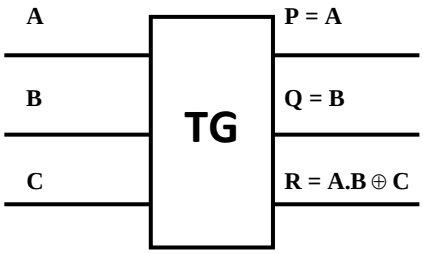

Figure 3. Toffoli gate

Toffoli gate is one of the most popular reversible gates and has quantum cost of five. It requires two V, one V^+ and two CNOT gates. Its quantum implementation is as shown in figure 4.

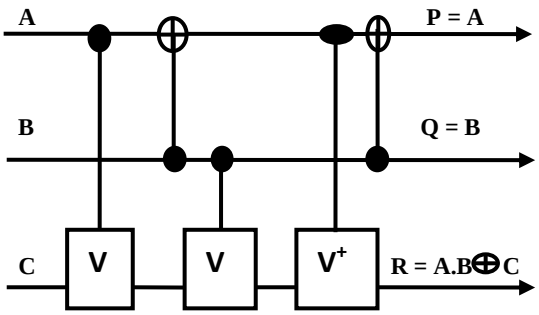

Figure 4. Quantum implementation of Toffoli gate

2.4 Fredkin Gate

Reversible 3*3 gate maps inputs (A, B, C) to outputs (P = A, Q = A^1B + AC, R = AB + A^1C) having quantum cost of five and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with quantum cost of each dotted rectangle is one, one V and two CNOT gates.

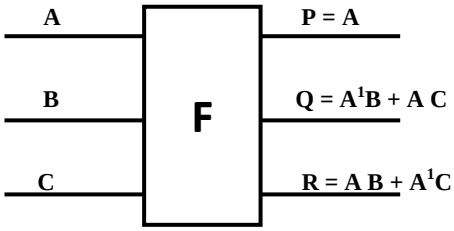

Figure 5. Fredkin gate

Fredkin gate and its quantum implementations are shown in figure 5 and 6 respectively.

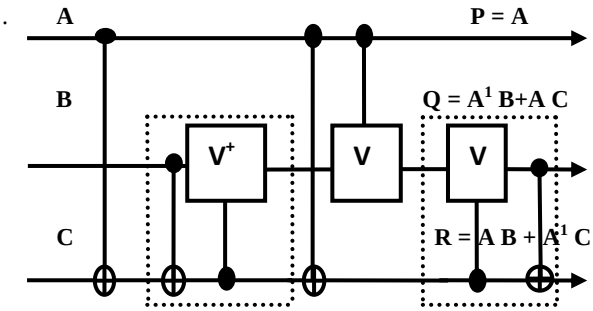

Figure 6. Quantum implementation of Fredkin gate

2.5 Peres Gate

The three inputs and three outputs i.e., 3*3 Reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A ⊕ B, R = (A.B) ⊕ C). Since it requires two V^+, one V and one CNOT gate, it has the quantum cost of four. The Peres gate and its quantum implementation are as shown in the figure 7 and 8 respectively.

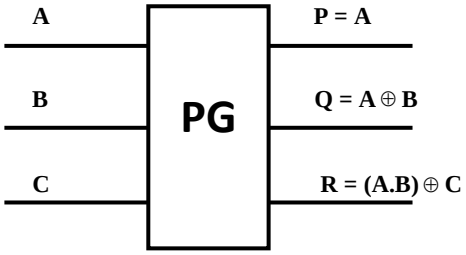

Figure 7. Peres gate

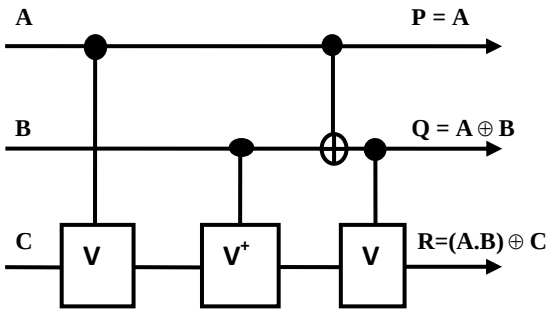

Figure 8. Quantum implementation of Peres gate

2.6 Double Peres Gate

The 4x4 reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to (P = A, Q = A ⊕ B, R = A ⊕ B ⊕ D, S = (A ⊕ B) D ⊕ AB ⊕ C) is as shown in figure 9.

The DPG has a quantum cost of six as it requires three V, one V^+ and two CNOT gates and its implementation is as shown in figure 10.

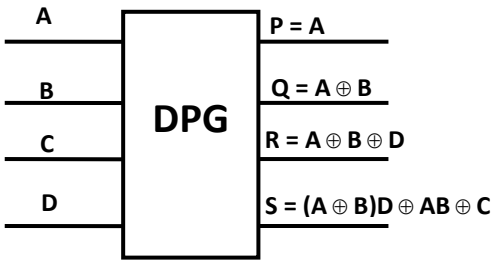

Figure 9. Double Peres gate

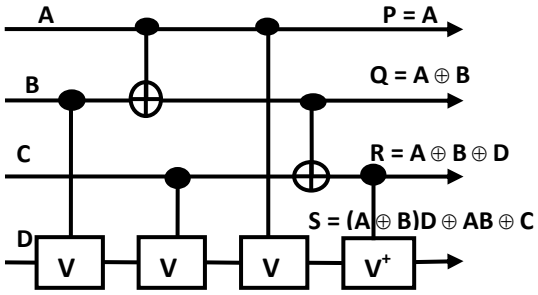

Figure 10. Quantum implementation double Peres gate

The Double Peres Gate (DPG) alone can be used as reversible full adder. The full adder function is realized by using input *C* as control input i.e., *logical low* and D input as C_{in} input of the full adder. With inputs (A, B, 0, C_{in}) mapped to the outputs (P = A, Q = A ⊕ B, R = A ⊕ B ⊕ C_{in}, S = (A ⊕ B)C_{in} ⊕ AB is as shown in figure 11. Here outputs P, Q are garbage outputs and R, S are sum and carry outputs of the full adder respectively.

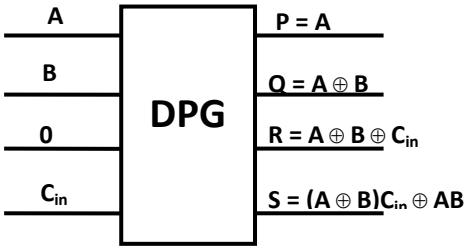

Figure 11. DPG as full adder

2.7 TR Gate

The gate has three inputs and three outputs having inputs (A, B, C) mapped to the outputs (P = A, Q = A ⊕ B, R = (A.B^1) ⊕ C). TR gate is shown in figure 12.

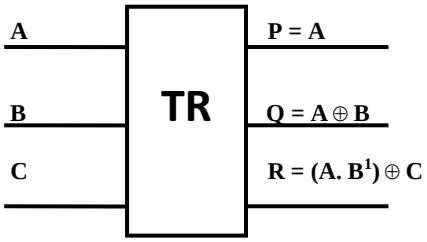

Figure 12. TR gate

The quantum cost of TR gate can be estimated by realizing from two Controlled V gates, one CNOT gate, and one Controlled V^+ gates resulting quantum cost of four and the quantum implementation is shown in figure 13.

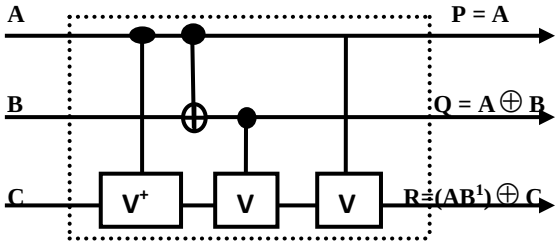

Figure 13. Quantum implementation of TR gate

3. BACKGROUND WORK

Shivakumar Sastry Hari et al., [3] proposed a set of basic sequential elements used to build large reversible sequential circuits. The design is optimized for logic and garbage reduction by a factor of two to six compared to the previous designs. Himanshu Thapliyal and Nagaraju Ranganathan [4] presented novel designs of reversible latches such as D, JK, T and SR. the proposed reversible sequential latches are better in terms of quantum coat, delay and garbage outputs. Min-Lun Chuang and Chun-Yao Wang [5] proposed novel designs of basic reversible sequential elements such as D latch, JK latch and T latch. Using these reversible latches the designs of the flip-flops is also presented. The design is aimed to considerably reduce the no. of gates and the garbage outputs compared to the previous work. J E Rice [6] presented a discussion of reversible logic new reversible implementation for a reversible RS latch is introduced. Four standard types of edge-triggered flip-flops are built exclusively from reversible logic gates. Introducing four reversible flip-flop designs based on the reversible RS-latch implementation. V Rajamohan and V Ranganathan [7] proposed a reversible T flip-flop which is better than the existing designs in the literature. The design of asynchronous and synchronous counter is also presented and the new reversible gate is designed which can be used as copying gate. J E Rice [8] presented a report on the overview of the current state of reversible sequential logic. The report suggests how the proposed structures are incorporated into logic synthesis techniques aimed at producing sequential reversible logic circuits.

Himanshu Thapliyal and M B Srinivas [9] provided the initial threshold to build more complex system having reversible sequential circuits which can execute more complicated operations. The reversible circuits designed here are highly optimized in terms of number of gates and garbage outputs. Majid Haghparast and Mohammad Samadi Gharajeh [10] propose a reversible 4-bit binary counter with parallel load. The reversible gates used are Feynman gate, Peres gate and Fredkin gate and the design has minimum number of garbage outputs and constant inputs. V Mugundhan [11] provided an account of quantum ternary reversible flip-flops and a serial adder implemented using the shift register and its synthesis. The circuit is faster than classical circuits and works at even low power. Nagapavani T et al., [12] presented a new D flip-flop and shift register using D flip-flop which is efficient in terms of garbage output, constant input and number of gates. The designs have the applications to perform serial-to-parallel and parallel-to-serial conversions.

Noor Muhammed Nayeem et al., [13] proposed novel designs of reversible shift registers such as Serial-In Serial-Out (SISO), Serial-In Parallel-Out (SIPO), Parallel-In Serial-Out (PISO), Parallel-In Parallel-Out (PIPO) and Universal shift registers. The design uses minimum number of reversible gates, garbage outputs and quantum cost. Matthew Morrison et al., [14]

presented a novel 4x4 gate and is used for controlling the read/write logic of a SRAM cell. The reversible SRAM cell and 4x4 reversible decoder gate are presented and verified. The dual-port SRAM cell and its implementation in synchronous n-bit reversible dual-port SRAM is presented. Saurabh Kotiyal et al., [15] proposed the design of reversible bidirectional arithmetic and logical barrel shifter. The design uses Fredkin gate in bidirectional arithmetic and logical barrel shifter, which has minimum number of quantum cost, ancilla bits and garbage outputs. The Feynman gate is used to avoid fanout as fanout is not allowed in the reversible logic. Matthew Morrison and Nagarajan Ranganathan [16] proposed novel 4x4 RD gate implemented as a 2-to-4 decoder with low delay and cost. It is used in the implementation of a novel n-to-2n decoder with low cost and delay. The reversible synchronous up-down counter and JK flip-flop is presented. Abu Sadat Md. Sayem and Masashi Ueda [17] presented optimized design of reversible sequential circuits in terms of number of gates, delay and hardware complexity. The design of D-latch and JK latch is presented and is better than the existing designs available in the literature. Himanshu Thapliyal and A P Vinod [18] proposed reversible latches and flip-flops using Fredkin, Feynman and Toffoli gates. Two new reversible gates called Modified Fredkin Gate (MFG) and Modified Toffoli Gate (MTG) are proposed for optimal implementations. The designs are better in terms of number of reversible gates and garbage outputs compared to the previous ones. The transistor implementation of the Feynman, Fredkin, Toffoli, MTG and MFG gates is presented. Noor Muhammed Nayeem et al., [19] presented novel design of sequential hardware having its application in the design of arithmetic logic unit. The design is efficient in terms of number of gates required, garbage outputs and quantum cost. David Y Feinstein and Mitchell A Thornton [20] presented a brief survey of recent developments in reversible sequential circuits and quantum finite state machines based on binary and multi-valued solutions. The reversible implementation of key asynchronous circuits are proposed and demonstrated. Mozammel H A Khan and Marek Perkowski [21] discussed the design of reversible synchronous counters based on positive polarity reed-Muller expressions. Design results shown that the direct design method is more efficient than the replacement method. The method can be also applied to permutative quantum automata that have quantum memories external to the circuit.

Anindita Banerjee and Anirban Pathak [22] provided a protocol for synthesis of sequential reversible circuits from any particular gate library. The reversible circuits for SR latch, D latch, JK latch and T latch are designed from NCT gate library. All the circuits are optimized in terms of lower gate complexities, lower number of garbage bits, lower quantum cost and lower number of feedback loops compared to the previous approaches with the help of local optimized algorithms. A protocol for minimization of quantum cost of reversible circuit is proposed. Himanshu Thapliyal and Nagaraju Ranganathan [23] presented the design of testable reversible latches such as D latch, T latch, JK latch and RS latch based on reversible conservative logic for molecular QCA. The design of QCA layouts and the verification of the latch designs performed using the QCA designer tool are presented. Himanshu Thapliyal and Mark Zwolinski [24] proposed the use of reversible logic for designing the ALU of a cryptosystem. The reversible design of carry propagate adder, four-to-two, five-to-two carry save adders and Montgomery multipliers are presented. Sujata S et al.,[25] introduced the basics of reversible logic gates used for reversible operation and one of the applications as synchronous counter. The design of synchronous and asynchronous counter using sayem gate is proposed and the comparison is made in terms of number of gates, garbage output and power dissipation.

Bahram Dehghan [26] presented asynchronous sequential circuits without hazard effect using reversible logic gates. Illustration to produce AND, OR, NAND, NOR, EXOR and EXNOR outputs in one design using reversible logic is made. The results showed that reversible logic can be used to design these circuits and the parameters like number of gates and garbage outputs are considered. K Prabhakaran and V Vidyadevi [27] proposed a new reversible gate which can be used as copying gate. The reversible T-flip-flop with less number of gates, garbage outputs and power dissipation is proposed and is better than the previous designs. Himanshu Thapliyal et al., [28] proposed the design of two vectors testable sequential circuits based on conservative logic gates. The circuits outperform the classical gates implementation in terms of testability. The design of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops is presented. The new conservative logic gate called multiplexer conservative QCA gate (Mx-cqca) that is not reversible in nature but has similar properties as Fredkin gate is presented.

4. PROPOSED MAC DESIGN

4.1 Multiplier

A reversible 4x4 multiplier circuit has two parts: Partial Product Generation (PPG) circuit and Multi-Operand Addition (MOA) circuit. The details of these two parts are discussed in the following sections:

Partial Product Generation

The basic operation of 4x4 parallel multiplier circuit is depicted in figure 14. It consists of sixteen partial products of the form Xi.Yi, where i vary between 0 and 3.

The PPG circuit using Peres and RAM gates is as shown in figure 4.2. Here sixteen PG gates are used to generate sixteen partial products as shown in figure 4.1. The RAM gate is used as a copying gate, for each Xi input four copies are generated and totally sixteen input signals are copied using four RAM gates as shown in figure 15.

			X3 Y3	X2 Y2	X1 Y1	X0 Y0
			X3.Y0	X2.Y0	X1.Y0	X0.Y0
		X3.Y1	X2.Y1	X1.Y1	X0.Y1	
		X3.Y2	X2.Y2	X1.Y2	X0.Y2	
	X3.Y3	X2.Y3	X1.Y3	X0.Y3		
Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

Figure 14. The basic operation of 4x4 parallel multiplier

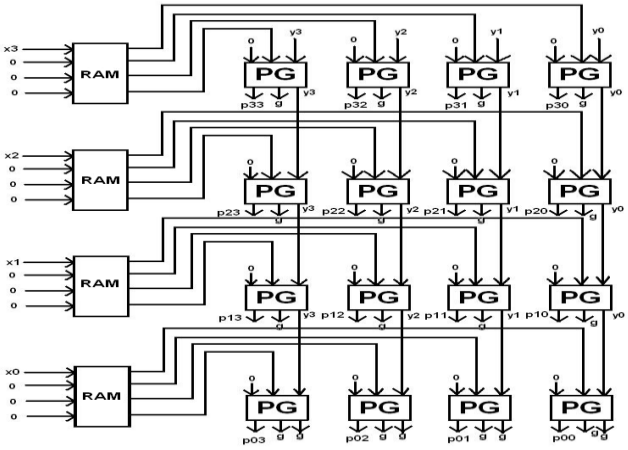

Figure 15. Proposed reversible partial products generation circuit using Peres and RAM gates

Multi-Operand Addition

The addition of the partial products using DPG and PG gates is as shown in figure 16. The basic cells for such a multiplier is full adder using DPG with three inputs and one constant input, two garbage outputs and half adder using PG with two inputs and one constant input, one garbage output.

The proposed reversible multiplier circuit uses eight DPG gates, four PG gates, sixteen PG gates for partial product generation and four RAM gates for fan-out creation. It is possible use FG gate as copying circuit, but it requires twelve FGs instead of four RAM gates and by using RAM gate the hardware complexity and garbage outputs are reduced.

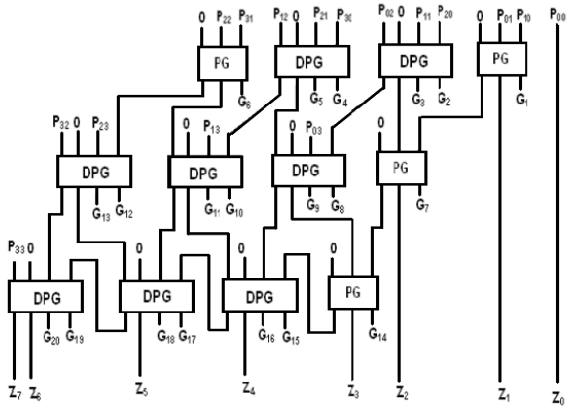

Figure 16. Reversible multi-operand addition circuit

4.2.2 Adder

Half Adder/Subtractor

Reversible half Adder/Subtractor–Design III is implemented with three Reversible gates of which two are FG gates each having Quantum cost of one and a PG gate with Quantum cost four is as shown in the Figure 17. The numbers of Garbage outputs is two i.e., g1 and g2, Garbage inputs are one denoted by logical zero and Quantum Cost is six.

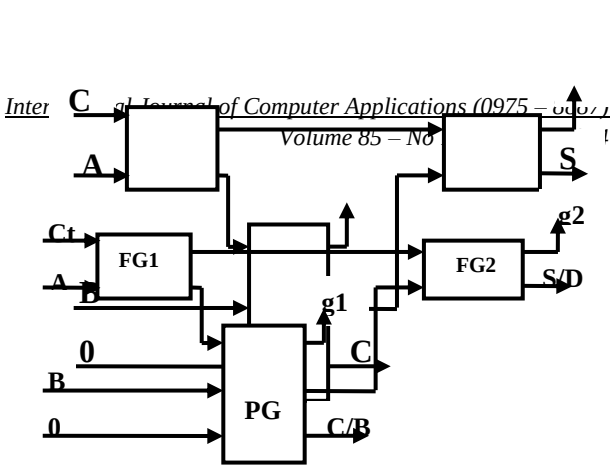

Figure 17. Reversible half adder/subtractor–Design III

Full Adder/Subtractor

The Reversible Full Adder/Subtractor Design III consists of two FG, two PG gates, and their interconnections are shown in the Figure 18. The three inputs are A, B, and Cin, The outputs are S/D and C/B. For Ctrl value zero the circuit performs addition and Subtraction for Ctrl value one. The numbers of Garbage inputs are 1 represented by logical zero. The Garbage outputs are 3 represented by g1 to g3.

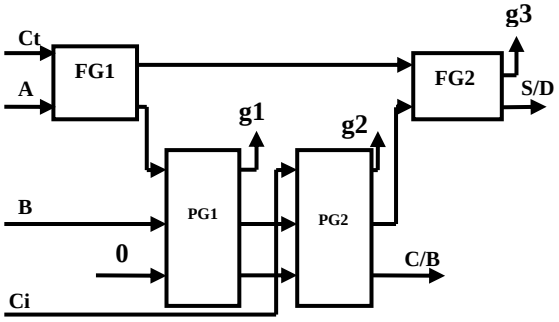

Figure 18. Reversible full adder/subtractor–Design III

The Quantum Cost for the design is 10. A Quantum Cost advantage of 11 is obtained when compared to Adder/Subtractor Design I and of 4 when compared to Adder/Subtractor Design II. Quantum Cost advantage is due to the realization of Arithmetic blocks using two PG gates as against two F and one TR gate for Design I and two TR gates for Design II.

Eight-bit Parallel Binary Adder/Subtractor

The Half and Full Adder/Subtractor Design I, Design II and Design III are used to construct Reversible eight-bit Parallel Binary Adder/Subtractor is shown in the Figure 19. The ctrl input is used to differentiate eight-bit addition and subtraction functions. The two eight-bit binary numbers are A0 to A7 and B0 to B7. Carry/Borrow is obtained after Addition/Subtraction is represented by C_B1 to C_B7. The outputs Sum/Difference and Carry are shown as S_D0 to S_D7 and C_B8 respectively. The implementation requires seven Full Adder/Subtractor units and one half Adder/Subtractor units in which first stage is half Adder/Subtractor.

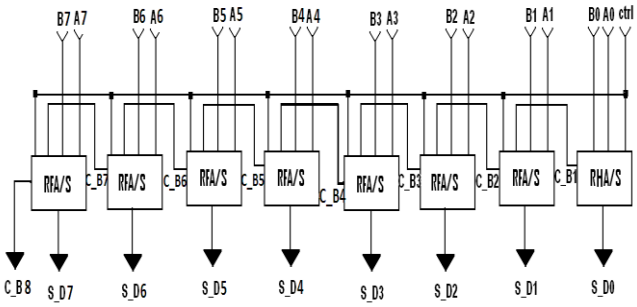

Figure 19. Reversible Eight-bit parallel Binary Full Adder/Subtractor

4.2.3 Accumulator

Accumulator is one of the most extensively used functional devices in digital systems. A register consists of a group of flip-flops connected together so that the information bits can be stored within a digital system so that they can be used later during computing process. Shift register is a register in which information can be shifted bit wise depending on the clock signal. This section proposes Parallel-In-Parallel-Out (PIPO) shift register. The designs are proposed using the basic reversible gates considering the previous designs, we are aiming on reducing the quantum cost of each designs.

Reversible D-Latch

The D-latch can be realized using Fredkin gate as shown in figure 20. The quantum cost of the design shown is five; number of garbage outputs is one. The propagation delay of the design is 5Δ.

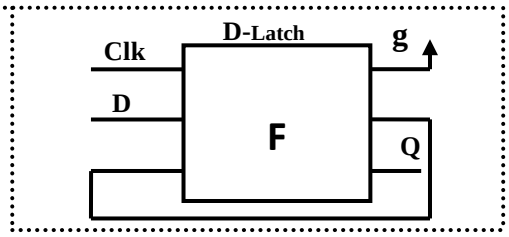

Figure 20. Reversible D-Latch

Reversible D Flip-Flop

A flip-flop is a bi-stable electronic circuit that has two stable states and one-bit memory device. The characteristic equation of D flip-flop is $Q^+ = D.\ Clk + Q.\ Clk^1$ which can be mapped onto the Fredkin gates as shown in figure 21.

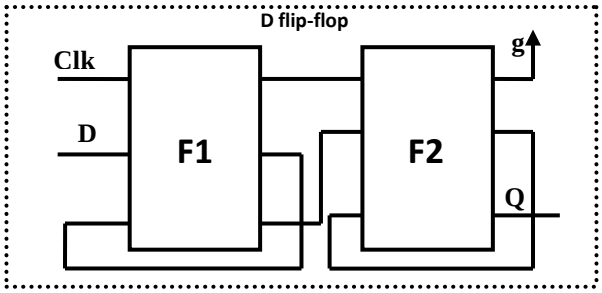

Figure 21. Reversible D Flip-Flop

The Feynman gate produces the toggled output of the input and the second Feynman again toggles the output of the first Feynman, thus we obtain the input at the output with a delay. The constant input '1' helps the second Feynman gate to toggle the input. The output 'g' represents the garbage output and Q is the actual output.

Reversible eight-bit PIPO Shift Register

In this shift register, the inputs are fed simultaneously into the flip-flops and we get the output when we apply clock pulse. Here eight D flip-flops are used for the design. The PIPO shift register combines the functions of the Parallel-In-Serial-Out (PISO) and Serial-In-Parallel-Out (SIPO) shift registers.

When there is a clock signal, the inputs D_0, $D_1 \ldots D_7$ are loaded parallel into the register coincident. The outputs Q_0, $Q_1 \ldots Q_7$ are available in parallel at the Q output of the flip-flops. The quantum cost of D flip-flop is ten, therefore the quantum cost of eight-bit shift register if eighty without fan-out creation and is eighty seven with fan-out creation.

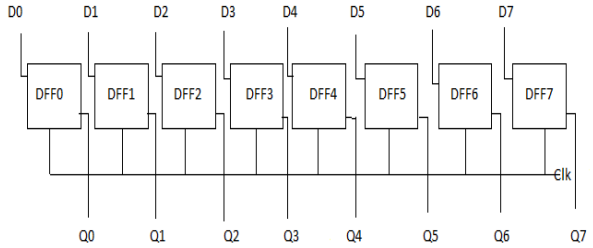

Figure 22. Reversible 8-bit PIPO Shift Register

4.2.4 Multiply Accumulate (MAC) Unit

This section describes four-bit reversible Multiply Accumulate Unit shown in figure 23. A MAC unit is used to perform the multiplication and accumulator operations together to avoid unnecessary overhead on the processor in terms of processing time and the on-chip memory requirements. This is extensively used in Digital Signal Processing algorithms for high performance digital processing system. The proposed reversible MAC unit comprises of a four-bit reversible Multiplier, eight-bit reversible Adder and eight-bit reversible Accumulator register. The Multiplier multiplies the inputs and gives the result to the adder, which adds the multiplier result to the previously accumulated result. The reversible Accumulator is designed using the reversible eight-bit register.

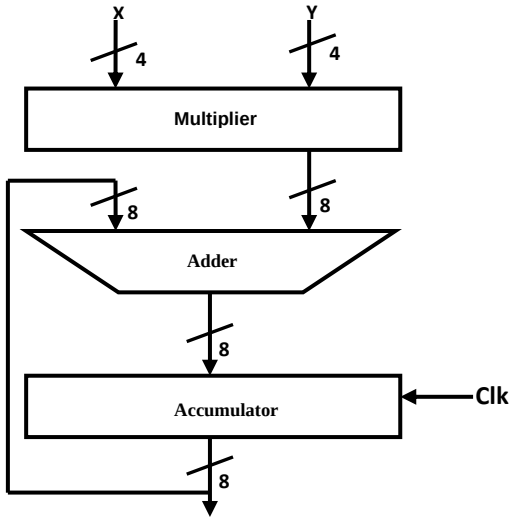

Figure 23. Reversible 4-bit multiply-accumulate unit

The four-bit inputs X and Y are applied to the multiplier unit which results in eight-bit product. The product is applied to eight-bit adder unit which adds the previous result stored in accumulator as well as the present out of the multiplier. Again the result of the adder is stored back into the accumulator and this process will repeat till the last bits.

In digital signal processing, Discrete Fourier Transform (DFT) computation is most widely used where number of multiplications and additions should be performed. Most of the power consumption occurs during data manipulation. Therefore to minimize the power consumption DFT computation can be implemented by reversible MAC unit. The conventional multiply accumulate unit consists of multiplier and an accumulator register that contains the sum of the previous consecutive products. The function of the multiply accumulate unit is given by the following expression.

$$F = \Sigma X_i . Y_i \text{ ---------- Eq 4.1}$$

5. RESULTS AND DISCUSSIONS

5.1 Simulation Results

Reversible Multiplier

Reversible multiplier is coded in VHDL and simulated using Modelsim simulator. Reversible gates such as PG, DPG and RAM gates are coded in behavioral style of modeling. The PPG generation circuit is coded in structural style of modeling and multi-operand addition circuit is constructed by using the reversible gates as the components for the structural model and the functionality is verified. The simulation result is given in figure 24. Here, a and b are four-bit inputs and z is the eight-bit multiplier output.

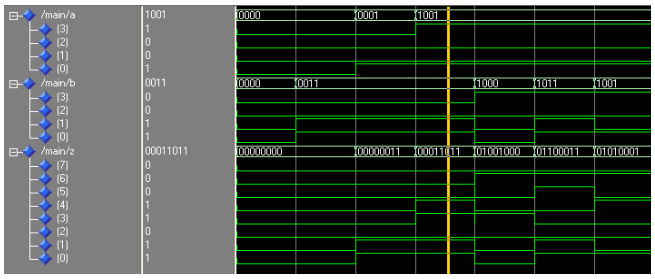

Figure 24. Simulation waveform of reversible multiplier

The wave form shown in figure 24 is an example for reversible multiplier. In this, a and b are four-bit inputs and z is eight-bit product output. For a = "1001" and b = "0011" inputs the circuit performs multiplication function results in z = "00011011" output.

Reversible Adder

Reversible adder/subtractor designs types are coded in VHDL and simulated using Modelsim simulator. Reversible gates such as FG and PG gates are coded in behavioral style of modeling. Half and full adder/subtractors are coded in structural style of modeling. Half and full adder/subtractors are constructed by using the reversible gates as the components for the structural model and the functionality is verified. Results of simulation are given in figure 25 to 27. In this design the control bit set to logic one indicates subtraction function and control bit set to logic zero indicates addition function. The output bits s_d and c_b shows the corresponding logic levels for the input bits a, b and c logic levels. The implementation uses seven full adder/subtractor units and one half adder/subtractor unit in which first stage is half adder/subtractor.

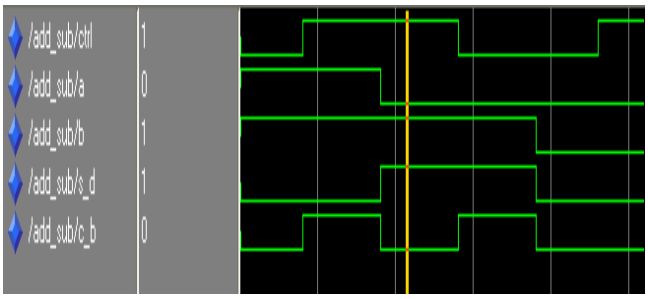

Figure 25. Simulation result of reversible half adder/subtractor

The wave form shown in figure 25 is an example for half adder/subtractor and is same for all the three design types. In this a, b and Ctrl are input bits and s_d and c_b are sum/difference and carry/borrow outputs respectively. For a = '0', b = '1' and Ctrl = '1' inputs the circuit performs addition function results in s_d ='1' and c_b = '0' outputs.

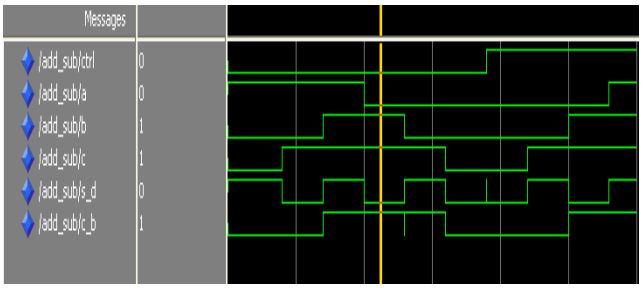

Figure 26. Simulation result of reversible full adder/subtractor

The wave form shown in figure 26 is an example for full adder/subtractor and is same for all the three design types. In this a, b, c and Ctrl are input bits and s_d and c_b are sum/difference and carry/borrow outputs respectively. For a = '0', b = '1', c = '1' and Ctrl = '0' inputs the circuit performs subtraction function results in s_d ='0' and c_b = '1' outputs.

The wave form shown in figure 27 is an example for eight-bit parallel adder/subtractor and is same for all the three design types. In this a and b are eight-bit and Ctrl one-bit inputs and s_d and c_b8 are eight-bit sum/difference and one-bit carry/borrow outputs respectively. For a = "10101110", b = "01010111", c = '1' and Ctrl = '1' inputs the circuit performs addition function results in s_d = "00000101" and c_b8 = '1' outputs.

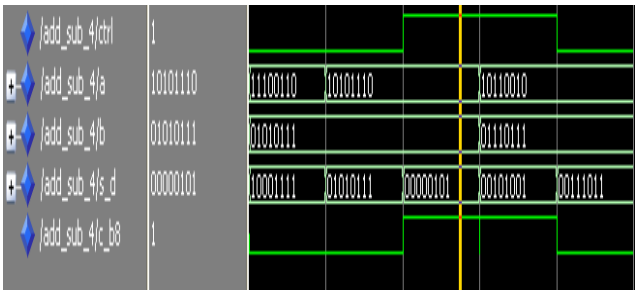

Figure 27. Simulation waveform of reversible eight-bit parallel binary adder/subtractor

Reversible Accumulator

Reversible D flip-flop and shift register designs types are coded in VHDL and simulated using Modelsim simulator. Reversible gates such as FG and F gates are coded in behavioral style of modeling. The simulation results of D flip-flop and Accumulator are shown in the following figures. In the D flip-flop, whenever Clk signal is high the input D appears at the output Q and is shown in figure 28.

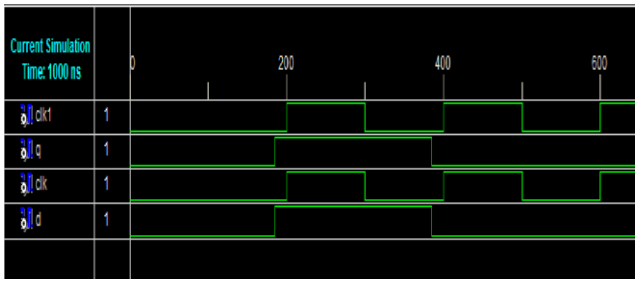

Figure 28. Simulation result of reversible D Flip-flop

In Parallel-In-Parallel-Out shift register the inputs are loaded parallel to all the flip-flops when clock signal is high and the same will appear at the output of each flip-flops as shown in the figure 29.

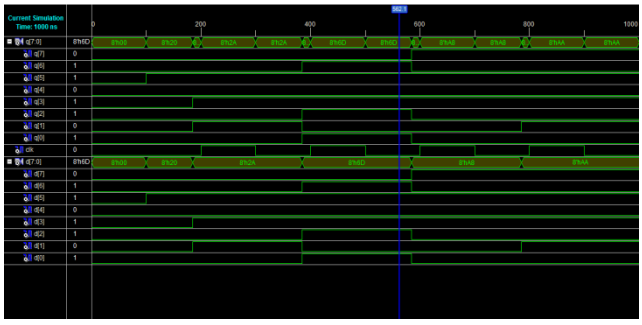

Figure 29. Simulation result of reversible eight-bit Shift register

5.2 Performance Comparison

Reversible Multiplier

The comparison of reversible 4-bit multiplier design is shown in table 1. The parameters such as the number of gates, number of garbage inputs/outputs and quantum cost of the existing and proposed design are summarized. It is observed that the proposed design has better performance compared to the existing ones. The garbage outputs are fifty two in case of [34, 35], whereas forty in the case of the proposed design. The quantum cost in case of [35] is one hundred fifty two and is one hundred forty in case of proposed design. The comparison of the key parameters is graphically illustrated in figure 30.

Table 1. Comparison of existing and proposed reversible 4-bit multiplier unit

4x4 Multiplier	Quantum Cost	No of gates	Garbage outputs	Constant inputs
Shaik et al., [34]	---	28	52	28
Swaraj et al., [35]	152	---	52	-----
Rangaraju et al., [36]	140	32	40	40

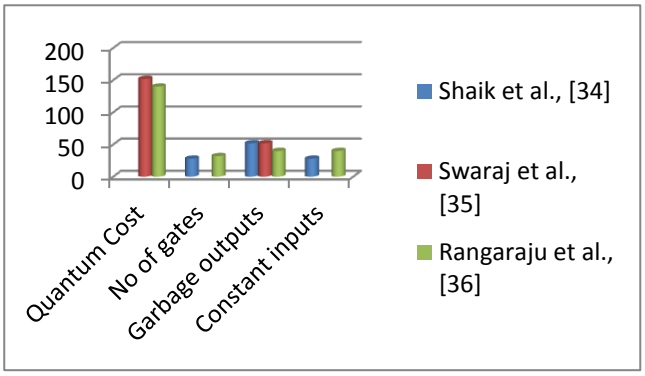

Figure 30. Comparison of the proposed and previous reversible multiplier designs

Reversible Adder

Half/Full Adder/Subtractor

The comparison of reversible full adder/subtractor is shown in table 2(a). It is observed that design-III has better performance compared to design-II and design-I. The number of reversible gates required for design-III is only four as compared to eight and four in the cases of design-I and II respectively. The garbage outputs are five in the case of design-I, whereas three in the case of design-II and design-III. The constant inputs are three in the case of design-I and one in case of design-II and design-III. The quantum cost of design-III, design-II and design-I is twenty one, fourteen and ten respectively. The percentage improvements of full adder/subtractor design-III compared to design-I and design-II are shown in the table 2(b).

Table 2 (a). Comparison of reversible full adder/subtractor designs [37]

Full Adder/ Subtractor	Reversible Gates	GO	CI	QC
Add/Sub D-I	08	05	03	21
Add/Sub D-II	04	03	01	14
Add/Sub D-III	04	03	01	10

Table 2 (b). Percentage improvement of reversible full adder/subtractor

Full Adder/Subtractor	Reversible Gates	Garbage outputs	Garbage inputs	Quantum Cost
% Improvement of D-II over D-I	50	40	66.66	33.33
% Improvement of D-III over D-I	50	40	66.66	52.38
% Improvement of D-III over D-II	-	-	-	28.57

The comparison of the key parameters like number of reversible gates, garbage outputs, garbage inputs and quantum cost of the proposed adder/subtractor designs is graphically illustrated in figure 31. From the graph it is clear that the design-III is better compared to other designs with respect to the key parameters.

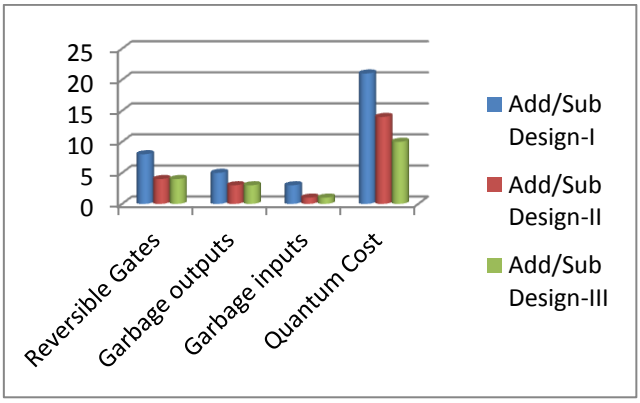

Figure 31. Comparison of the proposed different adder/subtractor designs [37]

Eight-bit Parallel Binary Adder/Subtractor

The number of gates, garbage inputs/outputs and quantum cost for reversible eight-bit parallel binary adder/subtractor design-I, design-II and design-III are summarized as shown in the table 3(a).

It is clear that design-III has better performance compared to design-II and design-I. The number of reversible gates required for design-III is thirty one as compared to sixty and thirty one in the cases of design-I and-II respectively, which is an improvement of 48.33% compared to design-I. The garbage outputs are thirty eight in the case of design I, whereas twenty three in the case of design-II and design-III yields an improvement of 39.47% in design-III compared to design-I. The garbage inputs are twenty three in the case of design-I and eight in case of design-II and design-III, resulting 65.21% improvement in design-III compared to design-I. Quantum cost of design-III, design-II and design-I is seventy six, one hundred six and one hundred and fifty nine respectively, hence an improvement of design-III over design-II and design-I are 28.30% and 52.20% respectively. The percentage improvements of eight-bit parallel binary adder/subtractor design-III compared to design-I and design-II are shown in the table 3(b).

Table 3 (a). Comparison of reversible eight-bit parallel binary adder/subtractor designs [37]

8-bit parallel binary Adder/Subtractor	Reversible Gates	GO	CI	QC
Add/Sub Design-I	60	38	23	159
Add/Sub Design-II	31	23	08	106
Add/Sub Design-III	31	23	08	76

The comparison of the key parameters like number of reversible gates, garbage outputs, garbage inputs and quantum cost of the proposed eight-bit parallel binary adder/subtractor designs is graphically illustrated in figure 32. From the graph it is clear that the design-III is better compared to other designs with respect to the key parameters.

The previous reversible binary subtractor based on reversible gate [38] to implement full subtraction requires quantum cost of twelve, garbage inputs of one and garbage outputs of two. The proposed reversible eight-bit parallel binary adder/subtractor design-III is better compared to the existing design in terms of quantum cost, garbage inputs and garbage outputs and also in our design the full subtraction and addition function is implemented together as compared to only subtractor in the existing design. Hence we claim that design III is better in terms of performance compared to the previous designs.

Table 3 (b). Percentage improvement of eight-bit parallel binary adder/subtractor design

Eight-bit parallel binary Adder/Subtractor	No of gates	GO	CI	QC
% Improvement of D-II over D-I	48.33	39.47	65.21	33.33
% Improvement of D-III over D-I	48.33	39.47	65.21	52.20
% Improvement of D-III over D-II	---	---	---	28.30

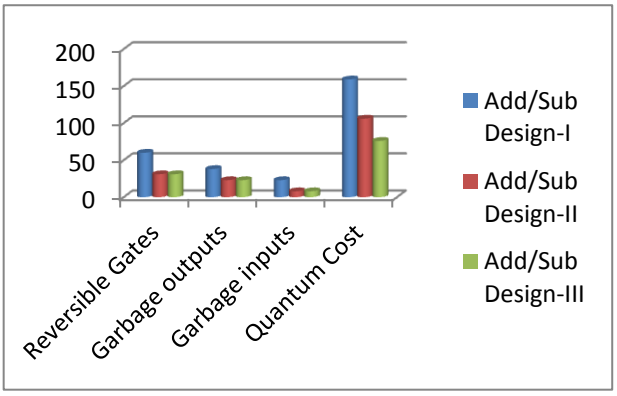

Figure 32. Comparison of the proposed eight-bit parallel adder/subtractor designs [37]

Reversible Accumulator

D-Latch

The comparison of reversible D latch is shown in table 4. The parameters such as the number of gates, number of garbage inputs/outputs and quantum cost of the existing and proposed design are summarized.

It is observed that the proposed design has better performance compared to the existing ones. The number of reversible gates required for [29] and [30] are two and for [31] are one, whereas the proposed design requires only one reversible gate. The garbage outputs are two in the case of [29, 30, and 31], whereas one in the case of the proposed design. The quantum cost in case of [29, 31] is six, five in case of [30] and five in case of proposed design.

Table 4. Comparison of existing and proposed reversible D-Latch designs

D-Latch	QC	No of gates	GO	CI
Himanshu and Ranganathan	6	2	2	1
Krishnaveni and Geetha [30]	5	2	2	1
Prashant and Sujata [31]	6	1	2	1
Proposed design	5	1	1	0

The comparison of the key parameters like number of reversible gates, garbage outputs, garbage inputs and quantum cost of the proposed D-latch design is graphically illustrated in figure 33. From the graph it is clear that the proposed design is better compared to other designs with respect to the key parameters.

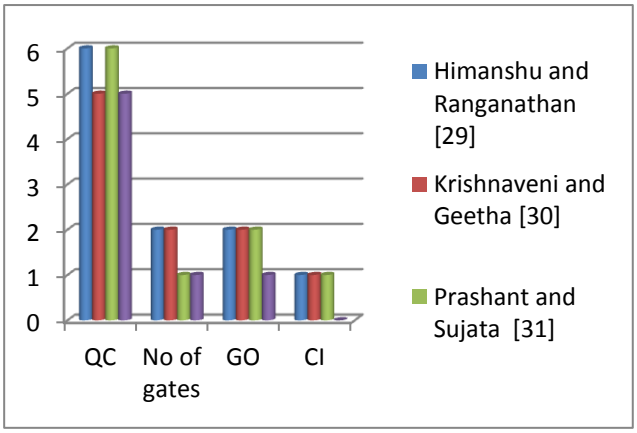

Figure 33. Comparison of existing and proposed reversible D-Latch designs

D-Flip-Flop

The comparison of reversible D flip-flop is shown in table 5. The parameters such as the number of gates, number of garbage inputs/outputs and quantum cost of the existing and proposed design are summarized.

Table 5. Comparison of existing and proposed reversible D Flip-Flop designs

D Flip-Flop	QC	No of gates	GO	CI
Himanshu and Ranganathan [29]	12	4	3	2
Prashant and Sujata [31]	-	3	4	4
Belayet et al., [32]	-	3	2	3
Bhagyalakshmi and Venkatesha [33]	10	4	2	2
Proposed design	10	2	2	0

It is observed that the proposed design has better performance compared to the existing ones. The number of reversible gates required for [29, 33] are four and for [31, 32] are three, whereas the proposed design requires only two reversible gates. The garbage outputs are three in the case of [29], four in [31] and two in case of [32, 33], whereas two in the case of the proposed design. The quantum cost in case of [29] is twelve, ten in case of [33] and ten in case of proposed design.

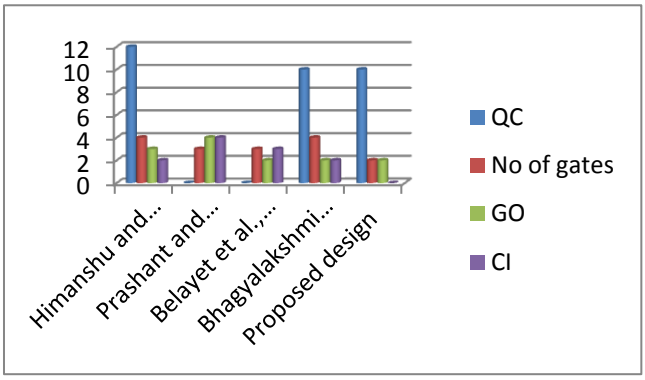

Figure 34. Comparison of existing and proposed reversible D Flip-Flop designs

The comparison of the key parameters like number of reversible gates, garbage outputs, garbage inputs and quantum cost of the proposed D flip-flop design is graphically illustrated in figure 34. From the graph it is clear that the proposed design is better compared to other designs with respect to the key parameters.

Reversible MAC Unit

The comparison of reversible 4-bit multiply accumulate unit design is shown in table 6. The parameters such as the number of gates, number of garbage inputs/outputs and quantum cost of the existing and proposed design are summarized. It is observed that the proposed design has better performance compared to the existing ones. The garbage outputs are ninety one in case of [35], whereas seventy one in the case of the proposed design. The quantum cost in case of [35] is three hundred and two and is three hundred and three in case of proposed design.

Table 6. Comparison of existing and proposed reversible 4-bit multiply accumulate unit

4-bit MAC Unit	QC	No of gates	GO	CI
Swaraj et al., [35]	302	---	91	---
Proposed design	303	86	71	55

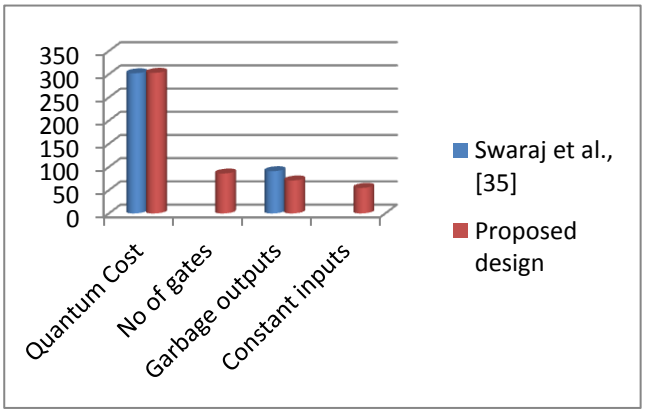

Figure 35. Comparison of existing and proposed reversible 4-bit multiply accumulate unit

The comparison of the key parameters like garbage outputs and quantum cost of the proposed four-bit multiply accumulate unit design is graphically illustrated in figure 35. From the graph it is clear that the proposed design is better compared to other designs.

6. CONCLUSIONS

In this paper design of reversible shift register and multiply-accumulate units are presented. The design is based on the useful properties of standard reversible gates suitable for multiplication, addition and accumulation. The 4-bit reversible multiply-accumulate unit is designed using 4-bit reversible multiplier circuit, 8-bit reversible adder/subtractor and 8-bit accumulator register. The key performance parameters like garbage outputs, number of reversible gates used, quantum cost and constant inputs are computed and analyzed for 4-bit multiply accumulate unit. It is observed that the performance parameter values are less in the proposed design compared to the existing approaches.

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