STG-NoC: A Tool for Generating Energy Optimized Custom Built NoC Topology

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ABSTRACT
Network on Chip (NoC) has emerged as a viable solution to the complex communication requirements of constantly evolving System on Chip (SoC). The communication centric architecture of NoC can be optimized across a variety of parameters as per the design requirements. With the development of customized application the inclination has shifted from regular architectures to irregular topology which leaves researchers with larger spectrum of optimization parameters. Many heuristic methods have been explored as the optimization problems encountered are NP-hard. This paper presents a customized topology generator STG-NoC which implements a heuristic technique based on simulated annealing for achieving the objective of energy optimization.

General Terms
Network-on-Chip (NoC) Simulated Annealing (SA).

Keywords
Customized Network-on-Chip (NoC), Energy optimization, Simulated Annealing (SA), STG-NoC (Simulated Annealing based Topology Generator for Network on Chip).

1. INTRODUCTION
Evolving standards and customized applications have resulted in a rapid increase in the number of cores on SoCs [1].

A viable solution to address the communication problems of such SoCs is presented by NoCs [2-4] where cores are interconnected using on chip micro networks. This feature of NoC helps in better modularity and design predictability in comparison to traditional systems based on bus architecture.

The design challenges [5] that need to be addressed for NoC includes application specific communication patterns, high predictability, energy efficiency constraints, real time requirements and VLSI issues viz. structure and wiring complexity.

Standard topologies like meshes, tori, fat tree or k-ary n-cubes etc which are characterized by their simplicity were favored by early researchers [6-7]. However the regular structures are best suited for general purpose applications. The heterogeneous architecture of most SoCs renders these regular structures inadequate in terms of wiring complexity and energy overhead. Customized NoCs are apt for these complex and irregular architecture. The efficiency of the selected routing function is highly dependent on underlying topology. Therefore a topology generated according the requirement of application specific communication pattern is more effective [8-9]. More over the optimization in terms of area, energy and bandwidth can be achieved using application specific communication structure.

Various phases involved in NoC synthesis [5] are topology task identification, core to tile mapping, floorplanning and optimization. Different optimization approaches follow different order of the given process and can be broadly classified [10] as area optimized NoC synthesis and interconnection optimized NoC synthesis.

In this paper a customized topology generator tool STG-NoC is proposed. The energy optimized topology generation is based on a heuristic technique adapted from Simulated Annealing process. The methodology used by the tool falls under the area optimized NoC synthesis [10] category.

Simulated annealing [11-12] is a meta-heuristic optimization technique derived from annealing process where a metal at a high temperature cools to attain a minimum crystalline structure. The cooling process is marked by movement in neighborhood allowing significant and random changes during high temperatures and as temperature lowers the movement is slow accepting only those changes which minimize objective function.

The paper is organized as follows. The next section, Section II provides a brief overview of communication model required for customized topology generation. Section III explains in detail the methodology incorporated by STG-NoC. Experimental results are given in Section IV and the paper concludes with Section V.

2. COMMUNICATION MODEL
This section describes the communication model. NoC energy model and architecture and the applicable routing function for the customized NoC.

2.1 Communication Model
For an abstract level model of the behavior of multi-core SoC applications which are inherently complex use of Task Graphs [7], [13] is favorable. The model assumes a point to point connection of cores and the communication is unidirectional. Each task is mapped to a set of cores represented by . Figure 1 shows the generic communication model.
The routing functions considered by STG-NoC for customized NoC in this paper are up*/down* and Left-Right routing functions [15-16]. These functions are distributed in nature. The implementation is achieved through look-up table and the routing tables are derived using breadth-first search (BFS) on the topology graph for customized NoC. These routing functions are based on turn restriction and thus achieve deadlock avoidance.

3. TOPOLOGY GENERATION USING STG-NoC

This section describes the process involved in topology generation using STG-NoC. The description is followed by figure 2 which gives a brief overview of the process.

3.1 STG-NoC design methodology

The method adopted by the tool to generate energy efficient customized topology takes application communication characteristic, defined by Task Graph and Core Graph, as input. The floorplans to be evaluated are obtained using B*-Trees [14] which is a non-slicing floor planner.

Link length is calculated according to Manhattan Distance and a physical constraint of maximum permitted channel length ($e_{\text{max}}$) is maintained. In addition nodes of the generated topology cannot exceed maximum permitted node degree ($n_{\text{max}}$). This prevents slowing down of routers due to delays caused by heavy traffic.

Topology generation is initiated by determining the shortest path using Dijkstra’s algorithm followed by construction of the minimum spanning tree using Prim’s algorithm. Due to the constraint of $e_{\text{max}}$ and $n_{\text{max}}$, the order in which traffic patterns (as observed from Core Graph) are considered determine the communication energy requirement of the topology. To identify this appropriate order a heuristic technique based on simulated annealing described in the next sub-section is utilized by STG-NoC.

The routing tables of the nodes/routers are updated with identified shortest paths during the process. Routing decision based on the selected routing function (up-down, Left-Right etc.) gives highest priority to shortest path. A modified Dijkstra’s algorithm is used to find routes from each node in the shortest path to the corresponding destination according to the up*/down* (Left Right) rule. Thus a customized topology which has optimized energy requirements is generated along with required routing tables.

3.2 Annealing Schedule

A heuristic technique based on simulated annealing is used to identify the most appropriate order of the traffic pattern which will lead to optimized energy requirement of the generated customized topology.

The optimization schedule commences with a high initial temperature. The initial solution (currentSolution) is generated with a random order of traffic patterns obtained from Core graph. The objective function is calculated in terms of energy as given by equation (1). The variable bestSolution tracks the best solutions obtained during the schedule.

A search for an optimum energy solution is made in neighborhood (newSolution) of the initial solution. This is achieved by rearrangement of traffic patterns of the currentSolution. The extent of rearrangement is determined by the corresponding temperature and the size of the topology being considered. This allows for significant changes during the initial phase of the schedule. The acceptance of the solution is determined by a probability function $exp(diff/T)$ which is temperature dependent. This ensures that the search does not get trapped in local minima as the solution is accepted even if it drifts away from optimization target during early phases of the process.

For each temperature the process is repeated iteratively and the iteration count depends on the factor ‘$\alpha$size’ which
represents the number of corresponding traffic patterns. In addition a stopping criterion determines that the process runs for specific iterations and marks the end of schedule if no further improvement is observed in the results even if the final temperature is not reached. This improves time efficiency of the algorithm.

<table>
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<tr>
<th>Requirement</th>
<th>Input: Task graph, Core graph</th>
<th>Output: Customized topology</th>
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<td>E: Energy (objective) function</td>
<td>$T_0$: Initial temperature</td>
<td>$cYear$: Temperature cooling rate</td>
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Adaptive simulated annealing schedule:
1. Generate an initial solution currentSolution
2. Set temperature $T$ to an initial value $T_0 > 0$
3. Set the final temperature $T_f$
4. Set bestSolution to currentSolution
5. Set the iteration count $icnt$ corresponding to aSize
6. while $T > T_f$ or stopping criteria not true do
7. for $i = 1$ to $icnt$ do
   a. Generate a neighbour solution newSolution
   b. diff = $E(newSolution) - E(currentSolution)$
   c. if diff < 0 then
      d. currentSolution = newSolution
   e. else
      f. Generate a random number $x$ uniformly in the range (0,1)
     g. if $x < \exp(\text{diff}/T)$ then
      h. currentSolution = newSolution
    i. end if
   j. end if
8. end for
9. $T = T * cYear$
10. currentSolution = newSolution
11. check for stopping criteria
12. end while
13. return bestSolution

Figure 2: Overview of the heuristic used by STG-NoC

Figure 3 represent the optimization achieved with respect to communication energy using the heuristic technique as described above for the topology generation process of STG-NoC. The values were observed for bestSolution variable. The observations are from a sample with 81 tile size and 89 communication patterns. Similar optimization trends have been observed for other tile sizes and configurations as well. As can be seen the initially drastic changes are observed which stabilize as the schedule progresses.

![Energy Optimization](image)

4. EXPERIMENTAL RESULTS

The core graphs samples were generated using TGFF [13]. The experiments were conducted for about 100 samples evenly distributed across topologies ranging from size 16(4x4) to 81(9x9). Various communication patterns with diverse bandwidth requirement were considered for the evaluation.

For customized NoC generated using STG-NoC the maximum permitted channel length ($c_{max}$) was assumed 1.5 times the core length. The maximum number of ports ($n_{max}$) was restricted to 4. $E_{\text{bit}}$ calculated for 0.18 micro meter technology was $0.00007$ pico-joules per mili-meter length of wire. $E_{\text{bit}}$ was estimated to 0.52 pico-joules for 2-virtual channel router and 32 bit flit with help of Orion power simulator [17].

The simulator IrNIRGAM [18] which is an extended version of NIRGAM [19] was utilized for experimental evaluation. It is a cycle accurate, SystemC based simulator which supports wormhole switching. It has provision for architecture based on virtual channel and source and table based routing. IrNIRGAM supports irregular and customized topologies as well as escape path routing for deadlock avoidance applied to the customized topologies obtained from the tool STG-NoC.

The simulator also allows evaluation of regular topology configuration like mesh, tori etc and routing function viz. XY and OE. It was run for 10000 clock cycles uniformly.

For comparative evaluation the tile size and task to core/tile mapping of each sample under test was applied to regular 2D-mesh structure with deterministic XY routing function and adaptive OE routing function and comparison was done with respect to average dynamic energy consumption and latency.

The subsections below give the details of comparative results.

4.1 Energy consumption

Figure 4 shows the comparison of average of dynamic communication energy in pico-joules observed across various tile configurations for customized topologies generated using STG-NoC and the regular structured topologies. As can be observed from the graph the energy required by the topology generated by STG-NoC is much less than the regular configuration topologies. When compared with deterministic routing function XY the difference estimates to 30%, while a
difference of around 50% is observed in comparison with adaptive routing function OE. The difference becomes more significant with increase in tile size.

Similarly the average communication energy consumption of STG-NoC generated topologies (42.5 pico-joules) shows an improvement of 4% and 27% respectively over regular topology routing functions XY(46.7 pico-joules) and OE(69.6 pico-joules).

5. CONCLUSION

This tool STG-NoC presented in this paper generates customized topology while attempting to optimize communication energy requirements of the generated topology. When the results obtained from the tool are compared with those of 2D mesh topology with respective routing functions the tool is observed to succeed in its optimization objective. The improvements are obtained in terms of energy and latency as well. Similar success is observed with the bench mark application also. The tool can be upgraded to incorporate enhanced architecture like 3D NoC and other optimization objectives like bandwidth requirement can be explored as well.

6. REFERENCES


