Analysis of Conventional CMOS and FinFET based 6-T XOR-XNOR Circuit at 45nm Technology

Neha Yadav
Research Scholar
ITM University, Gwalior, India

Saurabh Khandelwal
Research Scholar
ITM University, Gwalior, India

Shyam Akashe
AP, ECED, ITM University,
Gwalior, India

ABSTRACT
As technology has scaled down, the implications of leakage current and power analysis for memory design have increased. To minimize the short channel effect Double-gate FinFET can be used in place of conventional MOSFET circuits due to the self-alignment of the two gates. Design for XOR and XNOR circuits is suggested to improve the speed and power. These circuits act as basic building blocks for many arithmetic circuits. This paper contrasts and evaluates the performance of conventional CMOS and FinFET based XOR-XNOR circuit design. It is based on the study of high speed, low power, and small area in XOR-XNOR digital circuits. The proposed FinFET based XOR and XNOR circuits have been designed using Cadence VIRTUOSO Tool applying voltage supply of 0.2 to 1.2 voltages, with temperature at 27^0C and all the simulation results have been generated by Cadence SPECTRE simulator at 45nm technology. Simulation results exhibit low power, delay, power, delay product (PDP), and average dynamic power consumption.

KEYWORDS
XOR-XNOR gate; low power; delay; PDP.

1. INTRODUCTION
These days the use of portable electronic devices like cellular devices, laptops has grown exponentially. The main necessity of these portable devices is decreased power consumption, small area and high speed of operation. To meet these necessities research attempts in the field of low power VLSI (very large scale integration) have increased manifolds. As the number of transistors increases on a silicon single chip, the package density also enhances. As the CMOS process technology shrinks, the critical concerns arise with increase in leakage power consumption. The scaling of devices aim at increasing operational speed, reduction in space used and better control on channel by the gate configurations. The scaling of CMOS technology is based on Moore's law which says that the number of transistors on a chip doubles every 18 months.

Less power consumption is one of the most important factors in CMOS circuit design. Lowering the supply voltage (VDD) is a good way to reduce power consumption. On the other hand, when VDD is lowered, gate delay is enhanced and hence operating frequency is decreased. Recently two techniques have been proposed which enable VDD reduction without the performance degradation [1]. The demand for high density circuits and the dependency of the leakage current on the thickness of oxide(t_{ox}) and threshold voltages (V_{th})are emerging as big requirements in deep sub-micron CMOS technology. There are various factors responsible for the leakage current such as the gate leakage current due to very thin t_{ox} and the sub threshold leakage current due to low V_{th} [2]. As technology becomes proportionally small, it requires not only very ultra-thin t_{ox} to keep the current driving but also very low V_{th} to maintain the device speed and V_{th}variations under control when dealing with short-channel effects (SCEs) [3].

When the transistor is in OFF state, the current flows between the drain to source terminals, this current is also called sub threshold leakage current. The sub threshold current also passes when the gate to source voltage V_{gs} of transistor is less than the threshold voltage V_{th}. As technology scales down, the threshold voltage $V_{th}$of the transistor diminishes resulting in exponential improvement in sub threshold leakage current. When the current flows from the gate through the oxide layer to substrate, it is called gate leakage current. The gate leakage current of the transistor also enhances with the reduction of the t_{ox} over the linear region of the transistor [4]. Continuous shrinking of channel length increases the speed of devices in very large scale circuits [5]. This stable miniaturization of transistor with new contemporaries in bulk CMOS technology has yielded repeated improvements in the performance of digital circuits. The scaling of CMOS device faces significant challenges in the future due to fundamental material and procedure technology limitations.

Scaling limitations of CMOS technologies, for instance short channel effects or leakage currents impose the introduction of new device concepts like silicon-on-insulator (SOI) and/or multi-gate transistors [6]. However, scaling of MOS becomes considerably difficult for technology nodes below 45 nm, where the proximity source and drain cuts down the control of the gate over the channel leading to unacceptable short channel effects [7]. In 45nm technology, FinFET based designs offer better control over SCEs, low power, low leakage and better yield [8] which help to overcome the challenges in scaling. Thinner gate oxide assists in improvement of the short-channel effects (SCEs) [9].

FinFETs are 3D structures that rise above the planar substrate, providing them more volume than a planar gate for the similar planar area. Given the tremendous control of the conducting channel by the gate, which "wraps" around the channel, very small current is allowed to flow through the body when the device is in the OFF state. This allows the use of smaller threshold voltages (V_{th}), which yielding to optimal power and switching speeds. FinFETs are scalable as long as it is possible to scale the thickness of the channel.

Double gate MOSFETs (DG) body potential, controlled from two sides due to this DG MOSFET, has higher short channel effect immunity [10]. FinFET a double gate device in which second gate is added opposite to the first gate has long been discerned for it has better control on short channel effect [11]. Fabrications of FinFET devices are same as CMOS devices [12]. In this paper, short gate FinFET is used. XOR –XNOR circuits are the sub-circuits that are mostly used in various circuits' especially-Arithmetic circuits (Full adder and multipliers), Compressors, Comparators, Parity Checkers, Code converters, Error-detecting or Error-correcting codes and Phase detector. The performance of complex logic circuit is enhanced by the individual performances of the XOR-XNOR

circuits [13]. Several designs are available to realize the XOR-XNOR function using different logic styles [14]. The proper selection of XOR-XNOR circuit can add to the performance of large number of circuits. It optimizes the design for reduced delay, lesser PDP and lesser degradation on output voltage level. The aim to design XOR-XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with less number of transistors to implement it [15].

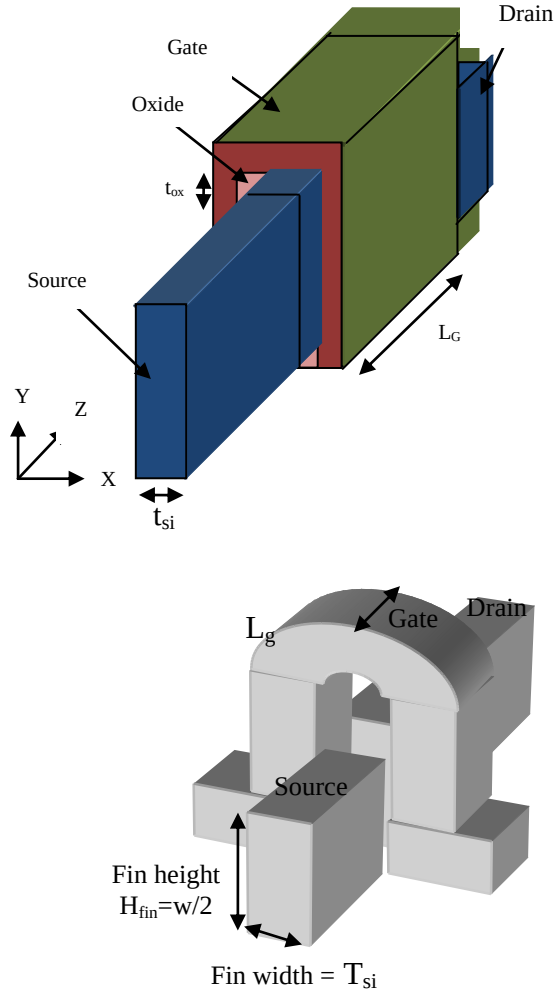

Fig. 1 3D structure and cross-sectional view of FinFET device

The remainder of this work is organized as follows. Section II gives the idea on previous works done on XOR and XNOR circuits in past two decades. Section III gives a short introduction to the proposed FinFET based XOR and XNOR circuit design. Simulation results are compared in section III. Some conclusions are shown in Section IV.

2. PREVIOUS WORK

Exclusive–OR (XOR) and Exclusive-NOR (XNOR) circuits have complementary functions with regards to each other. The binary operations perform the following Boolean Functions-

$$A \oplus B = A'B + AB' \quad (1)$$

$$A \odot B = A'B' + AB \quad (2)$$

A lot of designs were recorded to recognize the XOR-XNOR functions using different number of transistors, techniques and approaches [16][17][18][19][20][21].To amend the circuit performance in terms of speed and density the transistor count and methodologies kept changing in these previous papers. In [16] the conventional design of XOR-XNOR circuit using static CMOS network can be found. The inputs are connected to both an NMOS transistor and a PMOS transistor. It furnishes a full output voltage swing with many numbers of transistors.

The XOR-XNOR circuits based on transmission gates are described in [17]. This circuit design uses complementary inputs and eight transistors and has a hitch of loss of driving capability. XOR-XNOR circuits also have inverter based design. Inverter based design does not necessitate complementary inputs. However, it has no driving capability because there is no straight connection to VDD and GND. By adding a standard inverter to the output, this circuit design has been improved. This altered circuit provides a good driving capability but uses dozen transistors for XOR-XNOR circuits.

Design in [18] suggested two of XOR-XNOR circuits (Fig.2 and Fig.3) and claimed to have lower PDP, less power dissipation, and as swift as the design proposed in [19] with a low supply voltage. On the other hand, both the circuits provide a poor signal at output voltage in definite input signal combination. The XOR-XNOR circuit based on Pass Transistor Logic (PTL) using 6- Transistor is described in [20] as illustrated fig. 4. This circuit design exhibits full output voltage swing and better driving capability by using VDD and GND connection.

Design in the [21] is an improved version of [20] shown in fig. 5 and has improved power-delay product and higher noise resistance. The XOR-XNOR circuit contributes a forward and backward feedback between the XOR-XNOR gate in [19] and additional transistors to correct the tarnished logic level problems. This configuration shown in fig. 4 furnishes an improved performance of the circuit.

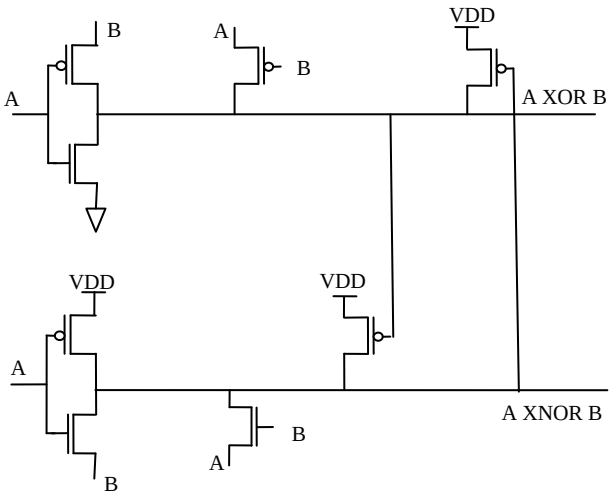

Fig. 2 XOR-XNOR gate using 8 transistors in [18]

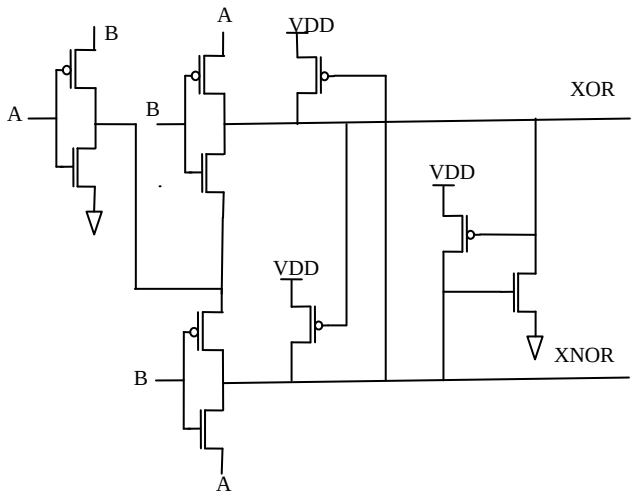

Fig. 3 XOR-XNOR gate using 10 transistors in [18]

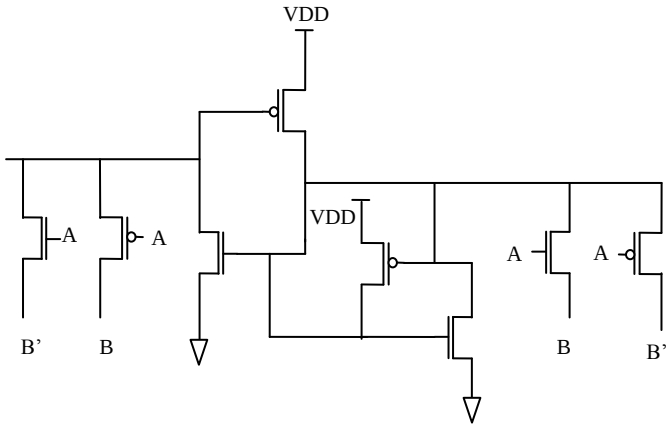

Fig. 4 XOR-XNOR gate using 8 transistors in [19]

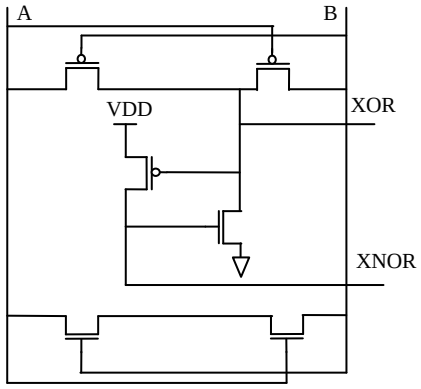

Fig. 5 XOR-XNOR gate using 6 transistors in [20]

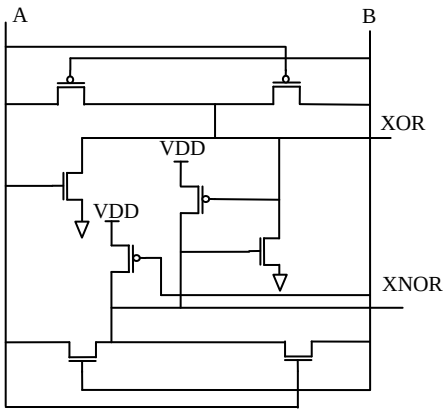

Fig. 6 XOR-XNOR gate using 8 transistors in [21]

3. PROPOSED XOR-XNOR GATE CIRCUIT

In Fig 7, the proposed circuit design of XOR-XNOR gate using 6- Transistors is displayed. This circuit design uses a concept of pass transistor and MOS inverter. The use of inverter is a driving output to attain a perfect output swing. VDD connection to transistor E3 and E4 are used to drive a good output of '1' (high). The output of XOR becomes '0' (low) when transistor E4 is used to drive the output signal and input signal A=B=1. In this condition, when transistor E1 and E2 are ON, they will pass a poor signal '1' with respect to the input of inverter. The output XOR will also be disgraced and accomplish a good output signal, transistor E4 is ON when output of XOR is '0', and it will pass the ideal signal '1' from VDD to the XOR.

Table 1. XOR and XNOR Gate Function

Input		Output	
A	B	XOR	XOR
0	0	Good 0	Good 1
0	1	Good 1	Good 0
1	0	Good 1	Good 0
1	1	Good 0	Good 1

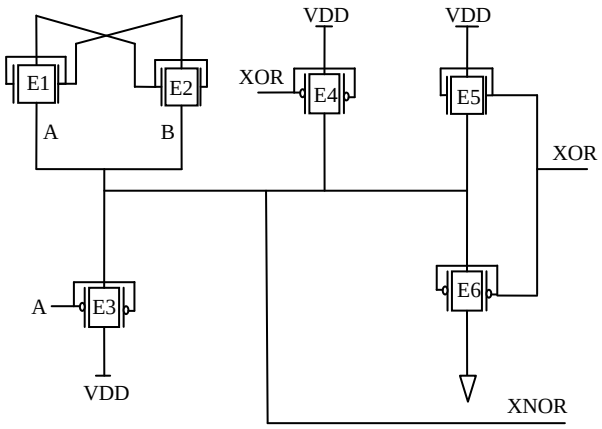

Fig. 7 Proposed XOR-XNOR gate using 6 transistors

The XOR-XNOR gate circuit simulation results have been generated by Cadence SPECTRE simulator in the voltage range 0.2 to 1.2 at 45nm technology. Simulation is performed

by changing supply voltages to show the effect of different voltages to the power dissipation of XOR-XNOR circuit. The analysis has been carried out on the combination of XOR-XNOR, based on the previous design. The delay has been computed between the time when the changing input reaches 50% of voltage level and the time its output reaches 50% of voltage level for both rise and fall transition. The power-delay product (PDP) is measured as the product of the average delay and the average power.

Table 2 shows the comparative output value for XOR-XNOR circuits for each input combination. In table 3, results of simulation have been listed which include a delay, power dissipation and power delay product as represented in Fig. 8,9,10,11,12. The overall PDP for the proposed circuit has improved more than 50% from previous circuits except from the circuit in [20], but nearly similar at the low supply voltage.

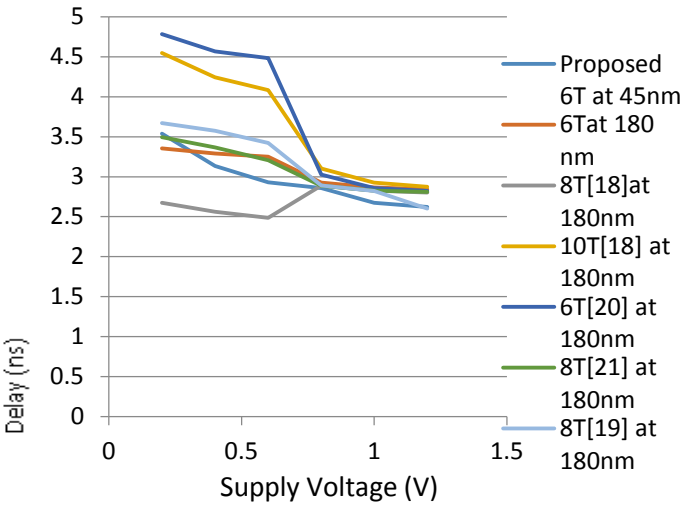

Fig.8 worst case delay of different XOR circuit

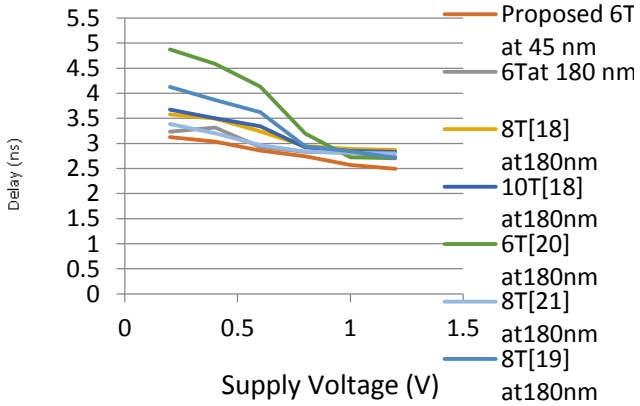

Fig. 9 worst gate delay of XOR circuit

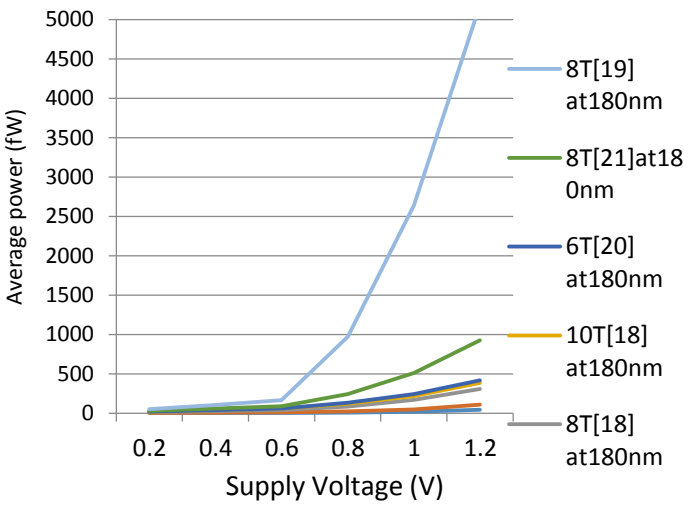

Fig. 10 Power consumption of different XOR-XNOR circuit

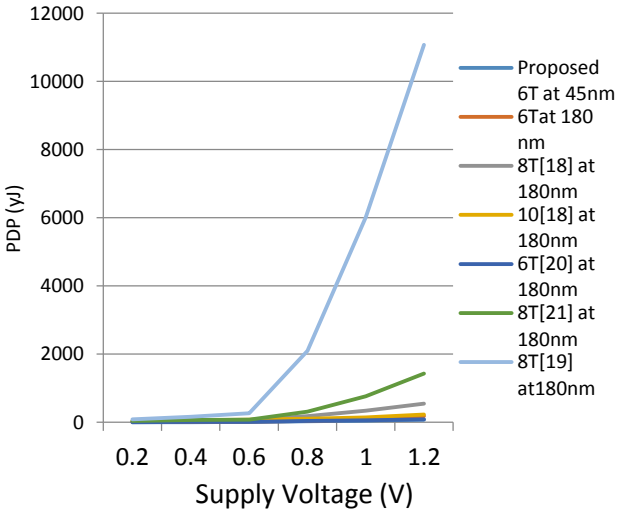

Fig.11 Power-delay products (PDP) of different XOR circuit

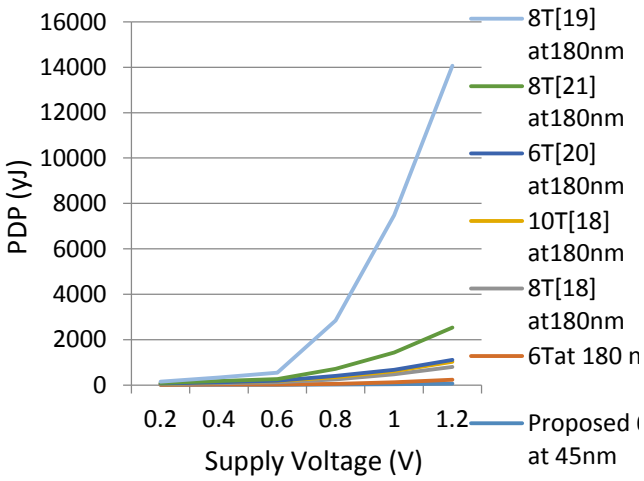

Fig. 12 Power-delay products (PDP) of different XNOR circuit

Table 2. Comparison of Output Value for XOR-XNOR Gate

Inputs		Proposed 6(T)		8T [18]		10T [18]		6T [20]		8T [21]		8T[19]	
A	B	XOR	XNOR	XOR	XNOR	XOR	XNOR	XOR	XNOR	XOR	XNOR	XOR	XNOR
0	1	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Good 0	Good 1
0	0	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Bad 0
1	1	Good 1	Good 0	Bad 0	Good 0	Good 1	Bad 0	Good 1	Good 0	Bad 1	Bad 0	Bad 1	Good 0
1	0	Good 0	Good1	Good 1	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Bad 1

Table 3. Simulation Result of XOR-XNOR Gate

	Voltage (V)	Proposed 6T at 45nm	6Tat 180 nm	8T [18] at 180 nm	10T [18] at 180 nm	6T [20] at 180 nm	8T [21] at 180 nm	8T [19] at 180nm
Delay for XOR (ns)	0.2	3.537	3.356	2.674	4.546	4.782	3.495	3.672
	0.4	3.134	3.292	2.561	4.243	4.567	3.367	3.576
	0.6	2.93	3.252	2.484	4.083	4.483	3.205	3.422
	0.8	2.857	2.925	2.892	3.101	3.025	2.886	2.891
	1	2.674	2.865	2.825	2.928	2.86	2.828	2.824
	1.2	2.621	2.843	2.802	2.874	2.823	2.81	2.603
Delay for XNOR (ns)	0.2	3.123	3.232	3.576	3.675	4.873	3.386	4.129
	0.4	3.037	3.313	3.494	3.498	4.586	3.198	3.867
	0.6	2.854	2.926	3.239	3.339	4.136	2.966	3.62
	0.8	2.743	2.832	2.947	2.922	3.195	2.835	2.942
	1	2.567	2.813	2.89	2.852	2.72	2.81	2.844
	1.2	2.495	2.731	2.867	2.831	2.701	2.798	2.711
Average power for XOR-XNOR (fW)	0.2	1.34	2.42	7.34	5.86	1.98	13.34	19.86
	0.4	2.89	4.49	19.82	11.57	2.23	17.54	44.89
	0.6	4.56	6.379	27.7	19.93	2.251	25.69	77.46
	0.8	8.94	12.62	64.36	33.65	13.75	109.4	726
	1	19.86	28.78	121.4	50.19	21.36	270.5	2129
	1.2	44.67	65.04	196.2	79.98	30.55	510.3	4254
PDP for XOR (fJ)	0.2	3.91	7.87	26.52	34.56	6.03	43.83	84.54
	0.4	6.74	12.51	43.93	56.87	8.89	67.84	167.34
	0.6	16.62	20.75	68.8	81.38	10.09	82.34	265.07
	0.8	27.87	36.91	186.1	104.35	41.53	315.73	2099
	1	54.67	82.46	343	146.96	61.09	764.97	6012.3
	1.2	74.81	184.9	549.8	229.86	86.24	1433.94	11073
PDP for XNOR (fJ)	0.2	2.19	9.06	23.73	19.35	4.43	31.96	54.34
	0.4	5.96	13.45	53.95	43.89	7.67	54.51	147.86
	0.6	8.63	18.66	89.721	66.55	9.31	76.2	280.41
	0.8	19.72	35.74	198.67	98.33	43.87	310.15	2135.89
	1	35.91	80.96	350.85	143.14	58.1	760.11	6054.88
	1.2	57.95	177.62	562.51	226.42	82.52	1427.82	11532.6

4. CONLUSION

In this paper, the FinFET based 6-transistor design with the combination of the XOR-XNOR circuit configuration. The performance of this circuit has been compared to previous CMOS XOR-XNOR design in terms of delay, power dissipation and PDP. The performances of these circuits have been evaluated by Cadence virtuoso tool and simulation results have been generated by Cadence SPECTRE simulator at 45nm technology. According to the simulation results, the proposed circuit offers better results than the previous design. It offers the lowest power dissipation at a low supply voltage. Based on the simulation results, it has been culminated that the proposed 6-transistor FinFET based XOR-XNOR circuits have better output signal levels, consume less power and have higher speed compared to the previous designs at low supply voltage.

5. ACKNOWLEDGMENT

This research endeavor in this paper was supported by ITM University, Gwalior, India in collaboration with Cadence System Design, Bangalore, India.

6. REFERENCES

[1] S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, et.al., "A 130 nm generation logic technology featuring 70 nm transistors, dual Vt transistors and 6 layers of Cu interconnects." Proc. Int. Electron Devices Meeting, 2000, pp. 567–570.

[2] N. Kr. Shukla, R.K. Singh, and M. Pattanaik, "Stability and Leakage Analysis of a Novel PP Based 9T SRAM Cell Using N Curve at Deep Submicron Technology for Multimedia Applications." International Journal of Advanced Computer Science and Applications 2, pp. 43-49 (2011).

[3] B. Amelifard, F. Fallah, and M. Pedram, "Low-Power Fanout Optimization using Multi Threshold Voltages and Multi Channel Lengths." Proceedings in Design, Automation and Test in Europe, 2006, pp 1-6.

[4] P. R. Anand, and P. C. Sekhar,"Reduce leakage currents in loe power SRAM cell structures. " IEEE International Symposium on Parallel and Distributed Processing with Applications Workshops, 2011, pp 33-38.

[5] L. Zhang, C. Wu, Y. Ma, J. Zhang and et.al, " Chracterization of a novel low-power SRAM bit-cell structure at deep sub-micron CMOS technology for multimedia applications." IETE technical Review 28, pp. 315-318 (2011).

[6] M. Fulde1, J. P. Engelst¨ adter2,3, G. Knoblinger2, and D. Schmitt-Landsiedel, "Analog circuits using FinFETs: benefits in speed-accuracy-power trade-off and simulation of parasitic effects ", Adv. Radio Sci., 5, 285–290, 2007, pp. 287-290.

[7] Seid Hadi Rasouli, Hanpei Koike, Kaustav Banerjee, "High-Speed Low-Power FinFET Based Domino Logic", Design automation conference 978-1-4244-2749-9/09, pp. 829-834.

[8] S. M kang and Y. Leblebici, CMOS digital integrated circuits II, TMH publishing company limited, 2007.

[9] Farshad Moradi, Sumeet Kumar Gupta, Georgios Panagopoulos, Dag T. Wisland, Hamid Mahmoodi, and Kaushik Roy, "Asymmetrically Doped FinFETs for Low-Power Robust SRAMs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 12, DECEMBER 2011.

[10] Jakub Kedzierski, Member, Meikei Ieong, Thomas Kanarsky, Ying Zhang, and H.-S. Philip Wong, "Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation With Ni", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 12, DECEMBER 2004, pp. 2115-2120.

[11] Michael C. Wang, "An Overview of Independent-Gate FinFET Circuit Synthesis", IAENG Transactions on Engineering Technologies – Vol. 4, 2010.

[12] Sherif A. Tawfik and Volkan Kursun, "Low-Power and Compact Sequential Circuits With Independent-Gate FinFETs", Ieee Transactions On Electron Devices, VOL. 55, NO. 1, JANUARY 2008.

[13] Shiv Shankar Mishra, Adarsh Kumar Agrawal and R.K. Nagaria, "A comparative performance analysis of various CMOS design techniques for XOR and XNOR circuits", International Journal on Emerging Technologies 1(1): 1-10(2010), pp. 196- 202.

[14] Aminul Islam A. Imran, Mohd. Hasan, "Variability Analysis and FinFET-based Design of XOR and XNOR Circuit", International Conference on Computer & Communication Technology (ICCCT)-2011,pp. 239- 245.

[15] Nabihah Ahmad and Rezaul Hasan, "A New Design of XOR-XNOR gates for low power application", 2011 International Conference on Electronic Devices, Systems & Applications (ICEDSA).

[16] K. E. Neil H. E. Weste, "Principles of CMOS VLSI Design: A Systems Perspective," 1993.

[17] W. Jyh-Ming, F. Sung-Chuan, and F. Wu-Shiung, "New efficient designs for XOR and XNOR functions on the transistor level," Solid-State Circuits, IEEE Journal of, vol. 29, pp. 780-786, 1994.

[18] S. W. Shiv Shankar Mishra, R. K. Nagaria, and S. Tiwari, "New Design Methodologies for High Speed Low Power XOR-XNOR Circuits," World Academy of Science, Engineering and Technology, 2009.

[19] S. Goel, M. A. Elgamel, M. A. Bayoumi, and Y. Hanafy, "Design methodologies for high-performance noise-tolerant XOR-XNOR circuits," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 53, pp. 867-878, 2006.

[20] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," Circuits, Devices and Systems, IEE Proceedings -, vol. 148, pp. 19-24, 2001.

[21] M. Elgamel, S. Goel, and M. Bayoumi, "Noise tolerant low voltage XOR-XNOR for fast arithmetic," in Proceedings of the 13th ACM Great Lakes symposium on VLSI Washington, D. C., USA: ACM,2003.