Design of High-Speed Low-Power Two Level Voltage Converters using Multi-VTH CMOS Technology

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ABSTRACT
The paper primarily focuses on reducing the power consumption without diminishing the speed of the circuit by using multiple supply voltages (Multi-VDD). Two multi threshold (Multi-VTH) level converter circuits are proposed and it is compared with the conventional circuits for operating at different supply voltages (Multi-VDD). The converter circuits are individually optimized for minimum power consumption and propagation delay. The speed and power consumption for the proposed level converters were analyzed.

General Terms
Voltage level converters, Multi-VTH CMOS technology and low power

Keywords
CMOS, Delay, Threshold, VDD, Voltage level converters, Multi-VTH

1. INTRODUCTION
Design techniques for low power consumption in modern VLSI are becoming more and more important. As technology moves into deep submicron feature sizes, power dissipation due to leakage current is increasing at an alarming rate. Projections show that leakage power will become comparable to dynamic power dissipation in the next few years. Dynamic power is also increasing, and still dominates. Supply voltage has not been scaled aggressively enough to keep power per unit area constant over technology generations. Exacerbating this problem is the growth in die area.

According to Gordon Moore law the no-of transistors in a die is increasing exponentially with time, which dwindles the die performance due to increase in power consumption and die area. One of the best techniques to reduce the power consumption is scaling the supply voltage VDD. During supply voltage scaling, both static and dynamic powers [11, 13] are reduced which decreases the performance of the circuits. In order to maintain generational speed enhancement, the device threshold voltage VTH must also scale down with VDD.

The work considers the effectiveness of the techniques of multiple threshold voltages, multiple supply voltages and sizing the combination of these techniques on both active and leakage power reduction. Level conversion [1, 2] penalties were considered with dual-VDD design. Two values were considered for the lower supply voltage and the higher supply voltage [5, 6]. Level conversion circuits for converting voltage levels from lower voltage to higher voltage levels and its applications were analyzed. Minimization of dynamic and static power through joint assignment of threshold voltages, sizing optimization and algorithm for minimizing standby power in deep submicron dual- VTH circuits [14]. Reduce the delay between CMOS circuits by maximizing the features of wires and change the device parameters design methodologies, for low power and high speed. Low power design techniques [11, 12] using clustered voltage scaling, variable supply voltage scheme, assign multiple threshold voltage and its applications.

2. MULTI-THRESHOLD VOLTAGE
The multi-threshold CMOS [7, 8, 9] (MTCMOS) is a dreadfully attractive technique to reduce sub-threshold leakage currents during standby modes. This technology is simple to use, as existing designs can be modified to become MTCMOS blocks with addition of high-VTH power switches. In addition, circuits can easily be placed in low leakage states at a fine grain level of control. These circuits are used even for normal CMOS circuits where dual threshold voltages are used for pull-up/pull-down networks.

3. EMBEDDING MULTI-VTH CMOS DESIGN IN LEVEL CONVERTERS
The static approach does not employ any control signals for power savings. In the static multi-VTH technique, gates in the critical paths are designed to operate at a high-VTH in order to reduce leakage power without compromising the performance; similarly the gates are operated at a low-VTH to maintain high performance. However in aggressive high-performance low- power circuit topologies that have several balanced critical paths, many gates cannot be slow down, hence a merger leakage reduction can be achieved. It is a known fact that some CMOS circuits operate at lower supply voltages (VDDL) while other at high supply voltages (VDDH). In order to overcome static current during circuit operation level converters between the VDDL and VDDH CMOS circuits.

4. EXISTING LEVEL CONVERTERS
4.1 High-Speed Level Converter

The figure 1 shows High-speed level converter (LC1) [3, 4]. This converter boasts improved speed as compared to many other conventional level converters, using feedback loop. Transistor M6 maintains the voltage of Node3 between VDDL and VDDL + VTHN in order to enhance the current produced by M1. The capacitor C stabilizes the voltage of Node3 against the noise induced in close proximity switching events. The circuit operates as follows: when the input is at 0V, Node 1 is discharged through M1 while M3 is turned ON and M2 is turned OFF. Node 2 is charged to VDDH, turning M4 off. The output is discharged to 0V. When the input transitions to VDDL, M2 is turned on. Node1 is initially charged to a voltage between VDDL - VTHN and VDDL through M1.

M3 is not completely cut off (weakly active). M2 is sized to be stronger than M3 for the circuit to function properly. When Node2 is discharged, M4 is turned ON while charging Node1 to VDDH, thereby eventually turning M3 OFF. The output transitions to VDDH. When the input switches from 0V to VDDL there is a direct current path from VDDH to GND through the M2–M3 path. This direct current path exists until Node1 is charged to VDDH via M4 and M5. Similarly, when the input switches from VDDL to 0V, there is a direct current path from VDDH to GND through the M5 - M4 - M1 path.

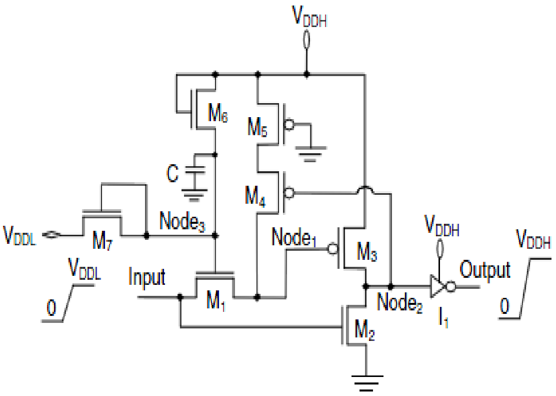

Fig 1: High speed level converter LC1.

This direct current path exists until Node2 is pulled up to VDDH and M4 is turned off. This states that LC1 consumes significant short-circuit power, during both low-to-high and high-to-low transitions of the output. This direct current path exists until Node 2 is pulled up to VDDH and M4 is turned off. In addition to this, even when VDDL is reduced, M2 maintains the required voltage, due to its increased size. The load seen by the driver circuit therefore increases at Lower VDDL and the tapered buffers are driving this circuit at very low voltages. Although this circuit eliminates leakage current and improves speed, it produces short-circuit current due to charging and discharging.

5. PROPOSED LEVEL CONVERTER

5.1 Multi-Vth Based Level Converters

Three multi-VTH level converters are analyzed and the results are compared. Unlike the previously published level converters that rely on feedback, the proposed level converters employ a multi-VTH CMOS technology [6, 7] in order to eliminate the static dc current. The high threshold voltage pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static dc current problem.

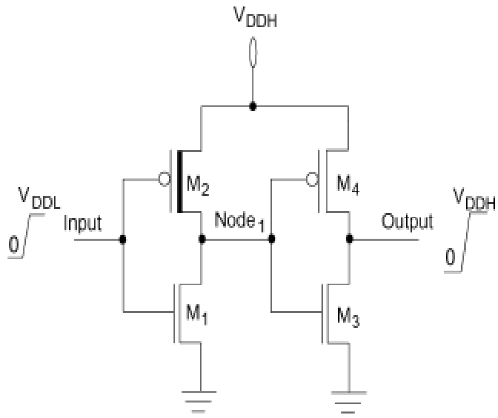

Fig 2: Multi-V_{TH} based level converters (PC1)

The first proposed level converter (PC1) is shown in Figure. 2. PC1 is composed of two cascaded inverters with multi-VTH transistors. The threshold voltage of M2 (VTH-M2) is low for avoiding static DC current in the first inverter (M1 and M2) when the input is at VDDL. |Vth-M2| is required to be higher than VDDH - VDDL for eliminating the static DC current.

When the input is at 0V, M2 is turned ON, M1 is cutoff and Node1 is pulled up to VDDH, therefore pulling the output to 0V. When the input transitions to VDDL, M1 is turned on, M2 is turned off since VGS, M2 > Vth, M2, Node1 is discharged to 0V and output is charged to VDDH. Short-circuit power of PC1 is reduced by eliminating feedback path and by using fewer transistors as compared with LC1, hence there is no need for increasing M1 transistor size.

5.2 Multi-Vth Based High Speed Level Converter

A dc current path exists between VDDH and VDDL through M3 and M4 in PC1. In order to avoid a static dc current path within the level converter, M3 and M4 are eliminated. The circuit configurations of the second proposed level converter (PC2) for operation at different supply voltages are shown in Fig. 3. (VTH-M2) is required to be higher than VDDH-VDDL for eliminating the static dc current when the input is low (Node1 is at VDDL). M1 needs to be cutoff after “logic 1” is successfully propagated to the output. As the input is at VDDL and the output is at VDDH, there is a possibility of a static dc current path between VDDH and VDDL through M1.

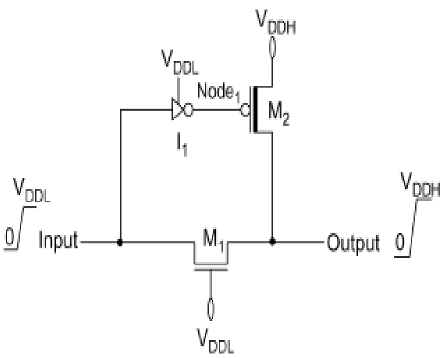

Fig 3: Multi-V_{TH} based high speed level converter PC2.

When the input is at 0 V, logic’0’ is pulled high at I1 turning M2 off. The output node is discharged to 0V through the pass transistor M1.When the input transitions to VDDL, the output node is charged to VDDH due to VDDL-Vthn-M1 through M1. M2 is turned ON after the high-to-low propagation delay of the inverter (I1). The output is pulled high all the way up to VDDH through M2. M1 is turned OFF isolating the two power supplies. Both M1 and M2 assist the output low-to-high transition, thereby eliminating the contention current and enhancing the low-to-high propagation speed. The small transistor count and the elimination of the feedback reduce the power consumption of the proposed level converter as compared to PC1.

5.3 Low Power Level Converter

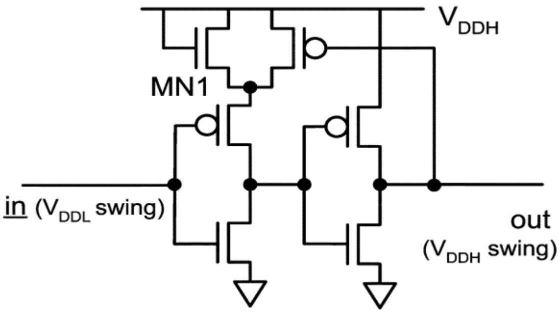

Fig 4: Low-power level converter (PC3)

The figure 4 shows low-power level converter (PC3). This converter consumes less power and has enhanced speed than the other level converters (PC1 and PC2). The threshold voltage of M2 VTH-M2 is required to be higher than 0.6, 0.8, and 1.3 V for VDDL= 1.2, 1, and 0.5 V, respectively, for both PC1 and PC2. Similarly, from the ranges of VTH-M3 for VDDL= 1.2 V and 1 V are 0.13 V 0.6 and 0.33 V 0.8 V, respectively.

The circuits are optimized with two different design criteria for each value of VDDL. When the VDDL is very low the level converters consumes high power. The design and optimization of the circuits are carried out using HSPICE built-in optimizer in a 0.18- µm TSMC CMOS technology. The optimization results are listed in Table 1. The table values depict that the proposed level converters use minimum power. The level converter PC3 is said to consume minimum power than the others. Graphical representation of power consumption is shown in the graphs 1 and 2.

Figures 5, 6 and 7 clearly depict the peak power graph of each of the mentioned level converters. It is found that the level converter consumes more when VDDL value is very low, then the VDDL value is increasing gradually step by step from 0.5v, 1v and 1.2v.The value of VDDH=1.8v. It's a standard nominal supply voltage in CMOS technology.

Table 1: The power consumed by the level converters PC1, PC2 and PC3 with Multi –VTH.

VDDL	VDDH	Name of the level converters	Power in µ watts
0.5V	1.8V	PC1	3.08
		PC2	3.05
		PC3	0.0057
1V	1.8V	PC1	2.11
		PC2	1.72
		PC3	1.0485
1.2V	1.8V	PC1	2.15
		PC2	1.67
		PC3	0.7861

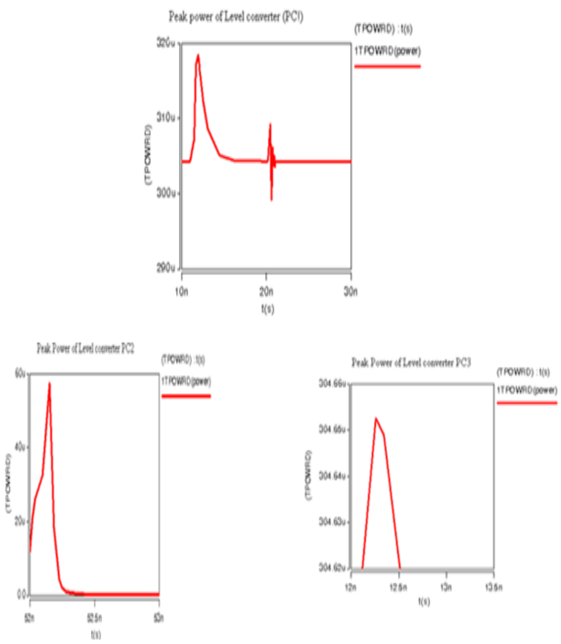

Fig 5: Peak power graph of the level converters

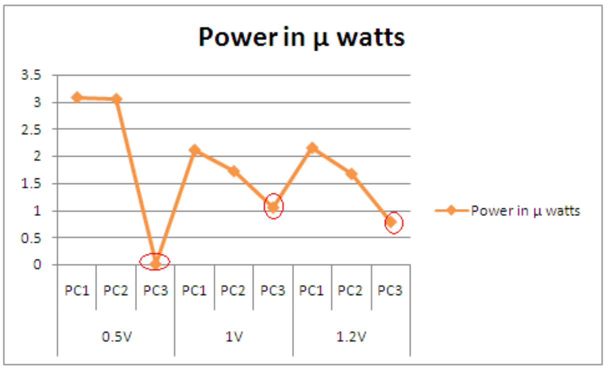

Fig 6: Power utilization graph for low threshold voltage

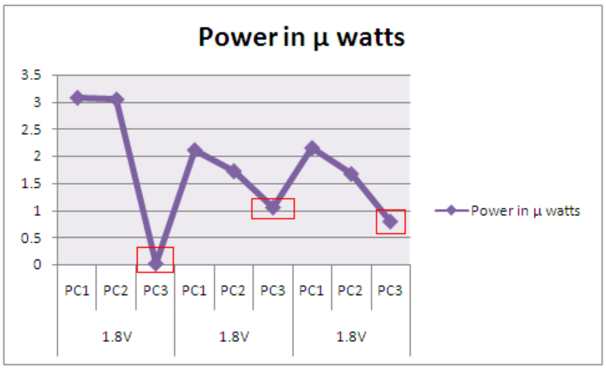

Fig 7: Power utilization graph for high threshold voltage

5. CONCLUSION

In this paper, a two level converters using multi-VTH CMOS technology is designed so as to reduce leakage power under performance constraints. The proposed level converters does not use feedback paths, therefore dc current paths in CMOS gates driven by low-swing input signals, is suppressed. The proposed level converters are compared with the previously published circuits for different values of the lower supply voltages in a multi-VDD system. When the circuits are individually optimized for minimum power consumption in a 0.18-m TSMC CMOS technology, the proposed level converter offers significant power saves and enhance speed compare to other level converters.

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