Reliability Study of Single Stage Multi-Input Majority Function for QCA

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ABSTRACT
Due to the physical limitations faced by CMOS (Complementary Metal Oxide Semiconductor) scaling many technologies were suggested to replace CMOS on the nanoscale. Most of the suggested technologies are not deterministic and follow the Law of Large Number LLN. So, the reliability inspection is essential to these technologies. In this paper the PTM (Probabilistic Transfer Matrix) is used to inspect the reliability of multi-input majority function for QCA (Quantum dot-Cellular Automata). This study conclude that the single-gate with multi-input Majority has the same reliability of its 3-input form. To extend the results to digital circuits, the full adder is used as a test bench. The results show the superiority of the full adder version designed with 5-input majority gate upon other designs from reliability point of view.

General Terms
Reliability in emerging technologies

Keywords
Reliability of majority gate, QCA, full adder

1. INTRODUCTION
For CMOS the study of error and faults sources could be done on the components level theoretically and physically, while in QCA the error sources can be studied theoretically only since up to this moment no QCA chips have been produced. In this paper the reliability of basic element in QCA which is the majority function with its three input and multiple input forms will be studied. The full adder designed in with QCA will be used as a test bench to compare the reliability of the different majority forms.

2. QCA BASICS

2.1 QCA Definitions
The current chips integration technology is reaching to its physical limits. So, there are a lot of proposed technologies that can be used at the nano scale. One of these is quantum dot cellular automata (QCA).

The theory of QCA was proposed by Lent et al. in 1993 [1]. QCA encodes binary information in the charge configuration within a cell. Coulomb interaction between cells is sufficient to accomplish the computation in QCA arrays-thus no interconnect wires are needed between cells. No current flows out of the cell so that low power dissipation is possible.

A simple QCA cell consists of four quantum dots arranged in a square, shown in Figure (1).

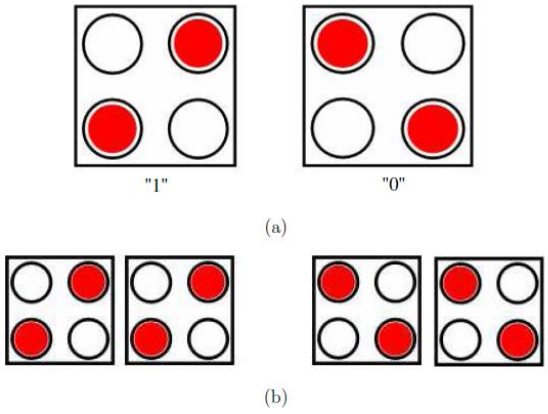

Figure (1) Schematic of a QCA cell. (a) Two states "1" and "0" in a single cell. (b) Coulomb interactions couple the states of neighboring cells.

Dots are simply places where a charge can be localized. There are two extra electrons in the cell that are free to move between the four dots. Tunneling in or out of a cell is suppressed. The numbering of the dots in the cell goes clockwise, starting from the dot on the top right. A polarization P in a cell, which measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as Eq.(1)

$$P = \frac{(p_1+p_3)-(p_2+p_4)}{p_1+p_2+p_3+p_4} \quad (1)$$

Where P_i denotes the electronic charge at dot i. Because of Coulomb repulsion, the electrons will occupy antipodal sites. The two polarized charge configurations P = ¡1 and P = 1 correspond bit value of 0 and 1 respectively. These two states are used to encode the binary information. When a polarized cell is placed close to another cell in line, the Coulomb interaction between them will force the second cell switch into the same state as the first cell, minimizing the electrostatic energy in the charge configuration of the cells. Based on the Coulomb interaction between cells, fundamental QCA devices can be built.

2.2 QCA Clocking
Since there is no current flow in QCA wire so to control signal flow direction and for Timing control, to restore the lost signal energy to the environment, creating pipelines if multiple clock signals could be used, forcing the circuit to stay in the quantum mechanics ground state and other reasons discussed by Hennessy et al. in 2001 [2] the QCA wire should be clocked. A lot of methods were proposed for clocking and

all of them had four phases with different timing for each phase.

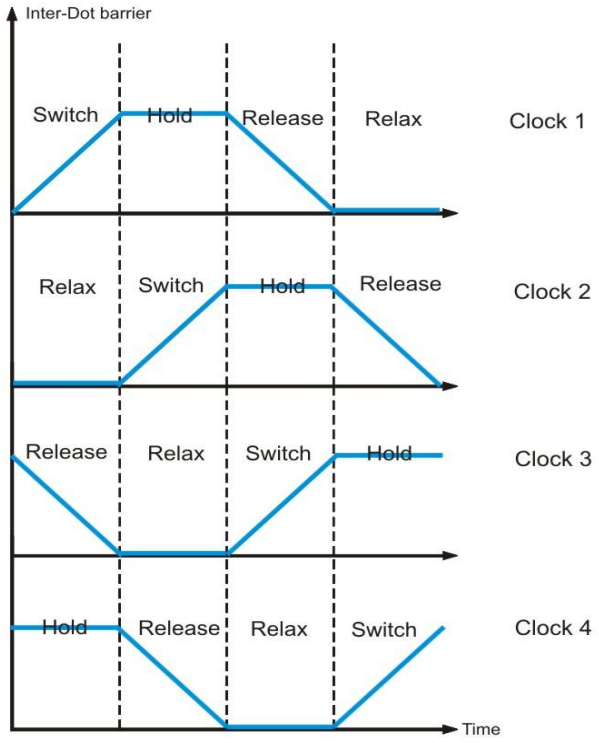

Figure (2) The four phases of the QCA clock (switch, hold, release, relax) and the transition of phase in order to move a bit in a wire left to right.

The clocking field with four phases shown in Figure 2 cannot be changed with the usual clock signal with two phases (high and low) because if abrupt switching is used The Input is changed suddenly to the QCA circuit and the circuit would be in some excited state and try to relax to ground state by dissipating energy to the environment, the relaxation will be inelastic and uncontrolled, and The circuit may enter a metastable state that is determined by local and not global ground state.

While for the four phase switching the clock signal is designed to ensure adiabatic switching (four phases signal), the relaxation is controlled by the switch and release phases of the clock signal, and the circuit is always kept in its instantaneous ground state.

3. RELAIBILITY WITH PTM

3.1 Theory

The study of the reliability of the majority gate had been inspected most of the times using the Probabilistic Transfer Matrix (PTM) [3] The PTM can be defined as the tensor product of gates' probabilities matrices. The computation of PTM matrix for NAND gate is shown in figure (3).In this figure the probability of the output for each input pattern is considered to form the individual gate matrix which describe the error probability of this gate. Now to compute the entire probability of the circuit the PTM for each gate need to be computed then the final reliability of the circuit can be obtained using the tensor products of the PTMs after dividing the circuits into suitable levels. From the circuit PTM the overall reliability of the circuit can be derived easily. For further information on calculating the PTM for multi-level QCA circuits reference [4] will be useful.

$$\begin{array}{c|cc} \text{Input} & 0 & 1 \\ 00 & p & 1-p \\ 01 & p & 1-p \\ 10 & p & 1-p \\ 11 & 1-p & p \end{array}$$

Figure (3) Illustration of PTM construction for the NAND gate

3.2 The PTM calculations for majority function

To study the reliability of the multi-input majority function one should start with constructing the PTM for the 3-input majority gate and compute the reliability of it. The PTM for the 3-input majority gate is illustrated in Figure (4).

To construct the overall circuit reliability from the PTM matrix the following steps is followed [4] :

- Construct the Truth table of the circuit. Which called ITM
- Multiply ITM by the PTM element wise multiplication.
- The non desirable element p is substituted by 0 after multiplication and the matrix called ETM. As in figure (2.c)
- The probability of each input combination is used to form a row vector called (for the majority example this vector has 8 elements since there are 3 inputs. Assuming equal probabilities of occurrence for inputs, the vector's elements will be 0.125. the result will be v *ETM =[0.5(1-p) 0.5(1-p)]).
- To calculate the final reliability of the circuit the elements of the result are summed together. (For the majority example the result is (1-p)).

Using the same approach the PTMs for the five-input and seven –input majority functionsare constructed and MATLAB is used to compute the overall reliability of these functions which ware equal to the reliability of the three-input majority function as a gate and as shown from the results in Figure (5) where different values of probability of error (p) are used and in both cases different probability of occurrence for each input and the equal probability of occurrence of each input.

$$\begin{array}{c|cc} Input & & \\ 000 & 1 & 0 \\ 001 & 1 & 0 \\ 010 & 1 & 0 \\ 011 & 0 & 1 \\ 100 & 1 & 0 \\ 101 & 0 & 1 \\ 110 & 0 & 1 \\ 111 & 0 & 1 \end{array} \quad \begin{vmatrix} 0 & 1 \\ 1-p & p \\ 1-p & p \\ 1-p & p \\ p & 1-p \\ 1-p & p \\ p & 1-p \\ p & 1-p \\ p & 1-p \end{vmatrix} \quad \begin{vmatrix} 0 & 1 \\ 1-p & 0 \\ 1-p & 0 \\ 1-p & 0 \\ 0 & 1-p \\ 1-p & 0 \\ 0 & 1-p \\ 0 & 1-p \\ 0 & 1-p \end{vmatrix}$$

a)T. Table(ITM) b)PTM c) Product (ETM)

Figure (4) the PTM for the 3-input majority gate

According to our best knowledge the reliability of the multi-input majority gate has not been inspected only in [5] where the reliability of the computation with majority function was investigated using a multi-level ternary tree of majority gates and Probability Gate Model (PGM). The results showed that when the number of the inputs for the majority tree increase the reliability will decrease and any none zero error components cannot be tolerated for long computation.

From the obtained results in this work one can say that the single gate multi-input majority functions (5, 7 input) have the same reliability of the three input majority function

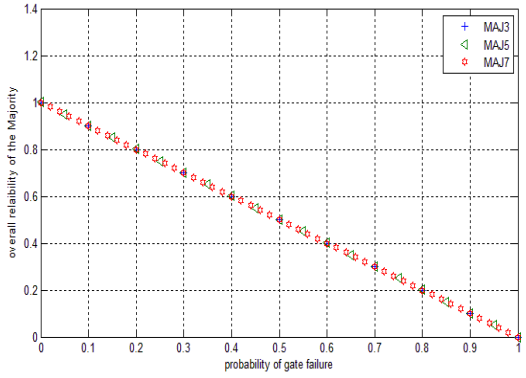

Figure (5) Reliability comparison of 5-input and 7-input majority functions with the 3-input Majority function

4. PTM FOR FULL ADDERS

Now to do further investigation the reliability of circuits built with multi-input majority function is studied and the one bit full adder cell introduce in [6] and illustrated in Figure (6) is taken as an example by dividing the circuit to sub-circuits and driving the overall PTM of it. To do that the special matrices introduced in [7] for two wires swap and three wires swap, the (n x n) Identity matrix, and gate fan2 matrix showed in Figure (7) & (8) respectively need to be considered. The final expression for PTM for MAJ5 full adder is given in eq.(2)

$$PTM = L1 * L2 * L3 * L4 * L5 * L6 * L7 \qquad (2)$$

$$PTM = (FAN2A \otimes FAN2B \otimes FAN2Cin) * (SWAP2 \otimes SWAP3 \otimes I2 * MAJ3 \otimes I8 * FAN2 \otimes I8 * NOT \otimes I16 * FAN2 \otimes I16 * MAJ5 \otimes I2$$

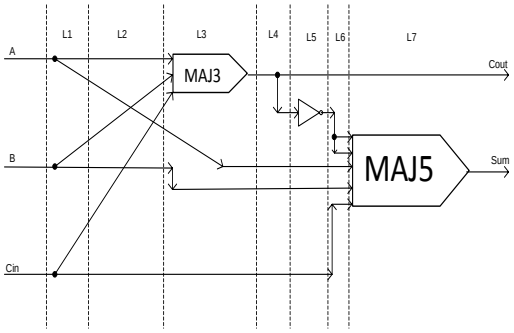

Figure (6) One bit full adder cell built with 5-input majority gate divided into 7 sub-circuits

$$\begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix} \quad \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{vmatrix} \quad \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{vmatrix}$$

(a) b) (c)

Figure (7) Wire swap matrices: (a) 2-wire swap matrix; (b) and (c) 3-wire swap

Matrices

$$I = \begin{vmatrix} 1 & 0 \\ 0 & 1 \end{vmatrix}, F_2 = \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix}$$

Figure (8) Special matrices used in PTM computation. a) Identity matrix b) Gate Fan2 Matrix c) Two wire swap matrix

Where

FAN2A=FAN2B=FAN2Cin=FAN2=Matrix F_2 in Figure (8).

SWAP2=Matrix a in Figure (7).

SWAP3=Matrix c in Figure (7) because the wire swap is like type c.

MAJ3=Matrix b in Figure (4).

I2, I8, and I16 are Identity Matrices of sizes (2 x 2), (8 x 8), and (16 x 16) respectively.

MAJ5= The PTM matrix of 5-input Majority gate calculated with the same methodology used for 3-input Majority.

5. RESULTS

Using MATLAB to compute eq.(2) enable us to find the probability of failure of the Sum and Cout outputs of the 5-input Majority full adder for every gate probability of failure .

The reliability of the previous designs of the FA cell was studied in [8] using PTM approach for four designs presented in Figure (9), where a) is the conventional XOR FA, b) conventional Majority based FA, c)Reduced no. of majority gates FA, and d)Minority based full adder.

The results shown in Figure (11) for the Sum and Cout reliabilities are obtained.

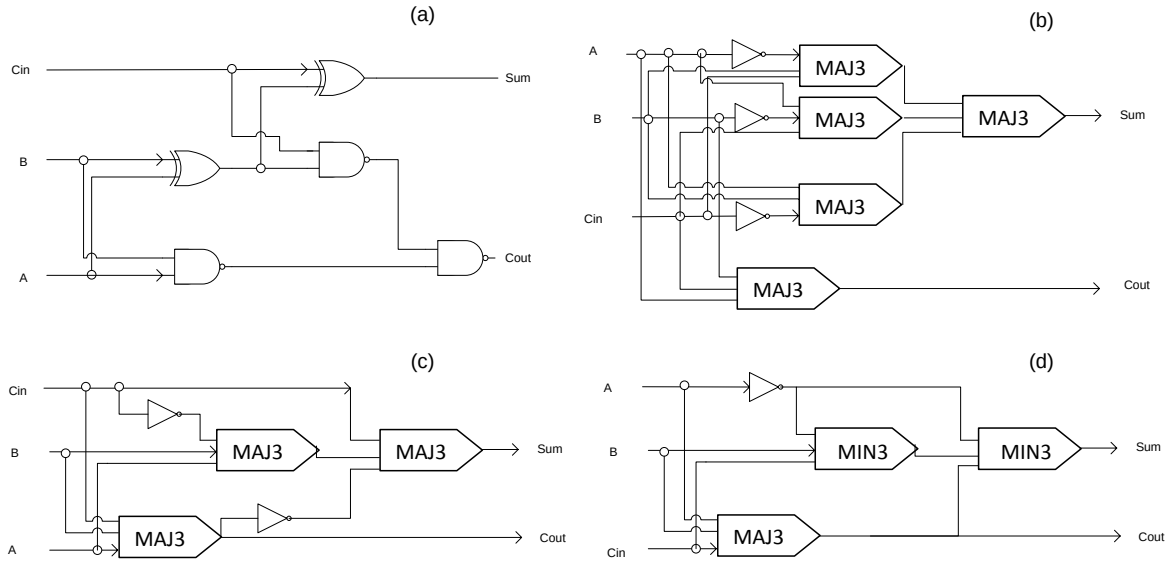

Figure (9) Calculating PTM for four full adder implementation. a) XOR-FA b) MAJ3-FA c) R-MAJ3-FA d) MIN-FA [8]

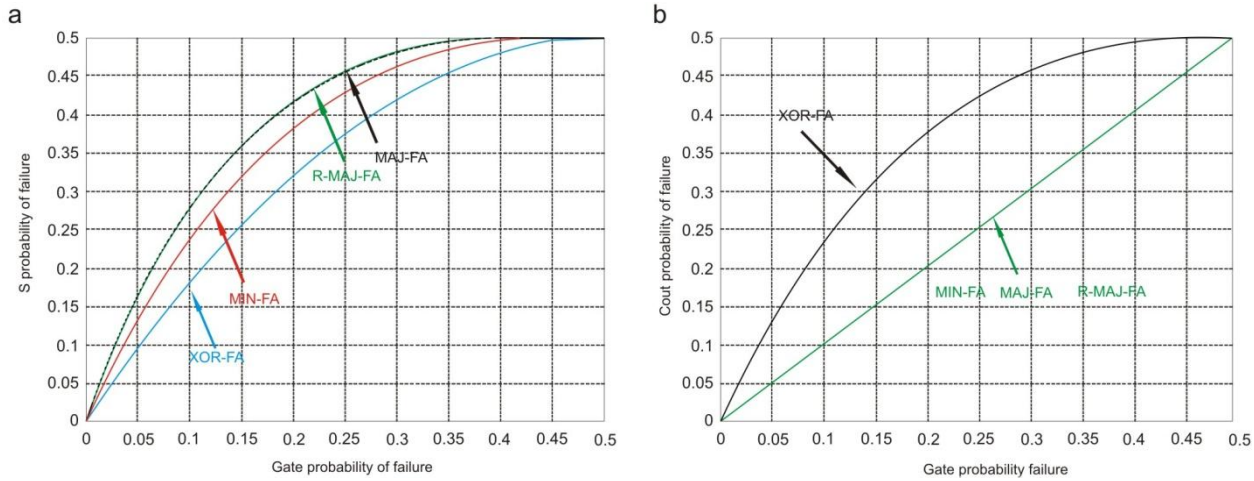

Figure (10) Probability of Sum and Carrey out with respect to gate probability of failure for the four FA illustrated in Figure (9)[8]

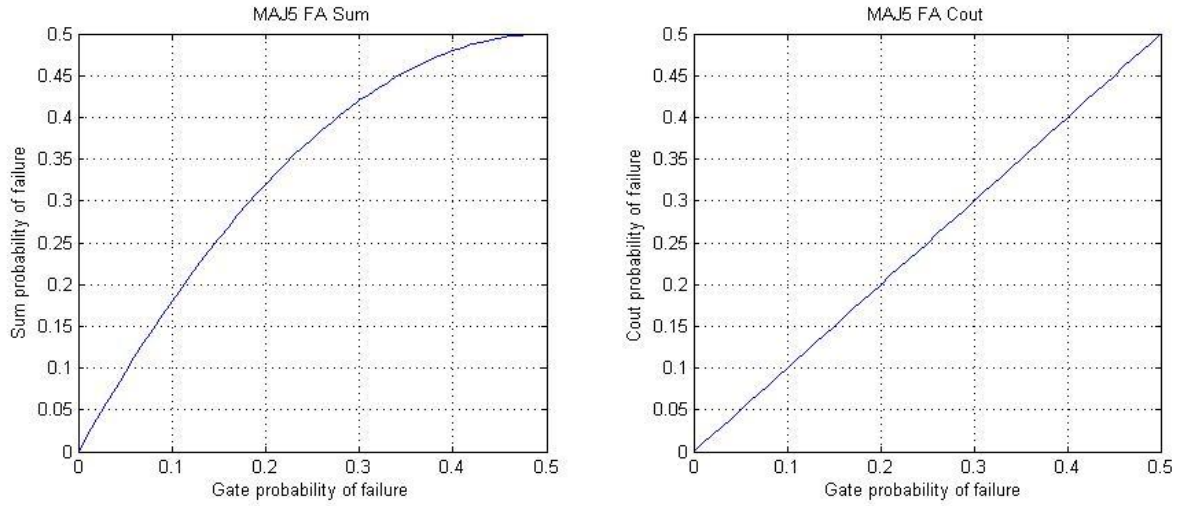

Figure (11) Probability of Sum and Carry out with respect to gate probability of failure for the 5-input Majority based FA

6. CONCLUSIONS

It can be seen from noticing the previous results that the XOR FA gives the best result for the sum output and the other three designs give the same result for the carry out output which is better than the XOR FA. This is a normal result since they have only majority gate in the path of the carry output.

For the FA built with the 5-input majority gate it can be seen from Figure (11) that the probability of failure of carry out output is equal to one obtained from the three majority designs and for the sum output it's equal to the one obtained from the XOR FA. It can be said that the FA cell designed with 5-input majority function has better overall reliability than the previous designs. This result is a good motive to try to redesign the other basic arithmetic cells with the multi-input majority function.

7. REFERENCES

[1] Lent, C. S., et al., "Quantum cellular automata," *Nanotechnology*,Vol. 4, No. 1, 1993, pp. 49-57.

[2] Hennessy, K. and C. S. Lent, "Clocking of Molecular Quantum-Dot Cellular Automata," Journal of Vaccum Science and Technology, Vol. 19, No. 5, 2001, pp. 1752-1755.

[3] Krishnaswamy, S., Viamontes, G.F., Markov, I.L., Hayes, J.P.," Accurate reliability evaluation and enhancement via probabilistic transfer matrices ",Proc. Of Design, Automation and Test in Europe,Vol. 1 pp.282-287, March 2005

[4] Dysart Timothy J. and Kogge. Peter M. ," Probabilistic Analysis of a Quantum-Dot Cellular Automata Multiplier Implemented in Different Technologies", 4th Non-Silicon Computing Workshop in conjunction with the 34th International Symposium on Computer Architecture and FCRC 2007. San Diego, CA. June 9, 2007.

[5] Jie Han, Erin R. Boykin, Hao Chen, Jinghang Liang, and Jos´e A.B. Fortes, "On the Reliability of Computational Structures Using Majority Logic", IEEE Trans. On Nanotechnology, Vol. 00, NO. 00, 2011.

[6] Rahimi M., Kavehei O., Navi K., "A Novel Design for Quantum-dot Cellular Automata Cells and Full-adders," Journal of Applied Sciences, 2007, 7, 3460–3468.

[7] Smita Krishnaswamy, George F. Viamontes, Igor L. Markov,And John P. Hayes," Probabilistic Transfer Matrices in Symbolic Reliability Analysis of Logic Circuits", ACM Transactions on Design Automation of Electronic Systems, Vol. 13,No. 1, Article 8, Pub. date: January 2008.

[8] Walid Ibrahim, Valeriu Beiu, and Mawahib Hussein Sulieman, "On the Reliability of Majority Gates Full Adders" , IEEE Transactions On Nanotechnology, vol. 7, no. 1, january 2008