Implementation of Low Leakage and High Performance 8-Bit ALU for Low Power Digital Circuits

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ABSTRACT
The insist for portable devices is fulfilled by the growing CMOS technology. As the size of the transistor shrinks, the leakage power component augments exponentially. Thus it becomes a critical metric for the future technologies. This paper deals with the techniques like GATED VDD, AVLS, AVLG, and AVL for reducing leakage power. These techniques are implemented on 8-bit ALU. 80% of cutback in leakage power can be achieved by applying proposed technique with minimum delay and area overhead. The circuit is simulated on cadence(R) Virtuoso(R) in 90 nanometer CMOS technology.

Keywords
8-bitALU, Gated -V_{dd}, AVLS, AVLG and AVL

1. INTRODUCTION
The need for the low power and portable devices increasing immensely, it is needed to scale down the transistor size. This in turn leads to increase in the leakage power. As technology scales down from 250nm to 45nm, leakage power in the region of dynamic power or it may exceed as technology grows [1]. There are different sources of leakage in CMOS transistor like

1) Reverse biased junction leakage (IREV) (i1)
2) Gate induced drain leakage (GIDL) (i2)
3) Weak inversion leakage (i3)
4) Current due to injection of hot carriers (i4)
5) Gate induced drain leakage (i5)
6) Channel punch through current (i6)

In order to compensate the delay requirements the threshold voltage also must be scaled down with the scaling of supply voltage. Because of this, weak inversion leakage increases exponentially, which is the major leakage component. This leakage is also termed as sub-threshold leakage.

With the perspective that leakage power dissipation in logic circuit would constitute a significant fraction of overall power dissipation, so effectual techniques are desirable to address this problem.

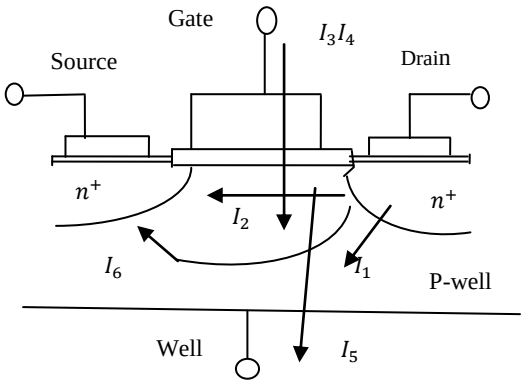


Fig 1: Sources of Leakage Current [3]

Leakage power can be reduced by different ways like cut off the power supply to the circuit, reducing the power supply to the circuit or by increasing ground potential of the circuit when the circuit is in inactive mode [3]. Here four techniques are implemented and one technique is proposed to reduce leakage power. A basic 8bit ALU is designed. The above techniques have been implemented on this ALU.

2. DESIGN OF ALU
An 8bit ALU is designed, which incorporates 6 logical operations, 3 arithmetic operations and a shift operation.

2.1 LOGICAL OPERATIONS
1) NAND
2) NOR
3) AND
4) OR
5) EX-OR
6) EX-NOR

2.2 ARITHEMATIC OPERATIONS
1) ADDER
2) SUBTRACTOR
3) MULTIPLIER

2.3 SHIFT OPERATION

SERIAL IN PARALLEL OUT (SIPO)

All the above logics adorned with a PMOS transistor between the power supply and the actual logic. This PMOS acts as an enable pin for the selection of particular block. Whenever the circuit needs to be ON the PMOS transistor is enabled and allows the power supply to the circuit. The enabling and disabling of logic blocks is done by a selector. Selector is same as a decoder but here NAND gates are used instead of AND gates. With the help of this selector the logical blocks are enabled or disabled. Whenever the incorporated enable pin of the selector is '0', all the outputs will be logic '1' irrespective of inputs. These outputs are given as inputs to the PMOS transistor on the top of every logical block. This leads the logic blocks to get cut off from power supply.

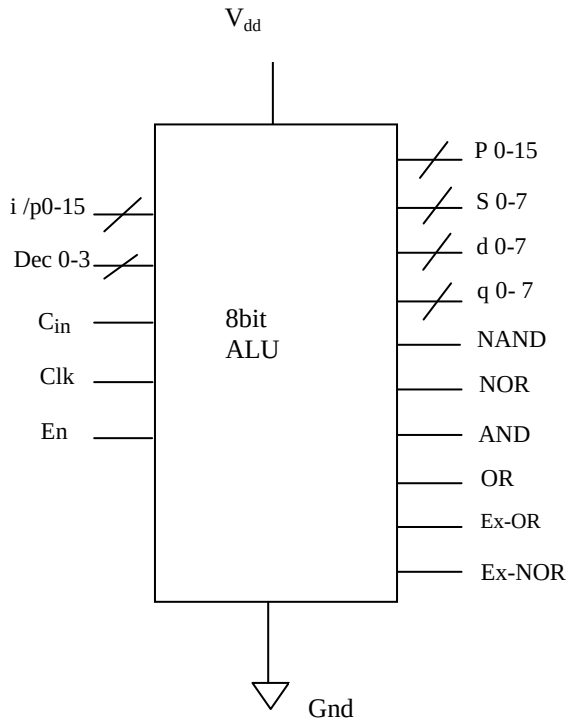


Fig 2:8bit-ALU

3. EXISTING TECHNIQUES:

3.1 GATED VDD

In this approach PMOS transistor is kept over the logic, which acts as gate way for power supply to the circuit [2]. Whenever the circuit is not in use this PMOS transistor will be kept off which in turn cuts off the power supply to the logical block.

The main reason behind the reduction in leakage current is stacking effect of self reverse-biasing series-connected transistors. Due to this leakage power reduces a lot. Fig3 shows the logic diagram for this approach.

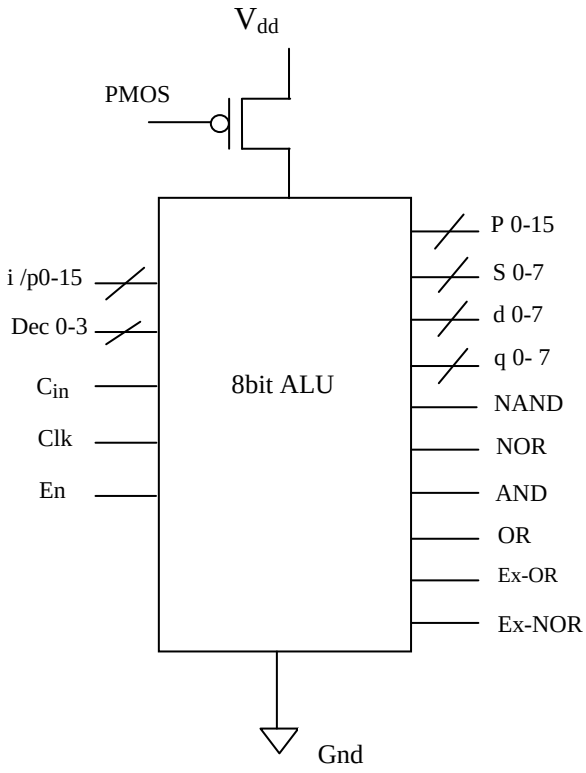
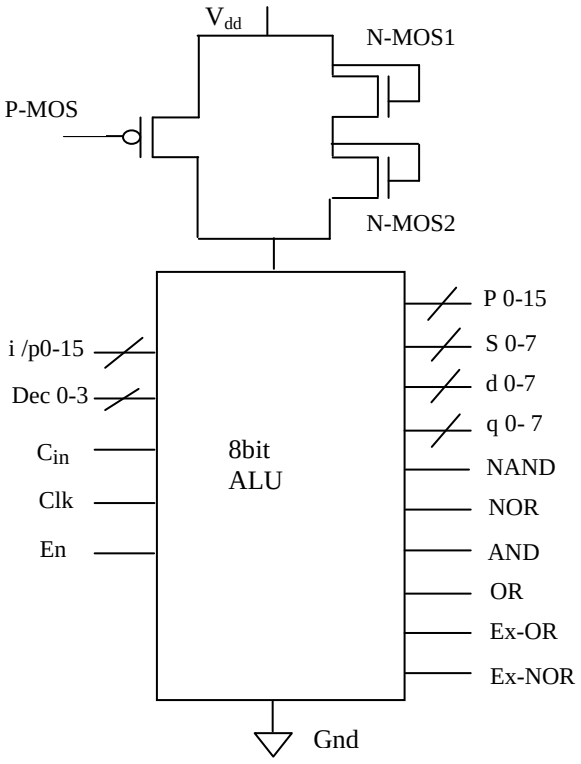


Fig 3.Gated Vdd

3.2 AVLS:

AVLS (Adaptive voltage scaling at supply) means that when he circuit is ON



. **Fig 4: AVLS**

The total power supply is applied to the logical circuits and a reduced power supply is applied to circuits when it is in static mode [3].This benefits in reduction of leakage power. Fig4 shows AVLS technique.

3.3 AVLG

The leakage power can be reduced by applying reduced power supply or by increasing the ground potential when the circuit is in off state. Here leakage power is reduced by adopting the second option i.e., increasing ground potential Fig.5 shows the respective logic.

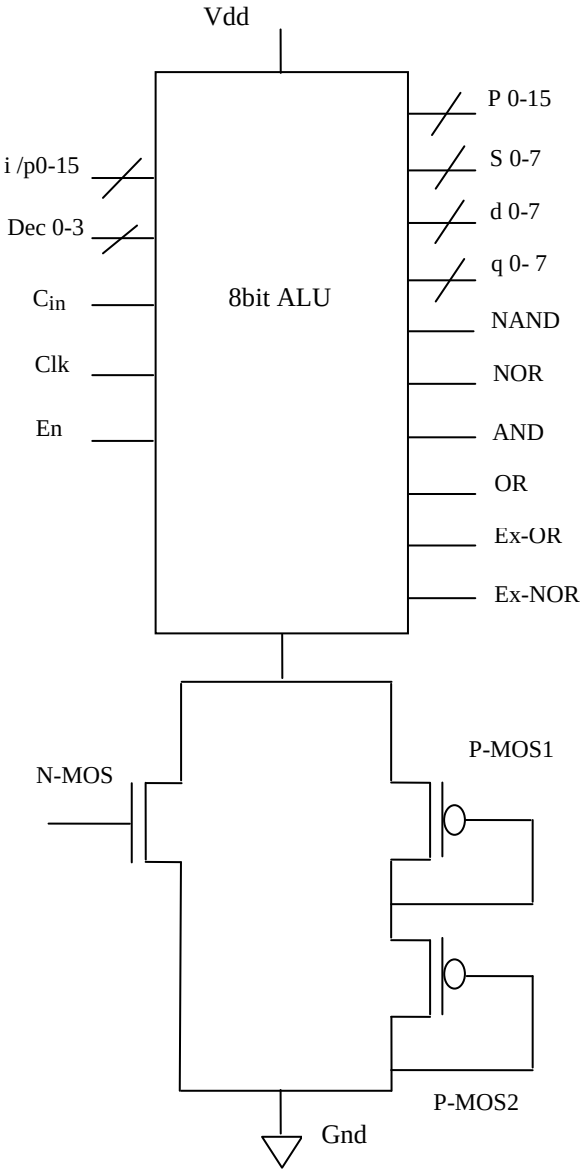


Fig 5: AVLG

3.4 AVL

This approach is the combination of both AVLS (Adaptive voltage level scaling at supply) i.e. reducing power supply to the circuit in static mode and AVLG (Adaptive voltage level scaling at ground) techniques i.e. increasing ground potential to circuit in inactive mode[3]. With reduced power supply & increased ground potential, the leakage power is reduced to a large extent. Fig6 shows the logic diagram for AVL technique.

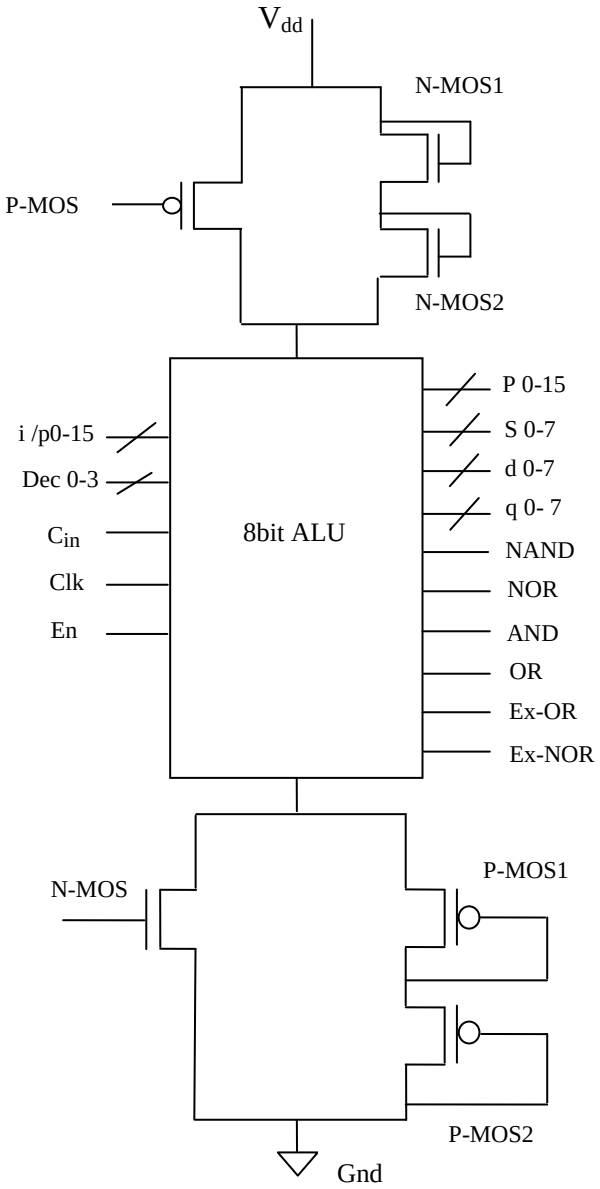


Fig 6: AVL

4. PROPOSED METHOD

Leakage power can be reduced by different ways like cutting off the power supply to the logic block or by reducing the power supply to the logical block in inactive mode. Delay overhead may occur due to cutting the power supply OFF for the logical block in static mode as it will take some amount of time to re-energize up to V_{dd} level while shifting from inactive to active mode. To compensate this delay overhead a reduced power supply as well as increased ground potential is applied to the logic block in this method. In this approach, whenever the circuit is to be ON the NMOS transistor will be kept ON. V_{dd} takes NMOS path as it is less resistive compared to that of two PMOS transistors PM1 & PM2. Ground is connected through PMOS3, which increases ground potential. This results in reduction in delay as transistor discharges to raised ground level instead of original level. In static mode NMOS and

PMOS3 were kept OFF. V_{dd} takes path of PMOS1&PMOS2 and ground takes path of PM0S4&PM0S5. This results in great reduction of leakage power. Fig7 shows logic diagram for the above method.

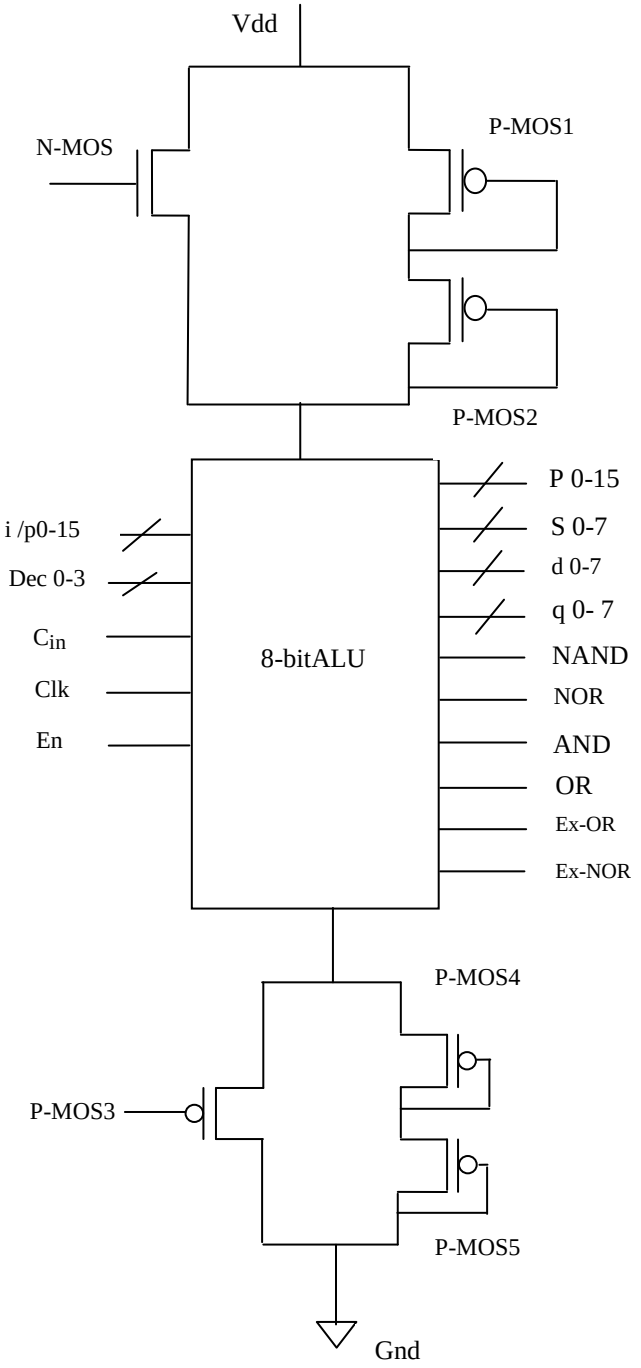


Fig 7: Logic diagram of proposed method

5. RESULTS AND ANALYSIS

Table1 shows average power, leakage power and delay of basic 8 bit ALU and different techniques applied on it. From results it is observed that there is a great reduction in leakage power. Though it is advantageous in terms of leakage power, there is average power and delay overhead. Proposed method has advantage in terms of average power, leakage power and delay compared with the existing techniques. The proposed method gives 46%, 76%, and 50% reduction in average power, leakage power and delay respectively.

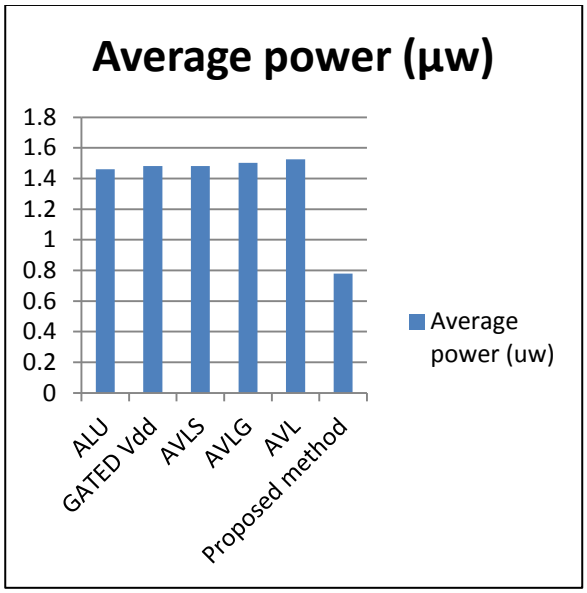


Fig 8: Bar chart for average power of 8bit-ALU for various techniques.

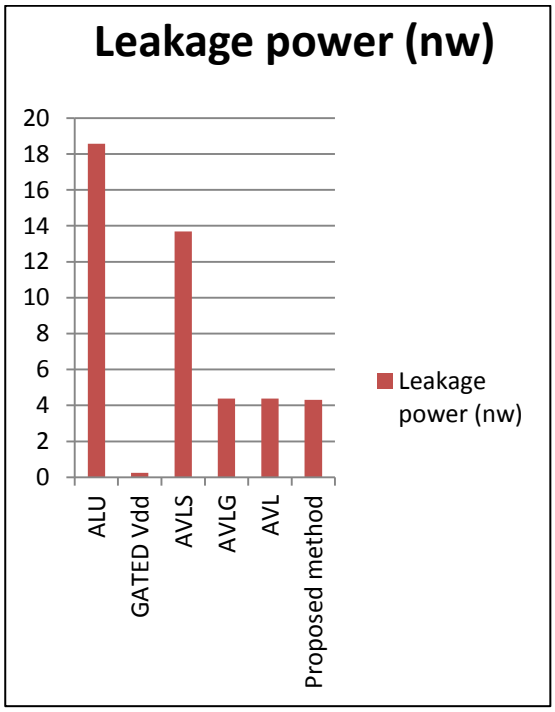


Fig 9: Bar chart for leakage power of 8bit-ALU for various techniques.

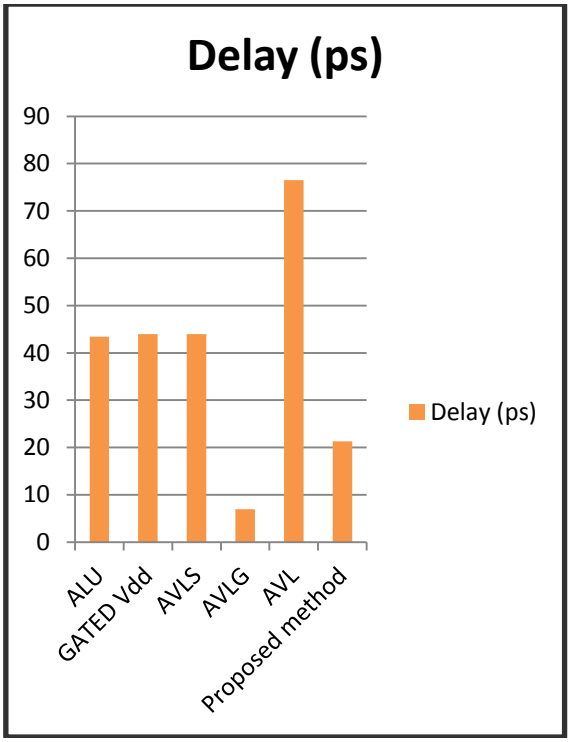


Fig 10: Bar chart for delay of 8bit-ALU for various techniques.

Table 1.power and delay values of 8bit-ALU

Method	Average power (µwatts)	Static power (nano watts)	Delay in (pico seconds)
Basic CMOS ALU	1.46099	18.56545	43.39799
Gated V_{dd}	1.48252	0.24574	43.96439
AVLS	1.48211	13.67854	43.96341
AVLG	1.50288	4.38585	6.94509
AVL	1.52446	4.38385	76.48786
PROPOSED METHOD	0.778604	4.30776	21.28299

6. CONCLUSION

In this paper 8bit ALU is designed. Different techniques like GATED VDD, AVLS, AVLG, AVL and proposed method are implemented on ALU. The proposed method gives 46%, 76%, and 50% reduction in average power, leakage power and delay respectively. It is concluded that proposed method is better than the existing in terms of power and delay. Table1 gives power and delay values of 8-bit ALU for different techniques.

7. ACKNOWLEDGMENTS

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