Area Efficient 1-Bit Comparator Design by using Hybridized Full Adder Module based on PTL and GDI Logic

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ABSTRACT
In this paper an area efficient 17T 1-bit hybrid comparator design has been presented by hybridizing PTL and GDI techniques. The proposed 1-bit comparator design consist of 9 NMOS and 8 PMOS. A PTL and GDI full adder module has been used which consume less area at 120 nm as compared with the previous full adder designs. The proposed Hybrid 1-bit comparator design is based on this area efficient 9T full adder module. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the used full adder module. Full adder modules outputs have been used for the generation of three different output of 1-bit comparator designs. The proposed 1-bit comparator has been designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm. Also the simulation of layout and parametric analysis has been done for the proposed 1-bit comparator design. Power and current variation with respect to the supply voltage has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed hybrid adder is 329.3μm^2 on 120nm technology. At 1.4V input supply voltage the proposed 1-bit hybrid comparator consume 0.367mW power at BSIM-4 and 0.411mW power at LEVEL-3 and 2.313mA current at BSIM-4 and 3.047mA current at LEVEL-3 model

Keywords
BSIM, CMOS, Gate Diffusion Input, NMOS, PMOS, Pass transistor logic, VLSI

1. INTRODUCTION
Comparator is a basic building block in the arithmetic unit of digital signal processors and application specific integrated circuits used in various digital electronic devices. In the world of technology the demand of portable devices are increasing day by day. Demand and popularity of these devices depends on the small silicon area, higher speed, longer battery life and reliability. The system performance can be affected by enhancing the performance of the comparator circuit used in these systems. Power and area consumption is a key limitation in many electronic devices such as mobile phone and portable computing systems etc. So far several logic styles have been developed to improve area and power consumption [1]-[4]. Several new logic styles have been developed that have better performance as compared to the traditional CMOS logic styles. The performance estimation of full adder is based on the design criteria for specific application. The main issues in performance estimation are Area Consumption, Power dissipation, Propagation delay and Power –Delay Product. Area, speed and power consumption are the main criteria of concern in CMOS Comparator design which often conflict with the design methodology and act as constrain on the design of comparator circuits. These performance criteria's should be individually investigated, analyzed for the various designs of the comparator by different logic styles.

Due to the growth of CMOS technology the VLSI industry has been driven toward the design of system on chip. Demand of the area efficient devices has been increased due to the explosive growth of VLSI industry. As Comparator is one of the basic circuitry used in arithmetic unit of various portable devices so area efficient comparator can help in the fulfillment of these demands. Due to this area efficient design of comparator has become essential for the researchers. Area of the circuit mainly depends on three things: Number of transistors in the circuit, Feature size of the transistor and Wiring complexity**.** No of transistors is of course the primary concern in the area efficient design because it affects the complexity of any circuit.

Power dissipation in any full adder circuit depends on two components: One is static dissipation which occurs due to the leakage current or other current drawn continuously from the power supply and second is dynamic dissipation which occurs due to switching of transient current, and charging and discharging of load capacitances. The static power dissipation is the product of the leakage current and supply voltage. The total static power dissipation P_s is given by

$$P_s = \sum_{1}^{n} \text{Leakage current} \times \text{Supply voltage} \quad (1)$$

Where n= no of devices and the leakage current is described by the equation

$$i_o = i_s(e^{qV/kT} - 1) \quad (2)$$

Where i_s is reverse saturation current, V is diode voltage, q is electronic charge, k is Boltzmann's constant and T is temperature.

The majority of the power dissipated in CMOS VLSI circuits is due to dynamic power. Thus for performance estimation of comparator only dynamic power is of interest. Average dissipated dynamic power is proportional to energy required to charge and discharge the circuit capacitance and switching frequency.

$$P_d = \frac{C_L V_{DD}^2}{t_p} \quad (3)$$

Total power dissipation is given by the sum of these three power dissipation i.e. static power dissipation, dynamic power dissipation and short circuit dissipation.

$$P_{total} = P_S + P_d + P_{sc} \quad (4)$$

The average propagation delay of the inverter is given by τ_P which is defined as the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \quad (5)$$

The propagation delay times τ_{PLH} and τ_{PHL} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output respectively. Power delay product is also defined as

$$PDP = 2P_{avg} \bullet \tau_P \quad (6)$$

Where the average switching is power dissipation at maximum operating frequency and τ_P is the average propagation delay. The factor 2 in above equation accounts for two transition of the output, from low to high and from high to low. Putting equation (3) in equation (6) PDP can be written as

$$PDP = 2(C_{load} \bullet V_{DD}^2 \bullet f_{\max})\tau_P \quad (7)$$

2. 1-BIT MAGNITUDE COMPARATOR

Digital Comparator "also called Magnitude Comparator" is a combinational circuit that compares two inputs binary quantities (A and B) and generates outputs to indicate whether the inputs are equal or which input is greater than the other, therefore, the circuit has three outputs to indicate whether A=B, A>B or A<B. At any given input quantities, only one output should be equal to logic '1'.

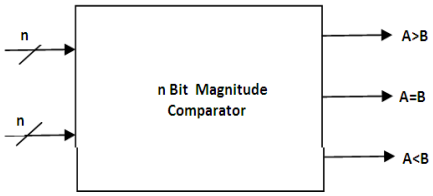


Fig. 1 Block Diagram of n-Bit Magnitude Comparator

Fig. 1 shows a block diagram of the magnitude comparator. The circuit, for comparing two n-Bit numbers, has 2n inputs & 22n entries in the truth table, for 2-Bit numbers, 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers 6-inputs & 64-rows in the truth table.

Table 1. Truth table of 1-bit Comparator

Inputs		Outputs		
B	A	G(A > B)	E(A = B)	L(A < B)
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

The truth table for the single bit comparator is shown in table 1.

From the truth table it can be observed that

$$E = \overline{A \oplus B}$$
$$L = \overline{A}B$$
$$G = A\overline{B}$$

Therefore, we can construct the logic circuit of the single-bit magnitude comparator as shown in Fig 2 where glowing LED shows high output.

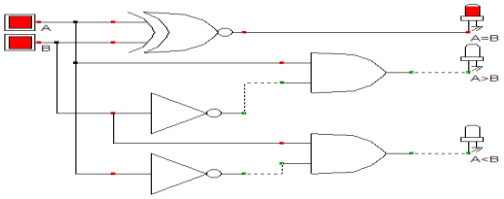


Fig. 2 Logic Diagram Of Single Bit Comparator

3. COMPARATOR DESIGNS

In the recent past various approaches of CMOS Comparator design by using various different logic styles has presented and unified into an integrated design methodology. Circuit area, speed and power consumption are the main criteria of concern in CMOS Comparator design which often conflict with the design methodology and act as a constrain on the design of comparator circuits. These performance criteria's are individually investigated, analyzed and their interaction to develop both quantitative and qualitative understanding of the various designs have been presented in literature**.**

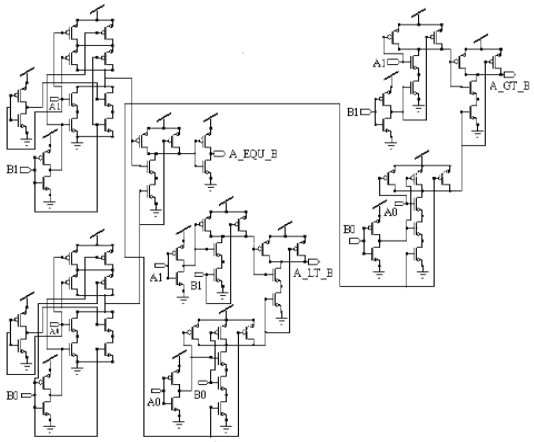


Fig 3: 2-Bit Comparator using CMOS logic style [5]

Different 2 bit Comparator designs by using different logic styles and their comparison have been presented in [5]. A CMOS and TG 2 bit comparator design provides full voltage swing between 0 and V_{DD}. But disadvantage of these designs is that they consume large power and area as compare to other designs. Also 2 bit comparator design by using pseudo NMOS logic style and by using pass transistor logic has been presented which consumes less area as compare to the two previous designs but does not provide full voltage swing at the output. Pass transistor logic consume less power and area as compared to other propose designs. But CMOS and TG show full voltage swing at the output as compare to the Pass transistor based comparator.

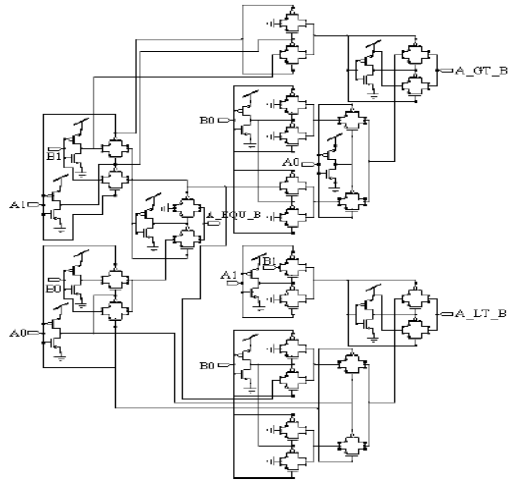


Fig 4: 2-Bit Comparator using Transmission Gate logic [5]

In recent years reversible logic has received great attention to reduce the power dissipation. A Novel low power comparator design using reversible logic has been presented in [6] which have ability to reduce the power dissipation. The proposed design full fills the requirement of less power consumption in various applications like ultra low power digital circuit and quantum computers.

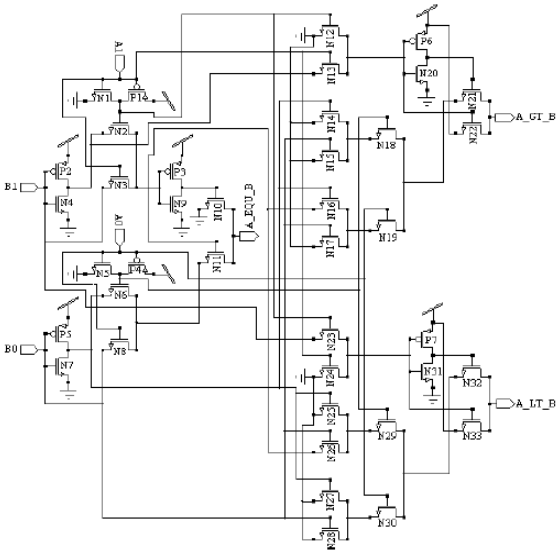


Fig 5: 2-Bit Comparator using Pass transistor logic style [5]

In recent years reversible logic has received great attention to reduce the power dissipation. A Novel low power comparator design using reversible logic has been presented in [6]-[8] which have ability to reduce the power dissipation. The proposed design full fills the requirement of less power consumption in various applications like ultra low power digital circuit and quantum computers.

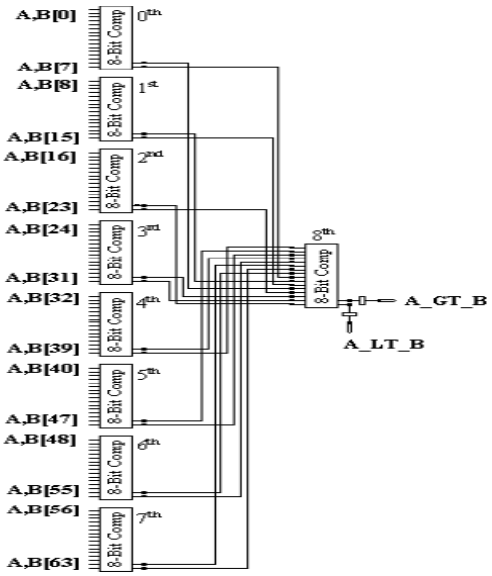


Fig 6: 64-Bit CMOS Binary Comparator [9]

A high speed 64 bit CMOS binary comparator has been proposed in [9] which have been implemented to improve the speed of the digital circuit. The proposed circuit shows better results as compared to the other existing designs in terms of speed. The proposed design maintains its superiority for high temperature. But disadvantage of this circuit is that the speed has been improved after sacrificing power consumption and area. The proposed design can be implemented for high speed circuits.

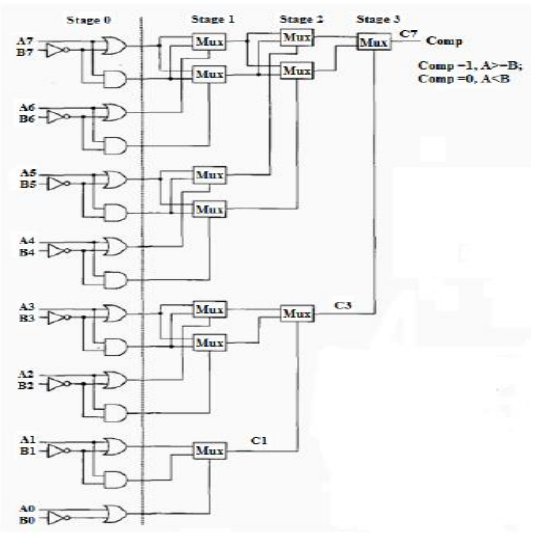


Fig 5: 8-Bit Comparator [10]

A hybridized low power 8 bit magnitude comparator has been proposed in [10] by hybridizing PTL and CMOS logic. The proposed design shows less power and area consumption as compared to other designs at different voltages. This hybrid comparator design shows less power consumption as compared to PTL and CMOS based comparator design. The proposed design also consumes less area as compared to other designs.

4. FULL ADDER DESIGNS

Full adder is a basic building block used in arithmetic unit of digital signal processors and ASIC's used in various digital electronic devices. There are various possible designs of full adder using different logic styles. Area consumption, speed and power consumption are the main criteria of concern in full adder design which often conflict with the design methodology and act as a constrain on the design of full adder circuits. These performance criteria's must be individually investigated and analyzed for the efficient performance of the digital circuits. The simultaneous generation of the sum and carry output are required in 1 bit comparator in which comparative outputs are obtained by using 1-bit full adder design. Various full adder designs have been presented in [11], [12], [11], [23]-[26].

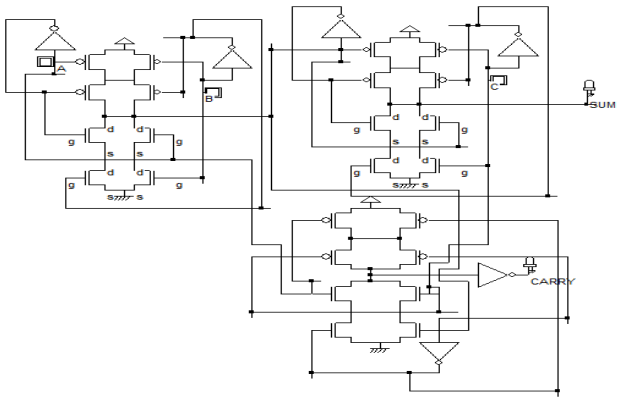


Fig 6: CMOS Full Adder Design By 2x1 Mux [11]

In Fig. 6 a 36T full adder design has been shown by using complementary CMOS design. This design has been implemented by using 12T complementary CMOS XOR and 12T 2x1 Mux design. In this design cascade operation of the XOR module has been done to implement the SUM output. Carry output has been generated by using 2x1 Mux for which the XOR output act as a select line. This design give the full voltage swing at the output by disadvantage is the large area consumption.

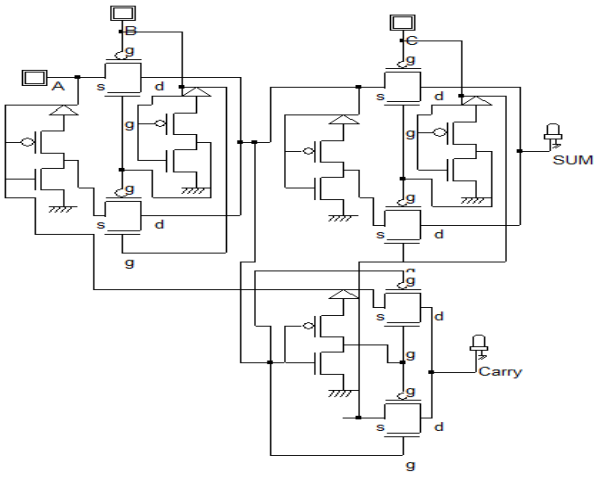


Fig 7: TG Full Adder Design by using 2xl MUX [12]

TG Full adder design by using 22 transistors has been shown in Fig 7 [12]. As transmission gate based full adder designs are low power designs and consume less transistors as compared to the complementary CMOS design. This paper presents an area and power efficient technique to design a full adder, using TG and multiplexer in order to reduce transistor count. Most of the conventional CMOS adders have been designed using 28 transistors which are very high and cause high power consumption. To overcome this existing problem, the TG full adder has been presented to improve the power and area simultaneously as compared to conventional CMOS.

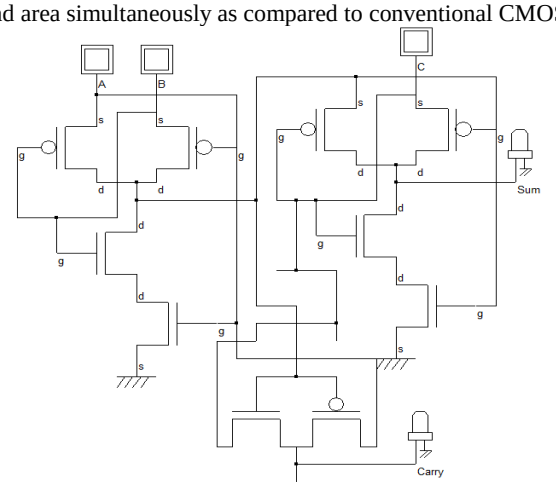


Fig 8: PTL Full Adder Design By 2x1 Mux [13]

If a logic style shows good performance in terms of one estimation criteria it can give degraded performance in other. The majority of the power dissipated in CMOS VLSI circuits is by dynamic power dissipation which is the power dissipated during charging or discharging of the load capacitance of a given circuit [13]-[15]. PTL based 10T full adder design by using 4T XOR and 2T Mux has been shown in Fig. 8 which consists less transistors as compared to CMOS and TG full adder designs. This design consumes less area as compared to CMOS and TG design but can't give full voltage swing at the output.

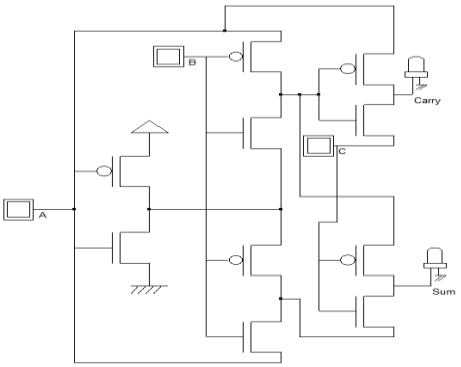


Fig 9: GDI Full Adder Design By 2x1 Mux [18]

In [16]-[20] full adder function has been achieved by using GDI technique shown in Fig.9. Circuit by using this technique uses 10 transistors to generate balanced SUM and Carry output. In this circuit simultaneously generation of XOR and XNOR output has been implemented which further acts as a input for the SUM and CARRY Module. Sum and Carry output has been obtained by using 2x1 MUX.

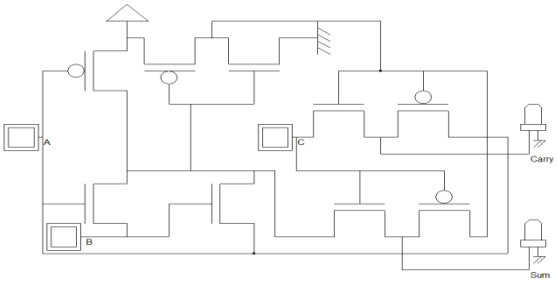


Fig 10: Hybrid Full Adder Design By 2x1 Mux [12]

In [12] a hybrid full adder has been implemented by using only 9 transistors shown in Fig.10. This full adder design consists five transistors in module 1and module 2and 3 has been implemented by using 2T GDI cell. Sum is obtained by using XOR-XNOR Module and 2x1 GDI Mux and an another 2x1 Mux is used for carry generation. Output of XOR-XNOR cell is used to drive the selection lines and control signal lines of the multiplexer. XOR-XNOR module has been designed by the PTL logic and consist only 5 transistors. So this design has been implemented by using only 9 transistors.

5. PROPOSED COMPARATOR SCHEMATIC

The design of proposed comparator consist Full Adder as a basic building block. To obtain the three comparative output inverted input at the B input terminal is given to the full adder design and C input is connected to the ground. Carry output directly act as A>B output of the one bit comparator. For the generation of A=B and B>A different input combinations for AND gate has been used. For generation of B>A input combination for the AND gate is B and A^1 and for the generation of A=B input combinations for AND gate are SUM and V_{DD}.

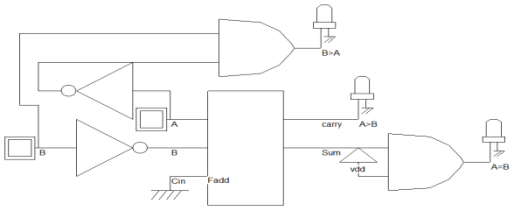


Fig 11: Logic Block Diagram of Proposed Full Adder

Proposed one bit comparator has been implemented by using only 17 transistors which consists hybrid full adder by using 9 transistors [12]. In full adder Sum is realized by XOR – XNOR module and GDI Mux and carry is realized XOR – XNOR module and GDI Mux by using different input combinations as compared Sum module. XOR-XNOR module has been implemented by 5 transistors. In Full Adder output of XOR-XNOR cell is used to drive the selection lines for Sum generation and control signal lines for Carry Generation. One bit Comparator has been designed by 9T full adder module shown in Fig.10. This full adder has been designed by hybridizing the PTL and GDI logic and consist only 9 transistors which is least as compared to all previous discussed full adder designs. Proposed one bit comparator design has been shown in Fig. 14.e.

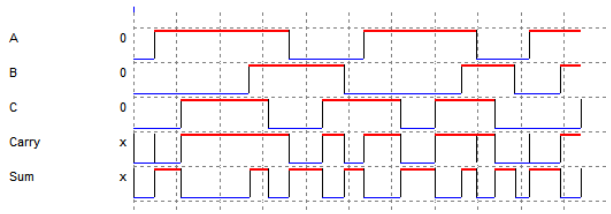


Fig 12: Timing Simulation of Hybrid Full adder

The full adder module has been compared with other discussed full adder in terms of area in microwind 3.1 designing tool. Microwind deals with both front end and back end designing of the VLSI circuits. In front end it has DSCH in which both transistor level and gate level designing can be done and also have ability to generate a verilog file which can be compiled by the microwind back end designing tool to get power and area consumption. Full adder module is compared with the other discussed full adder design in terms of area on 120nm technologies.

Table 2. Comparative Analysis of hybrid full adder Module in terms of area with other full adder design by different logics on 120nm technology

Full adder Modules	CMOS	TG	PTL	GDI	Hybrid
NMOS	18	11	5	5	5
PMOS	18	11	5	5	4
Area (μm^2)	577.4	408.2	179.6	190.5	156.8

Before the actual layout design of one bit comparator it necessary to validate the schematic of logic circuit. To overcome this problem DSCH and MICROWIND designing tools works parallel. Firstly the design is simulated in DSCH designing tools to know the exact functionality of the circuit and then implemented on the layout in microwind [21]. Timing simulation of proposed one bit comparator has been shown in Fig.13.In order to simulate the comparator design at logic level the design has been made in the DSCH tool and after launching the simulation the timing waveform can be obtained by chronogram icon. As shown in Fig. 13 the waveform the comparator output is according to required one bit comparator operation. Timing simulation shows the exact functionality of comparator for all three outputs.

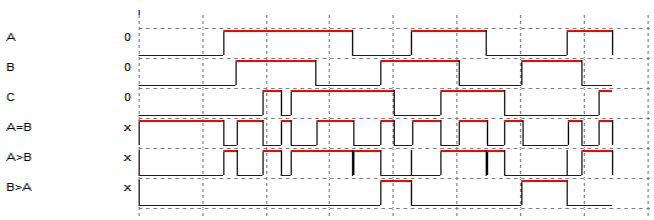


Fig 13: Timing Simulation of Hybrid one bit Comparator

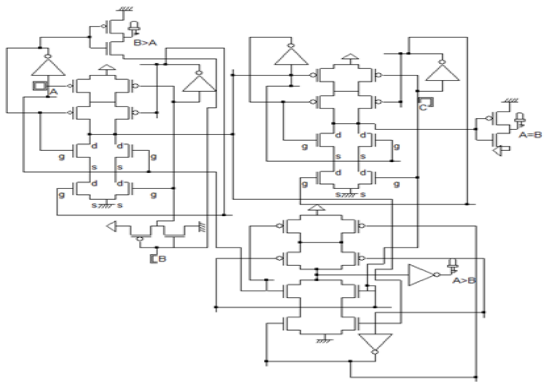


Fig 14.a: CMOS 1-Bit Comparator Design

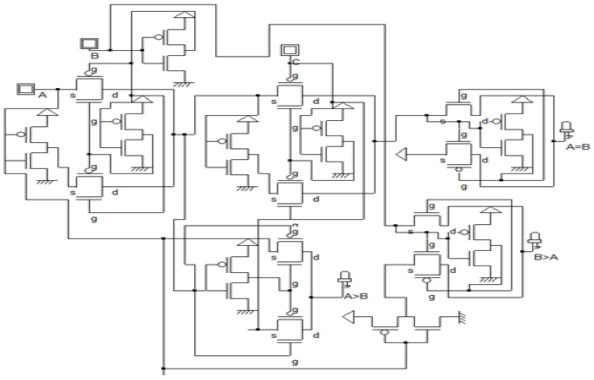
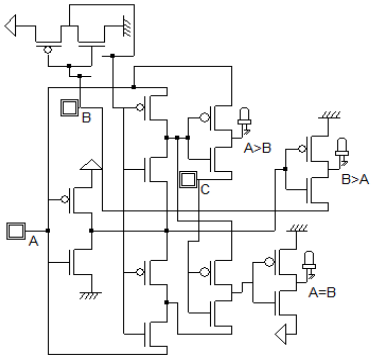
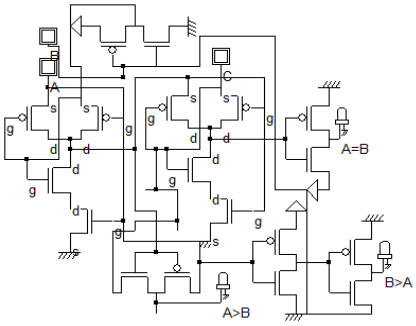


Fig 14.b: TG 1- Bit Comparator Design





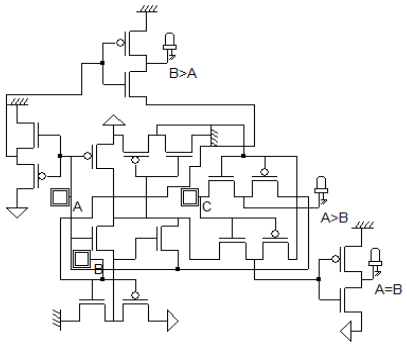


Fig 14.c: GDI 1- Bit Comparator Design Fig 14.d: PTL 1- Bit Comparator Design Fig 14.e: Hybrid 1- bit comparator Design

Fig 14: 1- Bit Comparator Design by using different logic

Different one Bit comparator designs has been proposed by using conventional CMOS, TG, GDI, PTL and hybrid logic styles as shown in Fig 14.a, 14.b,14.c, 14.d and 14.e respectively. One bit comparator by conventional CMOS consist 42 transistors, TG comparator consists 36 transistors, GDI comparator consists 16 transistors, PTL comparator consists 18 transistors and Hybrid comparator consists 17 transistors respectively as shown in Fig.14.

6. LAYOUT ANALYSIS

In complex VLSI design manual layout designing for a very complex circuit will become very difficult. So as compared to manual layout designing an automatic layout generation approach is preferred. In DSCH designing tool the schematic diagram has been firstly designed and validated at logic level. Although DSCH 3.1 have feature to analyze timing simulation as well as power consumption at logic level but accurate layout information is still missing. Verilog file is generated by the DSCH 3.1 tool which is compiled by the MICROWIND to construct the corresponding layout with exact desired design rules. Another way to create the design is by NMOS and PMOS devices using cell generator provided by the microwind 3.1. The advantage of this approach is to avoid any design rule error. Length and width can be adjusted by the MOS generator option on microwind tool.

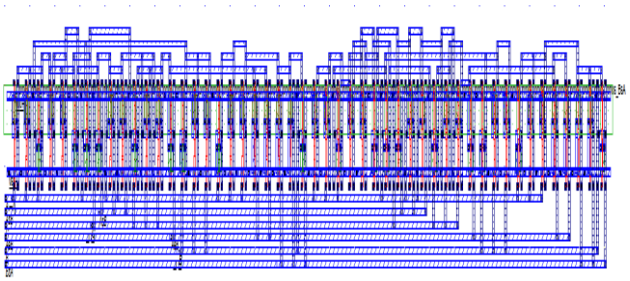


Fig 15: layout of proposed hybrid comparator 120nm

By default W=0.6µm (10 Lambda) and L=0.12µm (2 Lambda) in 120nm technology

7. SIMULATION RESULTS

The performance of proposed one bit comparator has been evaluated in terms of area and power on 120nm technology. Simulation has been performed using Microwind 3.1. Results are measured in terms of variation in power and current with respect to the variation in voltage.

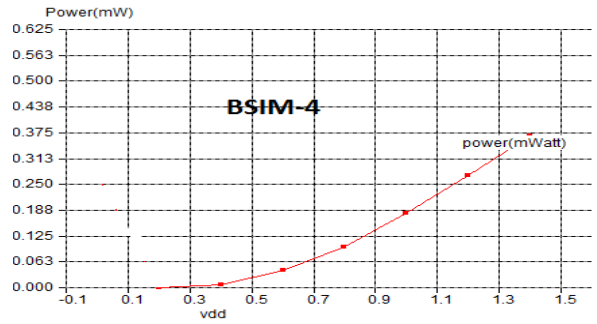


Fig 16: Power vs. Supply Voltage on BSIM-4

Simulation have been performed using the MOS Empherical model Level-3 and BSIM Model-4 at different power V_{dd}. Threshold voltage has been taken as 0.4V for both levels.

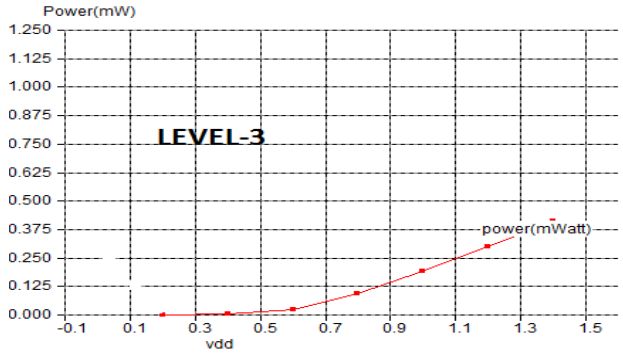


Fig 17: Power vs. Supply Voltage on LEVEL-3

All results have been performed using MOS Empherical model Level-3 and BSIM Model-4 in terms of power and current on voltage levels 0.6, 0.8, 1, 1.2 and 1.4V and operating temperature has been taken 27°C.

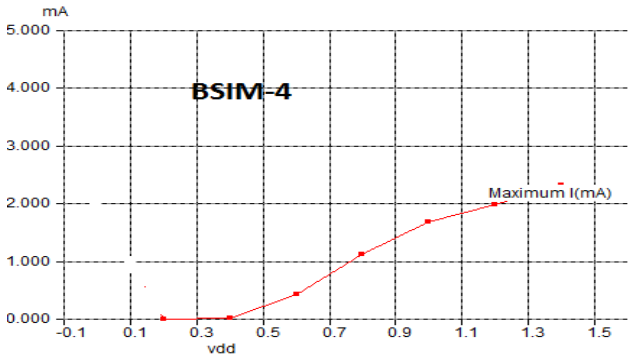


Fig 18: Current vs. Supply Voltage on BSIM-4

10 different curve fitting parameters has been used in MOS Empherical model Level-3 whereas BSIM Model-4 work with 19 different parameters Results plotted for change in power and current have been shown in Fig.16 and 18 for BSIM-4 and in Fig.17 and 19 for LEVEL-3 w.r.t supply voltage and results shows non linear dependence of the power with VDD.

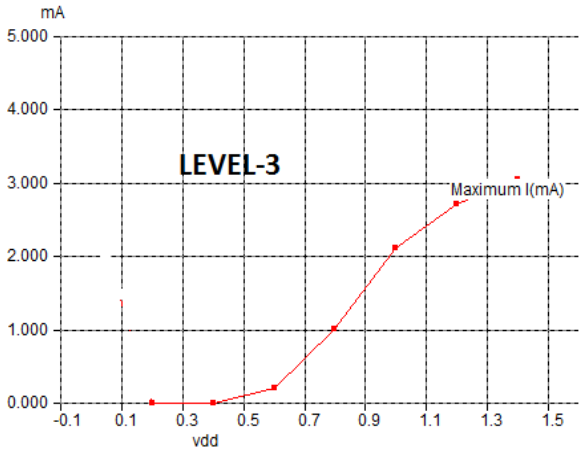


Fig 19: Current vs. Supply Voltage on LEVEL-3

Simulation results have been shown in table-2. From table it is clear that power dissipation increases with the power supply. Table also shows that the power and current dissipation is less at BSIM-4 as compared to LEVEL-3 at 1.4V input supply.

Table 3. Simulation results of 1-bit Comparator Design

Supply Voltage (V)	BSIM-4		LEVEL-3	
	Power (mW)	**Current (mA)**	**Power (mW)**	**Current (mA)**
0.6	0.042	0.463	0.025	0.206
0.8	0.099	1.119	0.095	1.010
1.0	0.179	1.688	0.194	2.112
1.2	0.271	1.993	0.299	2.716
1.4	0.367	2.313	0.411	3.047

Layout result will change on different technology i.e. if we use 120nm or 65nm for same circuit area consumption will be different. Finally the analog simulation has been obtained to know the power consumption at different voltage and temperature by using Microwind 3.1. Analog simulation is carried out for proposed 1-bit comparator on 120nm technology. For 120nm VDD is fixed to 1.2V and VSS to 0V. Simulation can be done by four ways in microwind 3.1.-Voltage vs. Time, Voltage and current vs. time, Voltage vs. Voltage and Frequency vs. Time. Voltage vs. Time simulation for proposed 1- bit comparator has been done on 120 nm.

Table 4. Comparison of Proposed 1-bit hybrid Comparator in terms of area consumption with other 1-bit comparator designs at 120nm Technology

Parameters	**CMOS**	**TG**	**PTL**	**GDI**	**HYBRID**
Area (μm^2)	1051.7 (μm^2)	716.6 (μm^2)	374.0 (μm^2)	350.7 (μm^2)	329.3 (μm^2)
NMOS	21	19	9	8	9
PMOS	21	17	9	8	8
Threshold Voltage (V)	0.4V	0.4V	0.4V	0.4V	0.4V
Operating Temperature (^{0}C)	27^0C	27^0C	27^0C	27^0C	27^0C
Supply Voltage (V)	1.4 (V)	1.4 (V)	1.4 (V)	1.4 (V)	1.4 (V)

Proposed 1-bit hybrid comparator has shown improvement in terms of area as compared to other 1- bit comparator designs. Results show that area consumed by the proposed hybrid adder is 329.3 (μm^2) on 120nm technology. At 1.4V input supply voltage the proposed 1-bit hybrid comparator consume 0.411mW power at LEVEL-3 and 0.367mW power at BSIM-4 and 2.313mA current at BSIM-4 and 3.047mA current at LEVEL-3 model.

8. CONCLUSION

An alternative 1-bit comparator design by hybridizing PTL and GDI approach has been introduced which consists only 17 transistors. Proposed 1-bit comparator has been implemented by using 9 NMOS and 8 PMOS transistors. Proposed 1 bit comparator has been designed using an area efficient Full adder module which has been implemented by using only 9 transistors. Full adder module has been also compared in terms of area from other existing Full adder modules and used full adder module has been proven area efficient as compared to other full adder designs. This area efficient module has been used as a basic module in proposed hybrid 1-bit comparator design. Area and simulation of proposed 1-bit comparator has been shown on 120nm. The simulation results have been shown on LEVEL-3 and BSIM-4 models. Area of proposed design is 329.3μm^2 on 120nm technology At 1.4V input supply voltage the proposed 1-bit hybrid comparator consume 0.411mW power at LEVEL-3 and 0.367mW power at BSIM-4 and 2.313mA current at BSIM-4 and 3.047mA current at LEVEL-3 model. The proposed 1-bit comparator circuit can work efficiently with minimum voltage supply of 0.4V and can work on wide range of frequency range between 2MHz to 400MHz. simulation results of 1-bit comparator shows that the power consumption and current is less at BSIM-4 as compared to LEVEL-3 model.

9. REFERENCES

[1] N. Weste and K. Eshraghian, (2002) Principles of CMOS VLSI Design: A System Perspective Reading, Pearson Education, Addison–Wesley.

[2] Sung-Mo Kang, Yusuf Leblebici, (2003) CMOS Digital Integrated Circuits: Analysis and Design, TATA Mc GRAW-HILL.

[3] Etienne Sicard, Sonia Delmas Bendhia, Basic of CMOS Cell Design, TATA Mc GRAW-HILL.

[4] Etienne Sicard, Sonia Delmas Bendhia, Advance of CMOS Cell Design, TATA Mc GRAW-HILL.

[5] Anjuli, Satyajit Anand, "2-Bit Magnitude Comparator Design Using Different Logic Styles," International Journal of Engineering Science Invention, Vol. 2, No. 1, pp. 13-24.

[6] A.N. Nagamani, H V Jayashree , H R Bhagyalakshmi, "Novel Low Power Comparator Design using Reversible Logic Gates," International Journal of Computer Science and Engineering,Vol.2, No. 4, pp. 566-574.

[7] H V Jayashree, A.N. Nagamani, H R Bhagyalakshmi, "Modified TOFFOLI GATE and its Applications in Designing Components of Reversible Arithmetic and Logic Unit," international journal of Advance Research in Computer Science and Software Engineering, Vol.2, No. 7, pp. 207-210.

[8] H G Rangaraju, Vinayak Hegde, K B Raja, "Design and Optimization of n-bit Reversible Binary Comparator," International Journal of Computer Applications, Vol. 55, No.18, pp. 22-30.

[9] Anjuli, Satyajit Anand, "High speed 64-Bit CMOS Binary Comparator," International Journal of Innovative Systems Design and Engineering, Vol. 4, No. 2, pp. 45-58.

[10] Geetanjali Sharma, Uma Nirmal, Yogesh Misra, "A Low Power 8-bit Magnitude Comparator with Small Transistor Count using Hybrid PTL/CMOS Logic," International Journal of Computational Engineering & Management, Vol. 12, No. 2, pp. 110-115.

[11] Anjali Sharma, Richa Singh, Rajesh Mehra, Member, IEEE, "Low Power TG Full Adder Design Using CMOS Nano Technology," IEEE International Conference on Parallel, Distributed and Grid Computing, pp. 210-213.

[12] Anjali Sharma, Rajesh Mehra, "Area and Power Efficient CMOS Adder Design by Hybridizing PTL and GDI Technique," International Journal of Computer Applications, Vol.66, No. 4, pp. 15-22.

[13] Chiou-Kou Tung; Yu-Cherng Hung; Shao-Hui Shieh; Guo-Shing Huang," A Low -Power High-speed Hybrid CMOS Full Adder For Embedded System," IEEE transactions on Design and Diagnostics of Electronic Circuits and Systems, vol.13, No.6, pp.-1 – 4, 2007.

[14] Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, "New Design Methodologies for High Speed Mixed Mode Full Adder Circuits," International Journal of VLSI and Communication Systems, Vol. 2, No. 2, pp.-78-98, 2011.

[15] Subodh Wairya, Rajendra Kumar Nagaria ,Sudarshan Tiwari, "Comparative Performance Analysis of XOR/XNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design ", International Journal Of VLSI Design & Communication System, pp.-221-242, 2012.

[16] Morgenshtein, A.; Fish, A.; Wagner, I.A., "Gate-diffusion input (GDI): A Power Efficient Method for Digital Combinational circuits," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol. 10 , No. 5 ,pp. 566 - 581 , 2002.

[17] Morgenshtein, A.; Fish, A.; Wagner, A, "Gate-diffusion input (GDI)-A novel power efficient method for digital circuits: A Design Methodology," IEEE International Conference, pp. 39 – 43,2001

[18] Po-Ming Lee; Chia-Hao Hsu; Yun-Hsiun Hung, " Novel 10-T full adders realized by GDI structure" Components, Circuits, Devices &Systems ,Engineered Materials, Dielectrics & Plasmas ,pp. 115 - 118 , 2007.

[19] Shahid Jaman, Nahian Chawdhury, Aasim Ullah, Muhammad Foyazur Raham, " A New High Speed-Low Power 12 Transistor Full Adder Design With GDI Technique," international Journal of Science & Engineering Research," Vol.3,No.7,2012.

[20] Pakkiraiah Chakali, K Sreeknath Yadav, Dilli Babu S, " A Noval Low Power Binary to Gray Code Converter Using Gate Diffusion Input (GDI), IOSR journal of engineering ,vol.2, No. 8, pp. 107-111,2012

[21] Microwind and DSCH version 3.1, User's Manual, Copyright 1997-2007, Microwind INSA France