A Novel Presentation of Toffoli Gate in Quantum-dot Cellular Automata (QCA)

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ABSTRACT
Quantum dot Cellular Automata (QCA) is one of the emerging nanotechnologies, promising alternative to CMOS technology due to faster speed, smaller size, lower power consumption, higher scale integration and higher switching frequency. The basic element in QCA is majority gate. This paper, present two different design layout of Toffoli gate based on QCA logic gates: majority voter gate (MV), QCA wire and inverter gate. QCADesigner, a common QCA layout design and verification tool is employed to verify and simulate the proposed Toffoli Gate (TG). The simulation result confirmed the correctness of the proposed circuits. The proposed circuit has a promising future in constructing of nano-scale low power exhausting information processing system and can stimulate higher digital applications in QCA.

General Terms
Nano Technology, Quantum dot Cellular Automata (QCA).

Keywords
QCA, Majority gate (MV), Toffoli Gate (TG), QCADesigner

1. INTRODUCTION
Now a day's, the use of Quantum technology is increased in various applications for its speed, size and power consumption [1, 2]. Quantum dot Cellular Automata is projected as a promising nanotechnology for future ICs [3, 4].

The basic element of QCA devices is the QCA cell shown in Figure 1(a). The basic structure in QCA is a cell that has four dots positioned at the corners of the squared cell and two mobile electrons. Depending on the position of the electrons, QCA cell has two type of polarization (p) [5-6]. A polarization of P=+1 (Binary 1) results if cells 1 and 3 occupied, while electrons on sites 2 and 4 result in P= -1 (Binary 0) as shown in Figure 1(b).

The cell polarization is defined [7] as Equation 1.

$$P=\frac{(\rho_2+\rho_4)-(\rho_1+\rho_3)}{(\rho_1+\rho_2+\rho_3+\rho_4)} \quad \ldots\ldots (1)$$

Where ρ_i denotes the electronic charge at dot i.

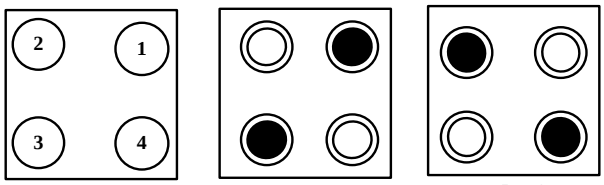


Fig 1: Basic Structure of QCA cell

2. QCA REVIEW
The fundamental unit of QCA-based design is wire, three input majority gate and inverter. QCA wire is an array of cells that are aligned one by one shown in Figure 2. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another [8].

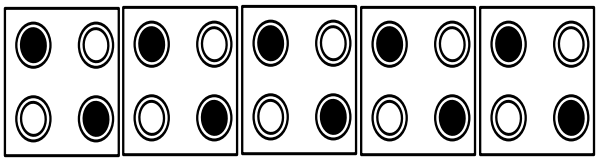


Fig 2: QCA wires

Three input Majority gate consists of five cells, three inputs, one output and a middle cell. The middle cell named device cell by reason of its function, switches to major polarization and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p = +1, respectively shown in figure 3. The Boolean expression of majority gate is as follows:

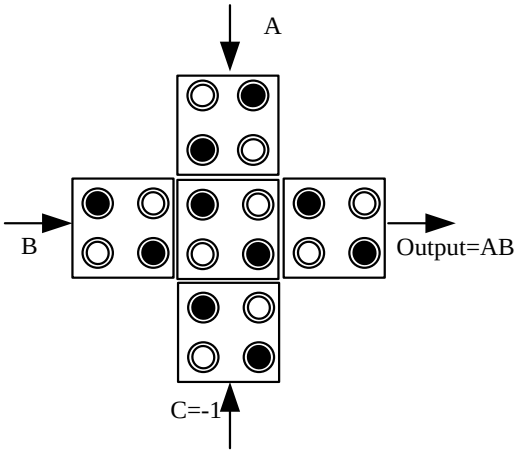
MV (A, B, C) = AB+AC+BC

To make AND gate, we need to set one of the MV input is zero, Equation (2) presents the AND gate equation.

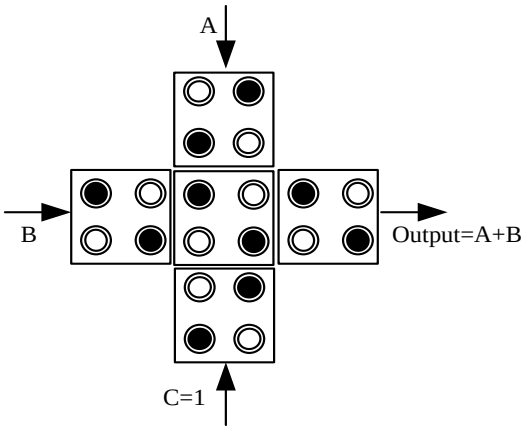
MV (A, B, 0) = AB+A.0+B.0= AB …… (2)

To make OR gate, we need to set one of the MV input is 1, Equation (3) presents the OR gate equation.

MV (A, B, 1) = AB+A.1+B.1= A+B …….. (3)



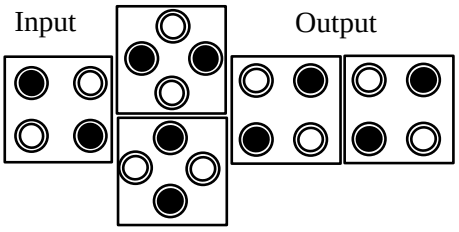
(a)



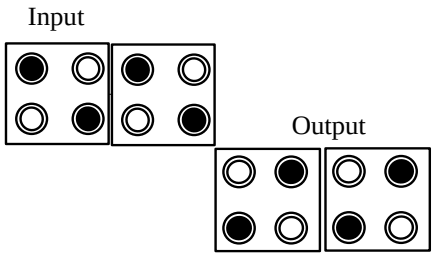
(b)

Fig 3: The QCA majority gate, function as (a) the AND gate and (b) the OR gate.

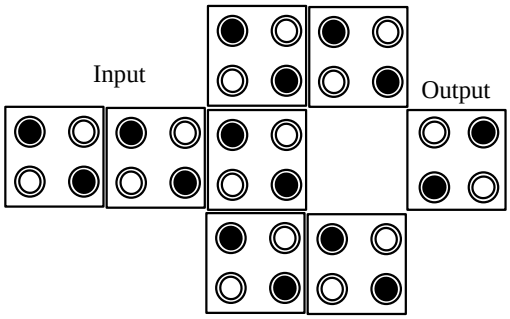
The inverting gate in QCA holds a different structure shown in Figure 4, since the last one operates properly in all various circuits. This inverter is made of eight cell or four QCA wires. The input polarization is split into two polarizations and in the end, two wires join and make the reverse polarization.



(a)



(b)



(c)

Fig 4: Three different structure of Inverter gates (a) (b) (c)

3. PROPOSED CIRCUIT AND PRESENTATION

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. In this paper we present one of the basic reversible logic gate "Toffoli Gate".

3.1 Toffoli Gate (TG)

Figure 5 shows a 3*3 Toffoli gate [9]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The outputs are defined by P=A, Q=B, R=AB⊕C. Table 1 represents the truth table of Toffoli gate and figure 6 shows the block diagram of Toffoli gate in QCA.

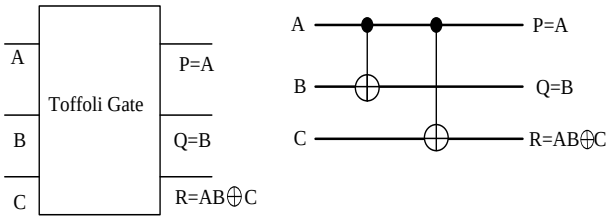


Fig 5: Toffoli Gate (TG)

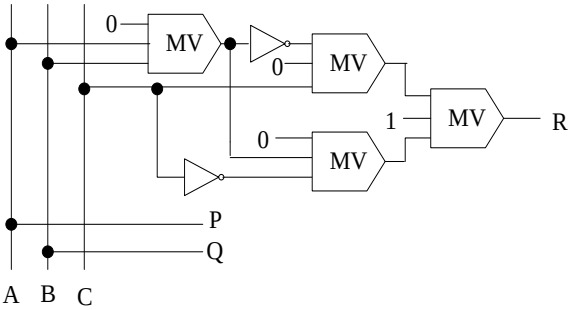


Fig 6: Block diagram of Toffoli gate in QCA

Table 1: Truth table of Toffoli gate

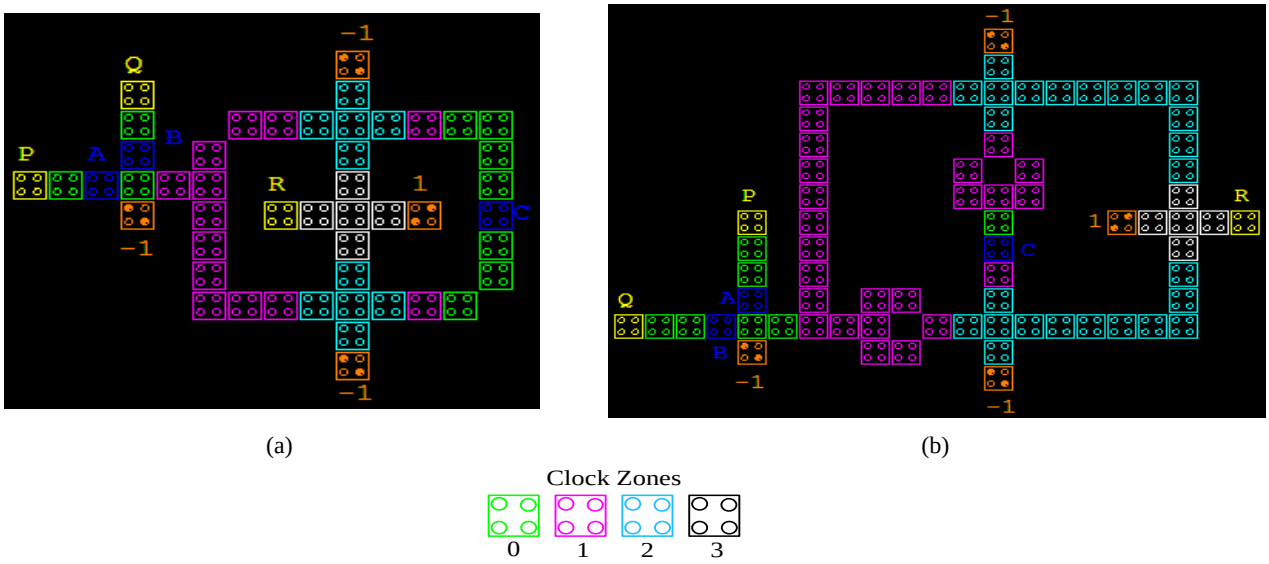
Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

4. SIMULATION AND RESULTS

The proposed circuit was functionally simulated using the QCADesigner [10]. The following parameters are used for a Bistable Approximation:

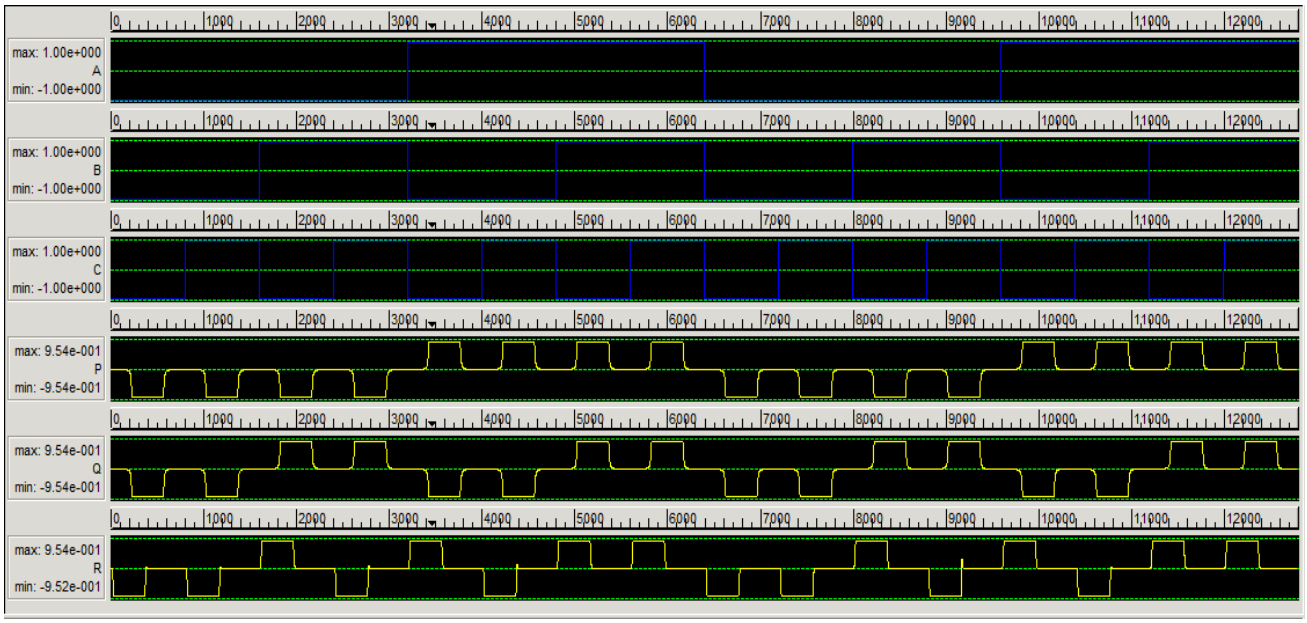
i. cell size=18nm,
ii. number of samples=50000,
iii. convergence tolerance=0.0000100,
iv. radius of effect=65.000000nm,
v. relative permittivity=12.900000,
vi. clock high=9.800000e–022 J,
vii. clock low=3.800000e–023J,
viii. clock shift=0,
ix. clock amplitude factor=2.000000,
x. layer separation=11.500000
xi. maximum iterations per sample=100.

Most of the above mentioned parameters are default values in QCADesigner. Figure 7 (a) and (b) shows the simulation of the circuit. In the Figure, the input signal are A, B, C and the output signal are P, Q and R, 7 (a) module goes through four clock zones also 7 (b) goes through four clock zones. The figure 8 (a) and (b) shows the input and output waveforms of proposed circuit.

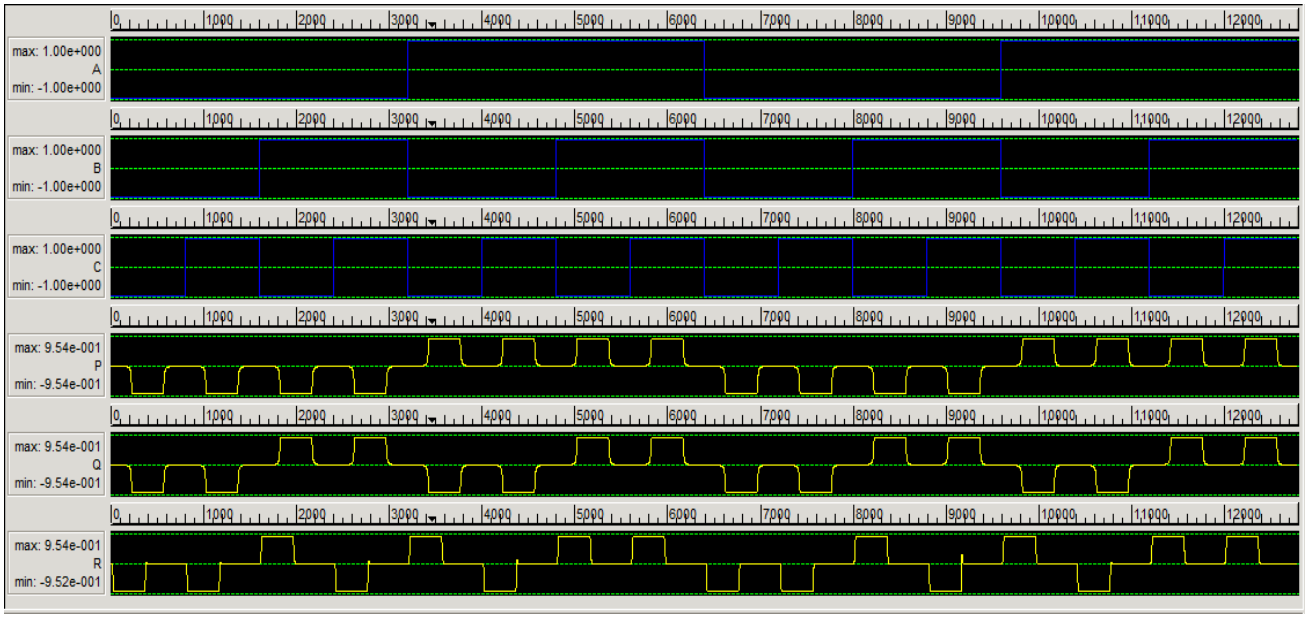


(a) (b)

Fig 7: Toffoli gate simulation (a) consist of 48 cell (b) consist of 75 cell



(a)



(b)

Figure 8: Simulation input output waveform (a) (b)

In Toffoli gate layout A, figure 4(b) inverter gate being used and this layout consist of 48 quantum cell, hence layout B used figure 4(c) inverted gate and need 75 quantum cell. Table 2 represents the performance comparison of two proposed layout of Toffoli gate.

Table 2: Performance comparison of two proposed layout

Parameter	Value	
	Layout A	Layout B
Number of cells	48	75
Covered area (μm^2)	0.067	0.136
Clock used	4	4

5. CONCLUSION

This paper presents a novel approach of designing Toffoli gate using quantum dot cellular automata. This proposed circuit has been simulated using QCADesigner and tested in terms of complexity (cell count) and area. The simulation result show that the proposed circuit performs well. The design is very useful for future computing techniques like ultra low power digital circuits and quantum computers.

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