A Novel Circuit Model of Small-Signal Amplifier using MOSFETs and BJT in Quadruple Darlington Configuration

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ABSTRACT
A novel circuit model of a small-signal narrow-band amplifier is proposed. The Proposed amplifier is designed using three MOSFETs and a BJT in quadruple Darlington configuration. The proposed circuit successfully amplifies small-signals of 1-10mV range and simultaneously provides high voltage gain and current gain with narrow bandwidth. In this way the proposed design achieved excellent results. Qualitative performance of the proposed amplifier is also compared with the circuit which is having BJT-MOSFET in Darlington pair configuration and with the circuit which is having BJT-MOSFETs in Darlington triple configuration. The proposed amplifier can be used to process audio range signal excursions and may be useful for those applications where high voltage and current gain would be the prime requirement of amplification in narrow-band low frequency region. The qualitative and tuning performance offer a flexible application to these amplifiers to be used as high voltage gain, high power gain and tuned amplifiers.
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General Terms
MOSFET – BJT - Voltage Gain – Current Gain -Bandwidth.

Keywords
Amplifier – Darlington – Frequency.

1. INTRODUCTION
The most important concept in electronics is the process of amplification through Darlington pair. It is considered to be a prominent configuration due to its wide range of application [1]-[5]. The flexible application-range of this vital configuration is extended from small-signal amplifiers to power amplifier circuits [1]-[5].In electronics, the Darlington transistor (often called a Darlington pair) is a compound structure. It consists of two bipolar transistors (either integrated or separated devices) connected in such a way that the current amplified by the first transistor is amplified further by the second one. This configuration has a much higher common emitter current gain than each transistor connected separately and, in the case of integrated devices, can take less space than two individual transistors because they can use a shared collector. Integrated Darlington pairs come packaged singly in transistor-like packages or as an array of devices (usually eight) in an integrated circuit. The Darlington configuration was invented by Bell Laboratories engineer Sidney Darlington in 1953. He used the idea of having two or three transistors on a single chip sharing a collector. However, a major drawback is associated with small-signal Darlington pair amplifier i.e. at higher frequencies its response becomes week than that of a single transistor amplifier [3]-[5]. Various attempts have been made to solve this problem by proposing different modifications in Darlington's composite unit as well as in respective amplifier circuits [6]-[10]. These attempts include the use of Field Effect Transistors in paired unit [11]-[13], experimentation with Triple Darlington's topology [5], [14]-[16] or the inclusion of some extra biasing resistances in respective circuits [3]-[4], [12], [15]-[16]. However, use of dissimilar active devices or hybrid combination of active devices in Darlington's topology (such as Darlington's unit with BJT and FET or BJT and MOSFET etc.) is still a field of electronic circuit designers to work with [11]-[13], [17].

2. BJT and MOSFET in PAIR DARLINGTON CONFIGURATION
Circuit-1 amplifier, Shown in figure 1, which is stated here as 'Reference Amplifier' [15], consists a compound unit of BJT and MOSFET in Darlington pair configuration. The circuit has a good benefit. This benefit comes from the fact that mosfet transistor has no gate current. This helps in avoiding the overloaded current which comes from the BJT transistor. This configuration has the advantages of high voltage and current gain.

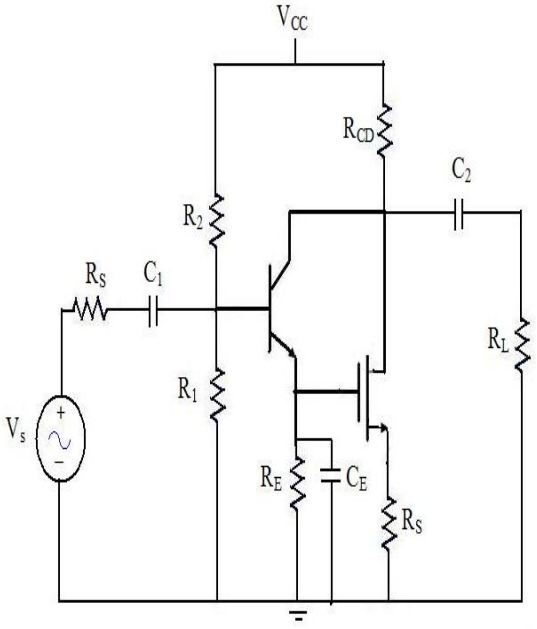

Fig. 1: Circuit -1 BJT and MOSFET in Darlington pair configuration

3. MOSFETs and BJT in TRIPLE DARLINGTON CONFIGURATION

The Circuit-2, shown in figure 2, is the same as that discussed in the previous session with addition of mosfet transistor. This circuit consists of two mosfets transistors and one BJT. Unlike reference amplifier, the drain point of M1 and collector point of Q1 in proposed amplifier are directly connected to the biasing supply V_{CC}. In addition, two additional biasing resistances R_{CD} and R_L are added in the given circuit with bypass capacitor across the source resistance [18]. The transistors are connected in the cascading way with BJT in the middle.

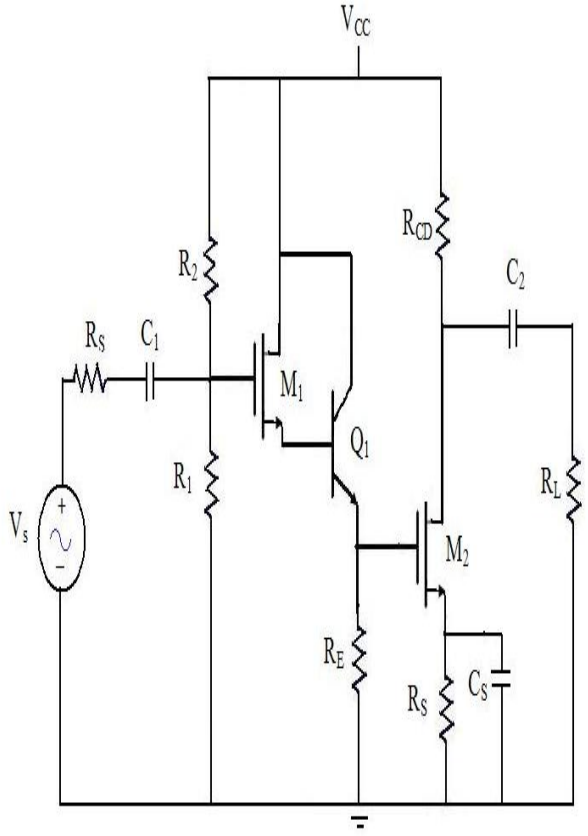

Fig. 2: Circuit-2 BJT and MOSFET in triple Darlington configuration

This topology looks very simple and achieves good results compared with the previous design.

4. THE PROPOSED CIRCUIT

The proposed circuit shown in figure 3 is based on the benefits of the previous of the two circuits discussed in sections 2 and 3.

Circuit of session 2 consists of a compound unit of BJT and MOSFET in Darlington pair configuration with an additional biasing resistance Rin the circuit. However, Circuit in session 3 consists of two identical MOSFETs and a BJT in triple Darlington configuration. Here the proposed design,shown in figure 3 introduces an additional MOSFET (M_3) connected to supply voltage Vcc through resistance R_{CD} and connected to the output resistance R_L through paypass capacitance C_s.

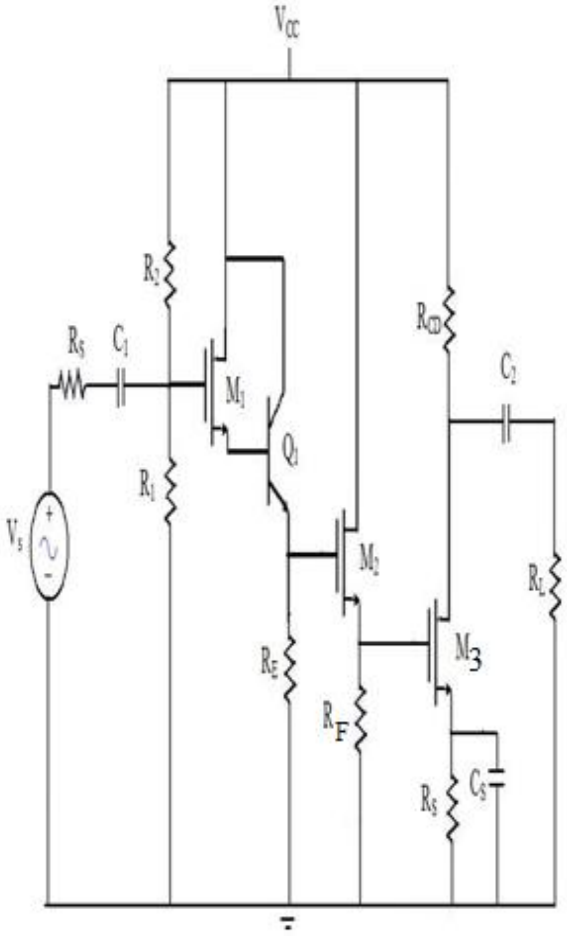

Fig.3: The Proposed Circuit

5. SMALL SIGNAL ANALYSIS OF THE PROPOSED CIRCUIT

Figure 4 shows the small signal of the proposed circuit. The voltage gain (A_{vg}) is derived from the following equations

$$\mathbf{A_{vg}} = \frac{\mathbf{v_{out}}}{\mathbf{v_{in}}} \qquad (\mathbf{1})$$

Where

$$V_{out} = -g_m v_{gs3} \times R_{CD}//R_L \qquad (2)$$

$$v_{in} = I_{in} \times R_s + V_{gs1} + v_{gs2} + v_{gs3} \qquad (3)$$

$$v_{gs2} + v_{gs3} = v_\pi + g_m \times (v_{gs1} + v_\pi) \times R_E \qquad (4)$$

$$v_{gs3} = g_m v_{gs2} \times R_F \qquad (5)$$

$$I_{in} \times (R_1//R_2) = v_{gs1} + v_{gs2} + v_{gs3} \qquad (6)$$

$$v_\pi = g_m(v_\pi + v_{gs1}) \times R_\pi \qquad (7)$$

From equation (4) through (7) and by substituting in equation (3) in term of v_{gs3} we get

$$\boldsymbol{v_{in}} = \left[\frac{(g_m \times R_F + 1)(1 - g_m \times R_\pi)}{g_m \times R_F \times (g_m^2 \times R_\pi \times R_E + g_m \times R_E)} + \frac{1}{g_m \times R_F} + 1\right] \times v_{gs3} \quad (8)$$

Using equation (2) and (8) we get

$$\frac{v_{out}}{v_{in}} = \frac{X}{Y} \quad (9)$$

Where

$$X = -g_m \times (R_{CD}//R_L) \quad (10)$$

$$Y = \left[\frac{(g_m \times R_F + 1) \times (1 - g_m \times R_\pi)}{(g_m \times R_F)(g_m^2 \times R_\pi \times R_E + g_m \times R_E)} + \frac{1}{g_m \times R_F} + 1\right] \quad (11)$$

The current gain (A_{IG}) is derived from the following equations

$$A_{IG} = \frac{I_{out}}{I_{in}} \quad (12)$$

Where

$$I_{in} = \frac{v_{in}}{(R_s + R_1//R_2)} \quad (13)$$

$$I_{out} - g_m \times v_{gs3} = \frac{v_{out}}{(R_{CD}//R_L)} \quad (14)$$

Also,

$$I_{in} = \frac{v_{in} - v_{gs1} - v_{gs2} - v_{gs3}}{R_s} \quad (15)$$

Relating

v_{gs1}, v_{gs2} *to* v_{gs3} *to get follwing equation*

$$I_{in} = \frac{v_{in}}{R_s} - \left[\frac{(g_m \times R_F + 1) \times (1 - g_m \times R_\pi)}{(g_m \times R_s \times R_F)(g_m^2 \times R_\pi \times R_E + g_m \times R_E)} + \frac{1}{g_m \times R_F \times R_s} + \frac{1}{R_s}\right] \times v_{gs3} \quad (16)$$

From equation (14) and by letting

$$\left[\frac{(g_m \times R_F + 1) \times (1 - g_m \times R_\pi)}{(g_m \times R_s \times R_F)(g_m^2 \times R_\pi \times R_E + g_m \times R_E)} + \frac{1}{g_m \times R_F \times R_s} + \frac{1}{R_s}\right] = Z \quad (17)$$

We get

$$I_{out} + \frac{(I_{in} \times R_s - v_{in})}{Z \times R_s} \times g_m = \frac{v_{out}}{R_{CD}//R_L} \quad (18)$$

Dividing equation (18) by I_{in}

$$\frac{I_{out}}{I_{in}} + \frac{g_m}{Z} - \frac{v_{in} \times g_m}{(I_{in} \times Z \times R_S)} = \frac{v_{out}}{(I_{in} \times (R_{CD}//R_L)} \quad (19)$$

Substitute from equation (13) in equation (19) we get

$$A_{IG} = \frac{I_{out}}{I_{in}} = \frac{(R_1//R_2)}{Z} \times g_m + A_{VG} \times \left(\frac{R_s + R_1//R_2}{R_{CD}//R_L}\right) \quad (20)$$

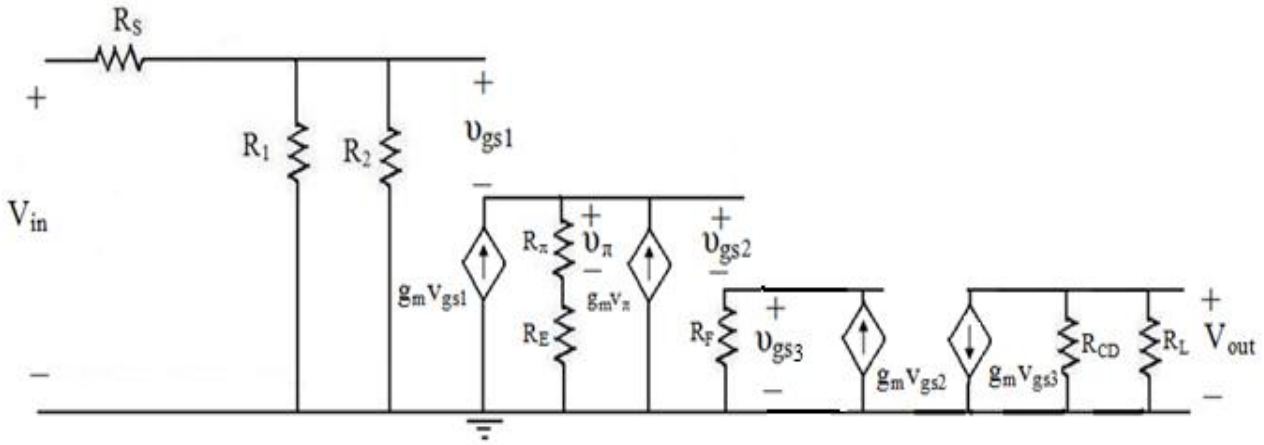

Fig.4 The small signal of the proposed circuit

6. SIMULATION RESULTS

The proposed circuit is simulated via Pspice tool, figure 5 illustrates the voltage gain versus frequency

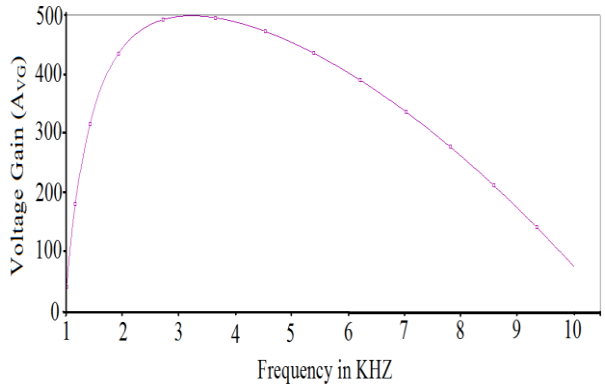

Fig. 5: The voltage gain of the proposed circuit versus frequency

Figure 6 shows the current gain of the circuit versus the frequency

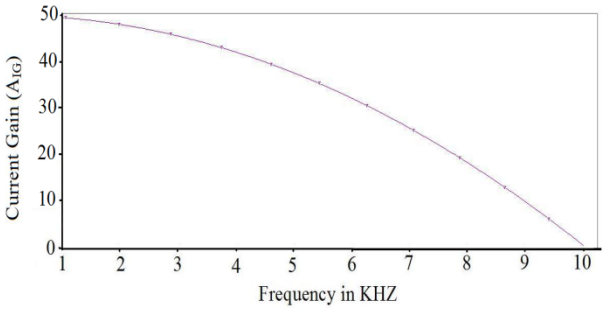

Fig. 6: The current gain of the proposed circuit versus frequency

Figure 5 shows that the maximum voltage gain reaches about 500 and figure 6 that the maximum current gain reaches about 50 which are a good result obtained from the proposed circuit .The amplifier of Circuit-1 [15] provides fair and distortion-less results for 1-10mV AC input signals whereas amplifier of Circuit-2[18] provides the same for 1-10mV. The reference amplifier of Circuit-1 [15] produces 115.522 maximum voltage gain AVG, 35.242 maximum current gain AIG and 12.258KHz bandwidth. Whereas the amplifier of Circuit-2[18] produces 212.593 maximum voltage gain VAG , 42.971 maximum current gain IAG and 9.665KHzbandwidth. Whereas the amplifier of the proposed Circuit produces 500.593 maximum voltage gain VAG, 48.258 maximum current gain IAG and 8.785KHzbandwidth. Clearly, the proposed amplifier produces higher voltage and current gain on the cost of reduced bandwidth.

7. COMPARISON OF THE RESULTS

Table 1 demonstrates the comparison of the different researches in darlington pair approaches to illustrate the benefits of the proposed work.

Table 1. Comparison between different approaches

	Maximum (A_{VG})	Maximum (A_{IG})	Bandwidth
This work	500.593	48.258	8.985KHZ
Circuit -1 [15]	115.522	35.242	12.285KHZ
Circuit -2 [18]	212.593	42.971	9.665KKHZ

8. CONCLUSIONS

A Darlington configuration is one of the most important designs in the field of communication. The proposed design uses the Darlington's topology with a new idea to serve the requirements of life. Through analysis and simulation of the proposed circuit, great results are obtained. The proposed amplifier can effectively process small-signals and is also free from the problem of poor response of small-signal Darlington pair or Triple amplifiers at higher frequencies. The proposed amplifier with narrow range bandwidth generates low harmonic distortion and simultaneously produces high voltage and current gains. Presence of additional biasing resistances in proposed amplifier is essential to maintain its high voltage and high current gain features. Collectively, these features make the proposed circuit one of the most important category for small-signal amplifiers based on Darlington's topology.

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