Comparative Analysis on Carrier Overlapping PWM Strategies for Seven Levels Symmetrical Inverter

K. Venkataramanan
Assistant Professor
Dept of EEE
Arunai Engg College
Tiruvannamalai,
Tamilnadu, India

B. Shanthi
Professor
CISL
Annamalai University
Annamalai Nagar
Tamilnadu, India

S. P. Natarajan
Professor & Head
Dept of EIE
Annamalai University
Annamalai Nagar
Tamilnadu, India

ABSTRACT
Multilevel Inverters have emerged in power conversion systems due to their lower output harmonics and high power capability. This paper presents the performance analysis of a new seven level symmetrical multilevel inverter with reduced number of switches using Carrier Overlapping PWM strategies. Due to switch combination redundancies, there are certain degrees of freedom to generate multilevel AC output. The results are compared with sine and Trapezoidal references in Carrier overlapping technique. Harmonic analysis and performance measures for various modulation indices have been carried out.

Keywords
COPWM, Sub harmonic PWM, CFD, Total Harmonic Distortion, and V_{RMS}

1. INTRODUCTION
A multilevel inverter is power electronic system which synthesizes expected output voltage from several levels of DC voltages. The advantages of multilevel inverter over conventional inverter are lower harmonic distortion, lower switching losses and high power quality. These inverters are suitable for renewable energy sources like solar, wind etc. The multilevel inverters are classified as Diode clamped, flying capacitor and cascaded H bridge inverters. When summarize all methods the number of main power switches required is 2(m-1) where 'm' stands for number of levels, in diode clamped and flying capacitor clamped needs passive components in addition to that main power switches. The main disadvantages of the above inverters are more number of switches, diodes and capacitors, so consequently they need complex firing circuits. To overcome these problems the number of switches reduced as much as possible. The new topology need one H bridge and (m-1)/2 switches to construct multilevel inverter. The multilevel inverters are operated in both fundamental switching frequency and high switching frequency. Power electronic inverters are very popular for industrial drives applications [1]. Total harmonic distortion and the RMS value of output voltage analyzed by multicarrier technique for Neutral point clamped inverter [2]. Donald Grahame Holmes et al [3] presented the harmonic cancellation by Carrier based PWM strategies. Lee et al [4] described the carrier based PWM method for voltage balancing of Flying Capacitor Multilevel Inverter. An analytical approach of the carrier based technique has been discussed in literature [5]. Improved carrier based space vector PWM is suitable for cascaded multilevel inverter topologies because it gives optimized switch utilization [6]. Phase Disposition and space vector modulation strategies have given similarity for diode clamped and cascaded inverters [7]. Ayob. S.M. and Salam.z investigated the multiple Trapezoidal modulating signals with single triangular carrier wave [8]. L.Ben-brahim and S.Tadakuma suggested the fluctuations presence in the output voltage can be reduced by redistributing the carrier waves [9]. Multicarrier PWM methods for a single phase five level cascaded inverter were investigated in literature [10]. S.Krishna describes the harmonic elimination based on selection of switching angles [11]. Shanthi and Natarajan proposed carrier overlapping strategy for FCMLI [12]. Rokan Ali Ahmed et al [13] introduced Multilevel Inverter with reduced switches has introduced for industrial applications. Nikhil Valsan. K and Joseph. K. D developed new multilevel inverter with reduced number of switches [14]. Nowadays many researchers shows interested in reduced switch concept. This paper investigates the various Carrier Overlapping PWM strategies on symmetrical multilevel inverter. Simulation is performed using MATLAB-SIMULINK.

2. SYMMETRICAL MULTILEVEL INVERTER
In conventional multilevel inverters 2(m-1) switches required to form 'm' levels. It is difficult to provide control circuit and firing circuit for more number of levels. To reduce the number of switches H Bridge should be modified. This new symmetrical multilevel inverter has One H Bridge inverter along with (m-1) / 2 power switches and three DC sources. Due to three equal voltage magnitude of DC source, it is called as Symmetrical multilevel inverter. This topology can be extended up to 'm' number of levels just adding single switch and source. The multilevel inverter operating modes are according to the polarity of load voltage and current. The advantages of symmetrical multilevel inverter are

- Number of switches decreased
- Lower Switching losses.
- Enhance good efficiency
- Cost and installation area reduced.

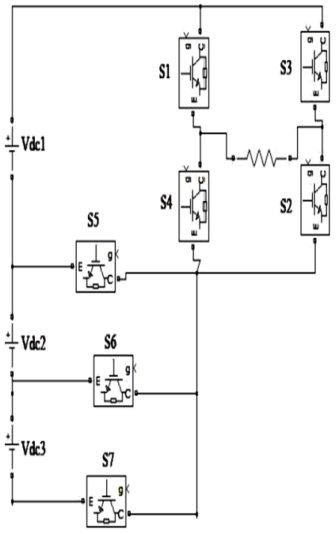

Fig.1 New Symmetrical Multilevel Inverter

The Power Stage Operation of the new inverter is as follows.

1. Output Voltage $3V_{dc}$: The switch S1, S2 and S7 is in ON condition.

2. Output Voltage $2V_{dc}$: The load should be connected through S1, S2 and S6.

3. Output voltage V_{dc}: The current path flow is S1, S2, Load and S5 thus we obtain V_{dc}.

In the negative half cycle ($-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$) the main switches S3 and S4 is in ON state instead of S1 and S2. The remaining switches operations are similar to the first three stages as mentioned above.

3. MODULATION STRATEGIES FOR MULTILEVEL INVERTER

A number of modulation strategies are used in multilevel inverters. They are generally classified as multistep, fundamental switching, space vector and carrier based PWM strategies

Fundamental Switching Strategies and Space vector PWM Strategies are very complicated for higher levels. So, carrier based switching strategy is preferred. In SHPWM all carriers are in phase.

This paper focuses on carrier based PWM techniques which have been extended for use in symmetrical seven level inverter. The amplitude modulation index is defined as

$$m_a = 2\ A_m / (m-3)A_c$$

Where A_m - Amplitude of reference

A_c - Amplitude of Carrier

Frequency ratio $m_f = f_c / f_m$

Where

f_c - Amplitude of carrier

f_m – Amplitude of reference

4. CARRIER OVERLAPPING PWM STRATEGIES

COPWM strategies which utilize the Control Freedom Degree of vertical offset among carriers. There are three methods COPWM-A, COPWM-B and COPWM-C. For an 'm' level inverter using carrier overlapping technique m-1 carrier with the same frequency f_c and peak to peak amplitude A_c are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is $A_c/2$. In this paper sine wave and Trapezoidal are used as references. The trapezoidal wave can be obtained from triangular wave by limiting its magnitude.

The vertical offset of six carriers are overlap other for symmetrical seven level inverter using COPWM-A shown in "Fig 2" and "Figure 5".

In COPWM-B strategy "Figure 3" and "Figure 6" shows the carriers are divided equally into two groups according to the positive / negative groups and they are opposite in phase with each other.

From the "Figure 4" and "Figure 8" the carriers invert their phase but in turn from the previous method, in COPWM-C strategy it was identified as PWM with amplitude overlapped and neighbouring phase interleaved carriers. Actually, pattern B and C can be looked as a second control freedom change besides offsets in vertical the carriers have horizontal phase shift from pattern A [12].

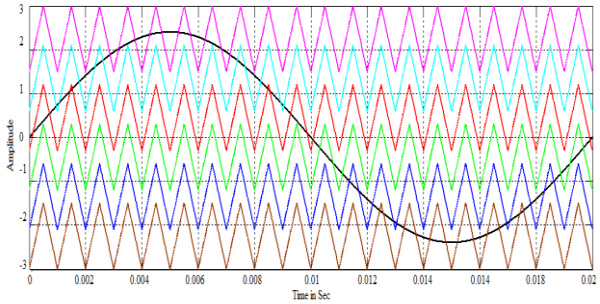

Fig 2: Carrier arrangement for COPWM-A strategy with sine reference (m_a = 0.8, m_f = 20)

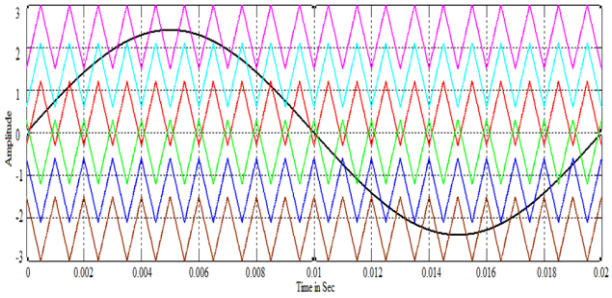

Fig 3: Carrier arrangement for COPWM-B strategy with sine reference (m_a = 0.8 , mf = 20)

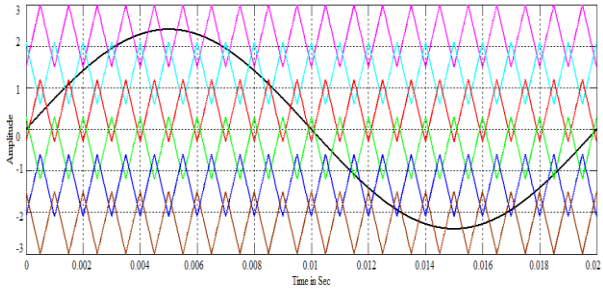

Fig 4: Carrier arrangement for COPWM-C strategy with sine reference (m_a = 0.8 , m_f = 20)

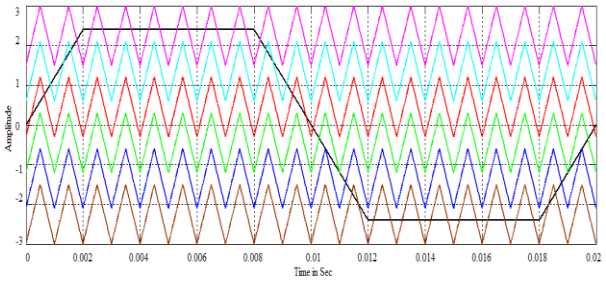

Fig.5. Carrier arrangement for COPWM-A strategy (m_a=0.8, m_f = 20) with trapezoidal reference

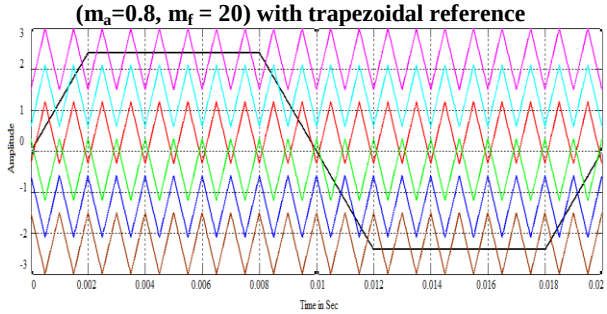

Fig.6. Carrier arrangement for COPWM-B strategy (m_a=0.8, m_f = 20) with trapezoidal reference

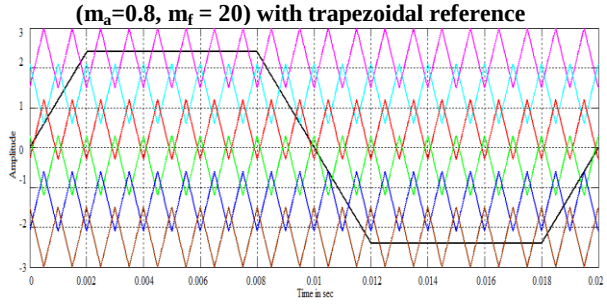

Fig.7. Carrier arrangement for COPWM-C strategy (m_a=0.8, m_f = 20) with trapezoidal reference

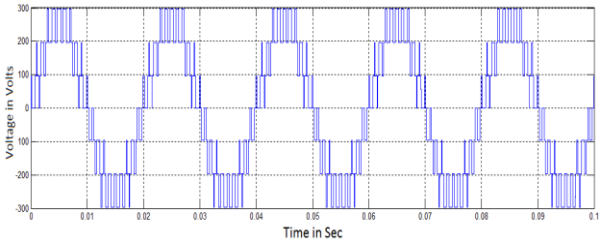

Fig 8 Output voltage generated by COPWM – A with sine reference

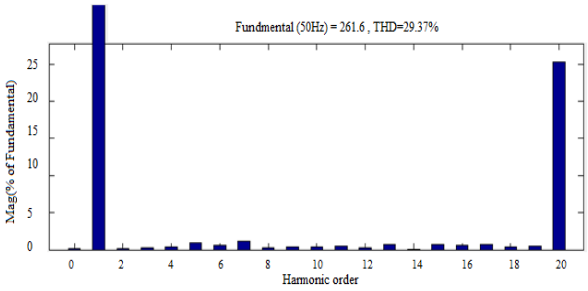

Fig 9 FFT plot for output voltage of COPWM - A with sine reference

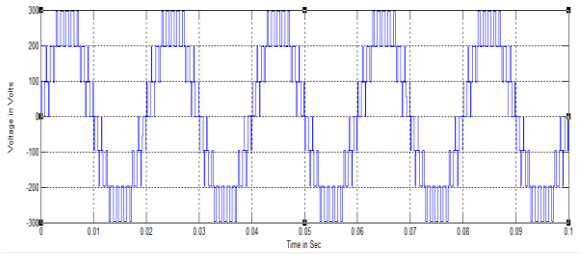

Fig 10 Output voltage generated by COPWM – B with sine reference

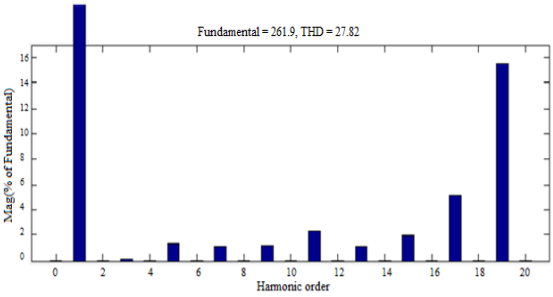

Fig 11 FFT plot for output voltage of COPWM - B with sine reference

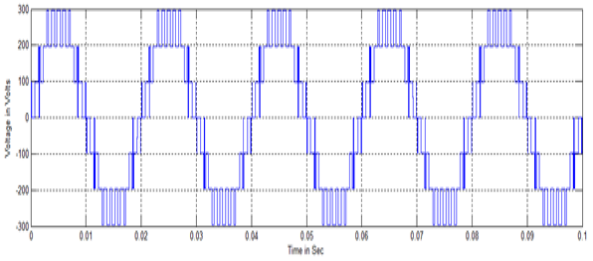

Fig 12 Output voltage generated by COPWM - C with sine reference

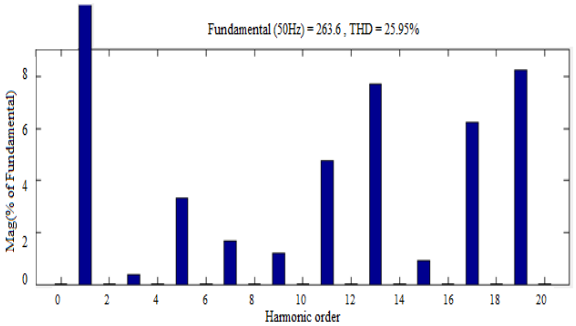

Fig 13 FFT plot for output voltage of COPWM - C with sine reference

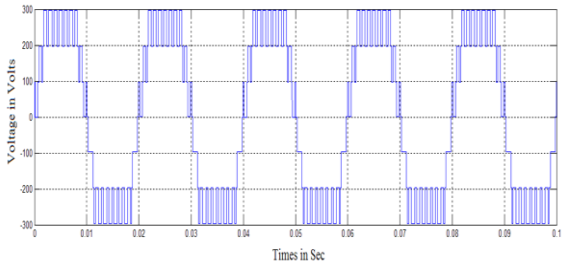

Fig 14 Output voltage generated by COPWM – A with Trapezoidal reference

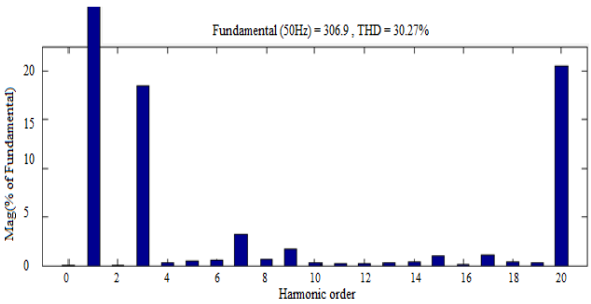

Fig 15 FFT plot for output voltage of COPWM – A with Trapezoidal reference

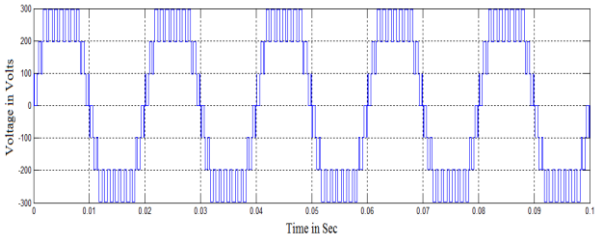

Fig 16 Output voltage generated by COPWM – B with Trapezoidal reference

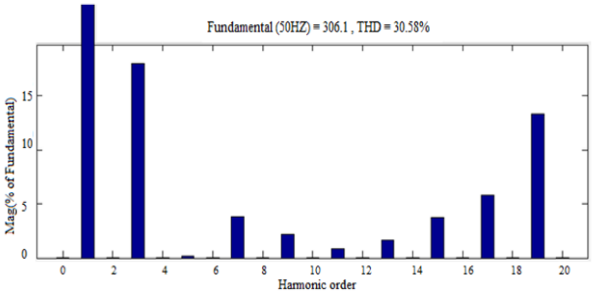

Fig 17 FFT plot for output voltage of COPWM – B with Trapezoidal reference

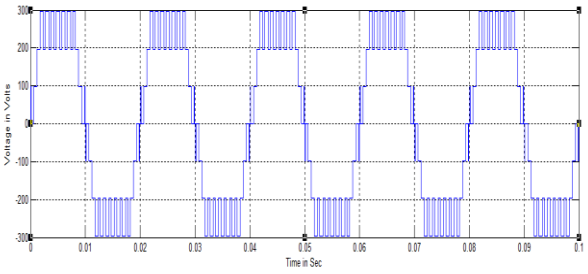

Fig 18 Output voltage generated by COPWM – C with Trapezoidal reference

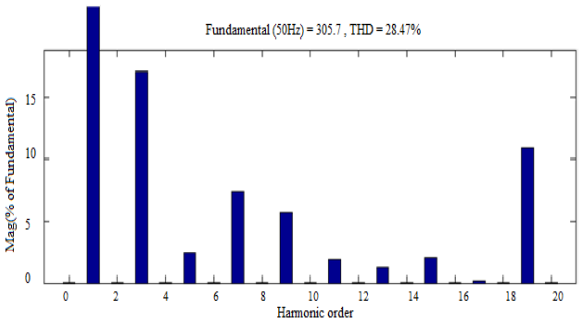

Fig 19 FFT plot for output voltage of COPWM – B with Trapezoidal reference

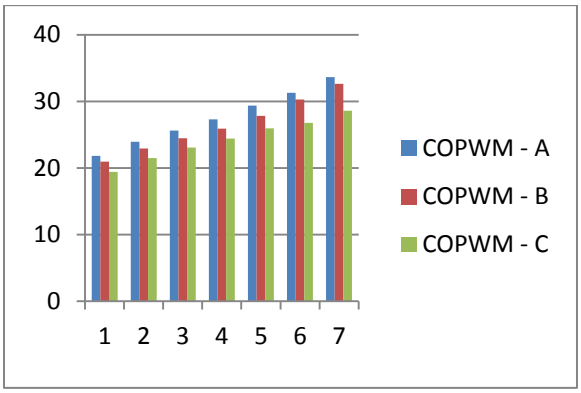

Fig 20: %THD Vs m_a for Sine Ref.

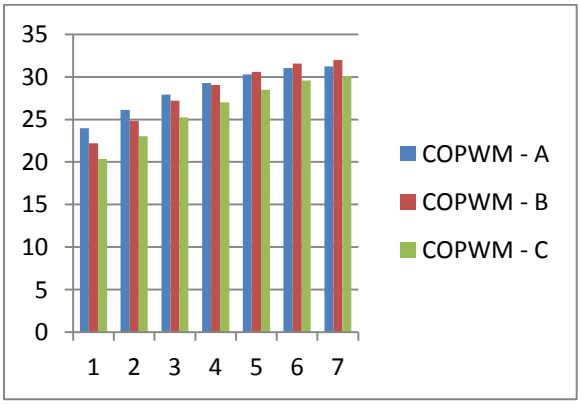

Fig 21: %THD Vs m_a for Trapezoidal Ref.

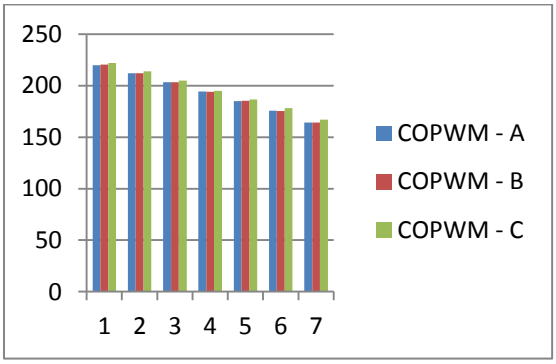

Fig 22: V_{RMS} Vs m_a for Sine reference

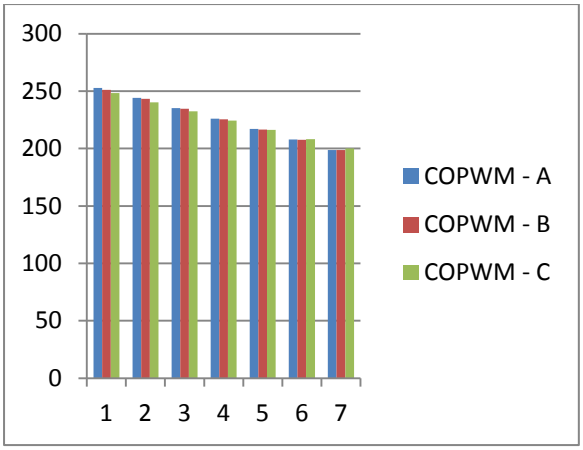

Fig 23:V_{RMS} Vs m_a for Trapezoidal reference

TABLE 1: % THD comparison for different modulation indices with Sine reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	21.81	20.97	19.43
0.95	23.94	22.94	21.46
0.9	25.60	24.44	23.05
0.85	27.30	25.92	24.41
0.8	29.37	27.82	25.95
0.75	31.28	30.26	26.74
0.7	33.61	32.61	28.57

TABLE 2: % THD comparison for different modulation indices with Trapezoidal reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	23.96	22.21	20.37
0.95	26.11	24.82	23.02
0.9	27.90	27.19	25.23
0.85	29.26	29.05	27
0.8	30.27	30.58	28.47
0.75	31.04	31.56	29.56
0.7	31.22	31.99	30.09

TABLE 3: % RMS comparison for different modulation indices with Sine reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	219.7	220.4	221.9
0.95	211.9	212.1	213.7
0.9	203.3	203.3	204.7
0.85	194.4	193.9	195
0.8	185	185.2	186.4
0.75	175.5	175.2	178.1
0.7	164.1	164	166.8

TABLE 4: % RMS comparison for different modulation indices with Trapezoidal reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	252.7	251.1	248.3
0.95	244	243.2	240.3
0.9	235.1	234.6	232.3
0.85	225.9	225.5	224.2
0.8	217	216.4	216.2
0.75	207.9	207.5	208.2
0.7	198.8	198.6	200

TABLE 5: Form Factor comparison for different modulation Indices with sine reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	457.7	INF	INF
0.95	662.18	INF	INF
0.9	924	INF	INF
0.85	925	INF	INF
0.8	925	INF	INF
0.75	1462.5	INF	INF
0.7	1823.3	INF	INF

TABLE 6: Form Factor comparison for different modulation indices with Trapezoidal reference

Ma	COPWM - A	COPWM - B	COPWM - C
1	**443.3**	**INF**	**INF**
0.95	**1016.67**	**INF**	**INF**
0.9	**2351**	**INF**	**INF**
0.85	**3765**	**INF**	**INF**
0.8	**2411.11**	**INF**	**INF**
0.75	**1039.5**	**INF**	**INF**
0.7	**1325.33**	**INF**	**INF**

5. SIMULATION RESULTS

The simulation results have been obtained by using MATLAB / SIMULINK. Simulations are performed for different values of m_a ranging from 0.7 to 1. "Figures 8 – 13" shows the simulated output voltage and FFT spectrum with sine reference for value of m_a = 0.8. It is seen that "Figure 9" COPWM – A with sine reference shows the 20^{th} harmonic energy is dominant. From "Figure 11" it is observed that COPWM – B with sine reference 11^{th}, 15th, 17th and 19^{th} harmonic energy are dominant. From "Figure 13" it is observed that COPWM – C with sine reference provides significant 5^{th}, 11th, 13^{th}, 17th and 19^{th} harmonic energy. In common 3^{rd} and 7^{th} harmonic energy are dominant in all the three cases when utilizing the trapezoidal as reference and apart from the above harmonic energy domination "Figure 15" COPWM – A with trapezoidal reference shows the 20^{th} harmonic energy dominant. From "Figure 17" COPWM – B with trapezoidal reference strategy has significant amount of harmonic energy present in 15^{th}, 17th and 19^{th} harmonics. From "Figure 19" it is observed that COPWM – C with trapezoidal reference strategy produces 9^{th} and 19^{th} harmonic energy. The following parameter values are used for simulation: Vdc = 100V, Resistive load = 100ohms.

6. CONCLUSION

The carrier overlapping technique has been investigated through single phase new symmetrical multilevel inverter. The performance parameters such as THD, V_{RMS} and Form factor has been analyzed and tabulated. The COPWM modulation strategy achieves lower harmonics when compared with conventional technique. From the simulation results we found that COPWM–C with sine wave as a reference creates lower harmonic reduction and COPWM–A with trapezoidal as a reference provides better DC utilization.

7. REFERENCES

[1] N. P. Schibli, T. Nguyen, and A. C. Rufer, "A three-phase multilevel converter for high-power induction motors," IEEE Trans. Power. Electron.,vol. 13, no. 5, pp. 978–986, Sep. 1998.

[2] M.Leon Tolbert, G.Thomas. Habetler, "Novel Multilevel Inverter Carrier-Based PWM Method", IEEE Transactions on Industry Applications, Vol. 35, No. 5, September/October 1999.

[3]Donald Grahame Holmes, P.Brendam and Mcgrath,"Opportunities for Harmonic Cancellation with Carrier-Based PWM for Two-Level and Multilevel Cascaded Inverters", IEEE Trans. on Industry Applications, 2001,37(2), 574-582.

[4] S.G.Lee,F.W.Kang,Y.H.Lee and D.S.Hyun: The carrier based PWM method for voltage balancing of flying capacitor Multilevel Inverter,IEEE Power Electronics Spec.Conf. Record.,Vol 1,2001, 126-131

[5] Brendan Peter McGrath, Donald Grahame Holmes, "An Analytical Technique for the Determination of Spectral Components of Multilevel Carrier-Based PWM Methods", IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002.

[6] Dae-Wook Kang, Yo-Han Lee, Bum-Seok Suh, Chang-Ho Choi and Dong-Seok Hyun, An Improved Carrier-Based SVPWM Method Using Leg Voltage Redundancies in Generalized Cascaded Multilevel Inverter Topology. IEEE Transactions on Power Electronics, Vol. 18, No. 1, January 2003

[7] Brendan Peter McGrath, Donald Grahame Holmes and Thomas Lipo,"Optimized Space Vector Switching Sequences for Multilevel Inverters IEEE Transactions on Power Electronics, Vol. 18, No. 6, November 2003.

[8] Ayob,S.M.; and Salam.z. A new PWM scheme for cascaded multilevel inverter using trapezoidal modulation signals. Research report of university teknologi Malaysia, 2004, 242-246,.

[9] L.Ben-brahim and S.Tadakuma, Novel Multilevel Carrier Based PWM Control Method for GTO Inverter in Low Index Modulation Region IEEE Transactions on Power Electronics, Vol. 18, No. 1, January 2006 42(1), 121-127.

[10] Al-Judi, A.; Nowicki, E.; and Bierk, H. (2007). Voltage switching scheme for harmonic reduction in multilevel inverters. Canadian Conference on Electrical and Computer Engineering, 2007. CCECE 2007, Rec.: 0840-7789/07, 709-712.

[11] S. Krishna, "Harmonic Elimination by Selection of Switching Angle and DC Voltages in Cascaded Multilevel Inverters", in proc. 15th National power system conference (NPSC), 2008, pp 119-124.

[12] B. Shanthi, S.P.Natarajan, "Carrier Overlapping PWM Methods for Single Phase Cascaded Five Level Inverter", International Journal of Science and Technology of Automatic Control & Computer Engineering (IJ-STA, Tunisia). Special issue on Control of Electrical Machines, 2008, 590-601.

[13] Rokan Ali Ahmed, S.Mekhilef, Hew Wooi Ping, "New Multilevel Inverter Topology with Reduced Number of Switches", Proceedings of the 14th Inter. Middle East Power Systems Conf. (MEPCON'10), Dec 19-21, 2010 pp 565-570.

[14] Nikhil Valsan. K and Joseph. K. D "A Reduced Switch Multilevel Inverter for Harmonic Reduction." 2012 Asia-Pacific Power and Energy Engineering Conference, (2012): 1-4