A Novel High Performance Dual Threshold Voltage Domino Logic Employing Stacked Transistors

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ABSTRACT
Among the assorted logic styles used in fostering the integrated circuits, the domino logic styles offers higher speed and smaller transistor count as compared to the static cmos circuits. However the domino logic suffers from lower noise immunity and higher power dissipation due to the problem of charge sharing and sub-threshold leakage currents. In this paper some of the earlier proposed techniques to reduce the power consumption of the domino circuits like Dual threshold voltage (DTV) and Dual threshold voltage–voltage scaling(DTVS) have been analyzed. A novel stacked transistors Dual threshold voltage (ST-DTV) approach which deploys DTV technique with stacked transistors together with a voltage regulated static keeper is analyzed to abate the total power dissipation of the circuit together with a better Power delay product (PDP). The ST-DTV design is tested on a 3-input OR gate and a 4x1 multiplexer at 90nm technology on multiple voltages and frequencies. Tanner tool EDA v13.0 is used for simulation.

General Terms
Power Consumption, Power Delay Product.

Keywords
Domino logic, dual threshold voltage, voltage Scaling.

1. INTRODUCTION
The high performance microprocessors employs domino logic circuit because of its higher speed of operation. The domino logic involves the implementation of only the nMOS logic as compared to the static cmos circuits which involves the implementation of both the nMOS and pMOS logic due to which there is colossal amount of reduction in the number of transistors in domino logic thus reducing the area of the circuit. The rudimentary domino circuit is shown in Fig.1. In the above figure CL represents the parasitic capacitance and PDN represents the pull down network which realizes the logic function to be implemented. When the clock is low the circuit is in precharge phase and Qp is on and Qe is off [1]-[2]. The dynamic node precharges to Vdd and the output of the cmos inverter is low. When clk =1 the circuit is in evaluation phase, Qe is on and Qp is off.

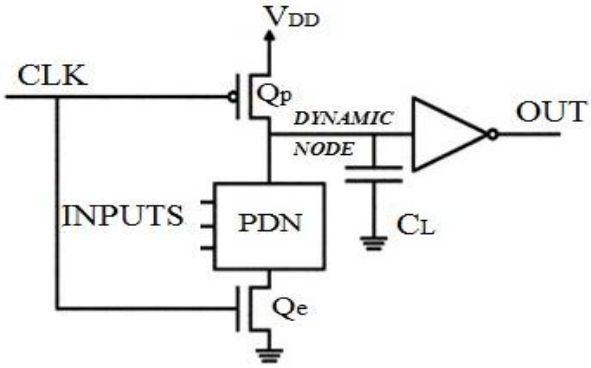

Fig 1: Basic Domino Circuit

When the input combination result in logic '0' then the dynamic node stays charged and output is low. When the input combination results in logic '1' then the dynamic node are discharged to ground and the output of the cmos inverter is high. However these domino logic gates suffer from lesser noise immunity and higher power dissipation [3]-[4]. As the technology scales down the leakage current increases and plays a pivotal role in the total power dissipation. Since the dynamic power is given by P=CV^2 f , so voltage must be waned to keep dynamic power within tolerable levels. However in order to meet the required conditions the threshold voltage (Vt) of the transistors must be reduced in order to compliment supply voltage scaling down, but this in turn result in exponential rise in the subthreshold leakage current.

Techniques such as the dual threshold voltage (DTV) which deploys high Vt and low Vt transistors are widely used in VLSI circuits to suppress the leakage current to reduce the total power dissipation. Dual threshold voltage-voltage scaling (DTVS) is a hybrid approach which incorporates both the DTV and the voltage scaling technique to gain an edge over the rudimentary DTV method. These techniques are discussed in section 2 of the literature. In this literature a novel stacked transistor–dual threshold voltage (ST-DTV) technique is proposed which incorporates the conventional DTV along with the stacked pMos and nMOS transistors and a voltage regulated static keeper. The paper is organized as follows: Section II analyzes the DTV. Section III analyzes the DTVS technique. Section IV proposes our novel design with a detailed description. Section V comprises of the simulation results and Section VI offers the wholesome conclusion of the literature.

2. Dual Threshold Voltage Technique

DTV is an efficient approach to quell the subthreshold leakage current in designing power efficient integrated circuits. The DTV technique deploys two types of transistors (a) high V_t transistors and (b) low V_t transistors. The high V_t transistors with thicker tox which aids in subduing the leakage current while the low V_t transistor are deployed in speed sensitive paths. In the Fig. 2 the DTV is implemented as a 3 input OR gate .Transistors (M1, M3, M4) are high V_t transistors which are active during the precharge phase of the domino circuit. The transistors (IN1, IN2, IN3, M5, and M2) which are low V_t transistors are active during the evaluation phase [5]. When the clock is low M1 is on such that the evaluation node is precharged to Vdd which turns off M4 and the output of the pMos inverter is low which as a result turns on M3. When the clock is set M1 is off and M2 is on and depending upon the logic combination, the evaluation node can stay high or can make a 1 to 0 transition.

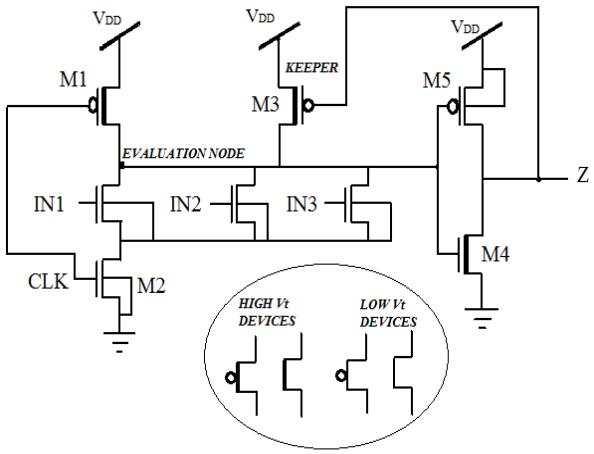

Fig 2: DTV Technique

The equation 1 below represents the sub threshold leakage current in the domino circuits [6]:-

$$I_{sub} = U_{ef}\left(\frac{W_{ef}}{L_{ef}}\right)\sqrt{\frac{(q\varepsilon_{si}N_c)}{2\varphi_s}}v_{th^2}\exp\left(\frac{V_{gs}-V_t}{nV_{th}}\right)\left(1-exp\left(-\frac{V_{ds}}{V_{th}}\right)\right) \quad (1)$$

where W_{ef} , U_{ef},L_{ef}, N_c, ε_{si} , V_{th}, φ_s, V_t and n are, effective channel width ,effective carrier mobility, effective channel length, effective channel doping, ,silicon permittivity ,thermal voltage, surface potential ,sub-threshold voltage and slope shape factor respectively[7]. From (1), it is inferred that the sub-threshold leakage current abates exponentially with the increasing of V_t, Thus, DTV can suppress the leakage current.

3. Dual Threshold Voltage- Voltage Scaling Technique

The Dual V_t technique was discussed in the last section, there is one more technique which has been adopted for the reduction of leakage power consumption i.e., the Voltage Scaling technique [6]. As it is known that average switching power dissipation is proportional to V_{DD}^2, as per the equation:-

$$P_{avg} = C_{Load}V_{DD^2}f_{clk} \quad (2)$$

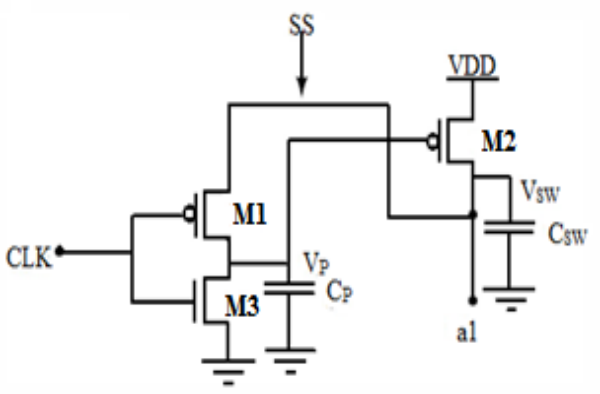

Fig 3: Voltage scaling and Charge sharing technique circuit

voltage difference (Vgs) of pMOS transistors determines the current of the M2. Csw and Cp shares charge through a self-stabilization connection with the help of SS path. The relation between Vsw, VDD and Vtp is: Vsw ≤ VDD - Vtp. As the DTV technique quells the circuit's leakage power and Voltage Scaling is useful in the ebb of dynamic power consumption hence, a coalition of dual threshold voltage and voltage scaling techniques will help in abating the total power consumption of the dynamic logic circuits. The Fig. 4, is an implementation of a 3-input OR gate using the DTVS approach. Here what is done is that instead of providing the circuit with supply voltage, VDD, the node a1 from the Fig.3 is connected to the circuit to provide the necessary power supply voltage. The transistors M1, M2 and M8 have a high V_t and the rest of the transistors are low V_t. When the clk = '0', the high V_t pMOS will be active and operates in pre-charge phase. During this phase, the output node will be low. But when clk makes a transition from low to high, then depending upon theological values of the nMOS network output will be obtained at the output node.

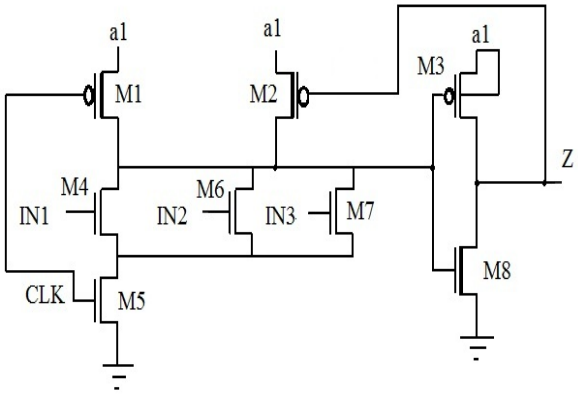

Fig 4: DTVS technique.

4. PROPOSED STACKED TRANSISTOR DUAL THRESHOLD VOLTAGE TECHNIQUE.

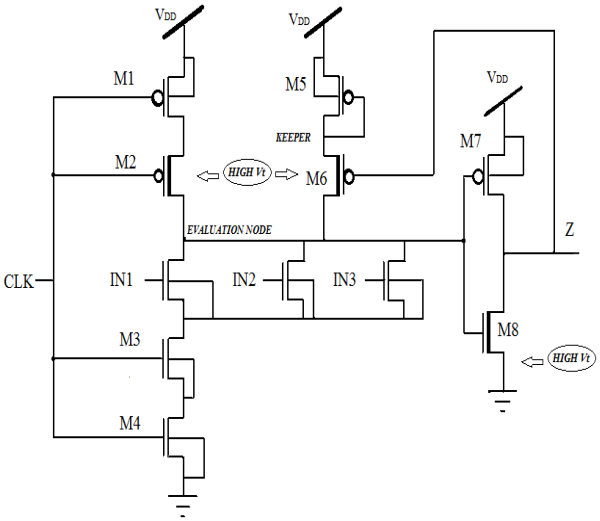

Fig 5: ST-DTV technique

The proposed stacked transistor dual threshold voltage (ST – DTV) technique is shown in the Fig. 5. This technique deploys forced stacked approach which helps us to waned the leakage current by dissevering an existing transistor into two transistors as a result the W/L of each of the dissevered transistors is half as compared to the existing transistor[9] . In the Fig. 5 M1 and M4 are the stacked such that (M1, M2) and (M3, M4) are two half size transistors. When the two dissevered transistors are switched off simultaneously, then the induced reverse bias between the two half divided transistors results in abatement of leakage current. This technique also incorporates a voltage regulated static keeper (VRSK) instead of a conventional pMos keeper as shown in Fig. 6. In VRSK a self biased M_p transistor is cascaded with the M_k transistor. By using the conventional keeper circuit the contention effect occurs when the dynamic node is to be evaluated as logic '0' as the keeper and the pull down network are simultaneously on. By incorporating VRSK the transistor M_k has a lower supply voltage with a weaker strength resulting in lowering the contention effect [10].

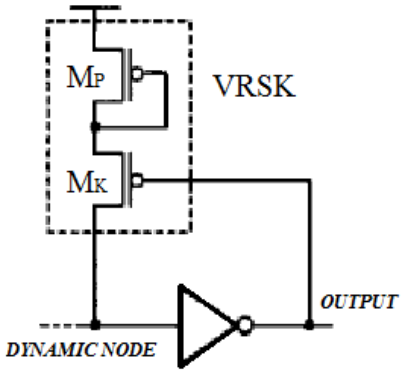

Fig 6: VRSK Keeper

When clock is low the M1, M2 are on and M3,M4 are off as a result the evaluation node is precharged to V_{DD} and the output of the CMOS inverter is low. During the evaluation phase the clock is high stacked pMos transistors are off and stacked nMos transistors are on. Depending on the combination of the inputs in the pull down network the evaluation node can stay charged or can make a high to low transition[11]-[12]. The proposed technique helps us to abate the sub threshold leakage current which result in reduce d power consumption. The circuit also exhibits better power delay product as compared to DTV and DTVS approaches.

5. SIMULATION RESULTS

The simulated results of different low power domino circuits are carried out on Tanner EDA Tool 13.0v for 1.2v and 1.7v at 500Mhz, 250Mhz, 166Mhz, 125Mhz and 100Mhz at 90nm CMOS Technology. The results are verified using a 3- input OR gate and a 4x1 Multiplexer. Table I and II show the power consumption (µW) at supply voltages 1.2 and 1.7v at different frequencies. The ST-DTV technique at 1.2v and 166 MHz consumes up to 28.56% less power as compared to the DTVS technique. The same circuit at 1.7v and 166 MHz consumes up to 32.33% less power than DTVS approach.

Table 1.Power consumption of 3-input OR gate at 1.2v.

Power Consumption(µW) at Supply Voltage 1.2v				
Frequencies	**DTV (µW)**	**DTVS (µW)**	**ST-DTV (µW)**	**Power Reduction (%)**
500MHz	4.47	4.04	3.25	19.29
250MHz	2.57	2.41	1.87	22.30
166MHz	2.16	1.81	1.29	28.56
125MHz	1.38	1.35	1.02	22.92
100MHz	1.24	1.08	0.890	17

Table 2.Power consumption of 3-input OR gate at 1.7v.

Power Consumption(µW) at Supply Voltage 1.7v				
Frequencies	**DTV (µW)**	**DTVS (µW)**	**ST-DTV (µW)**	**Power Reduction (%)**
500MHz	12.8	10.7	7.56	29.01
250MHz	7.99	5.84	4.54	22.26
166MHz	7.52	3.99	2.70	32.33
125MHz	4.22	3.27	2.35	28.13
100MHz	3.27	2.61	2.04	21.83

Fig. 7 and Fig. 8 show the graph of power consumption Vs frequency at 1.2v and 1.7v for 3 –input OR gate. From Table I and II ST – DTV techniques exhibits consistent results at other frequencies resulting in significant reduction of power consumption despite showing best results at 166 MHz. The reduction in the power consumption is due to the reduced sub threshold leakage current by deploying the stacked transistors together with a voltage regulated static keeper. The stacked transistor approach helps to abate the leakage current when the circuit is in the standby mode.

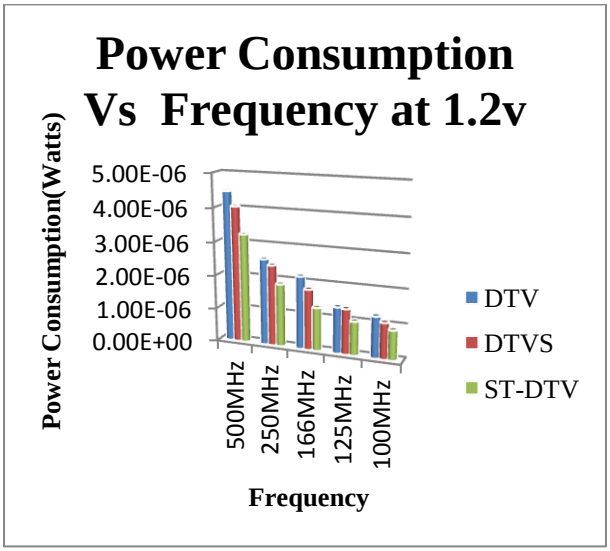

Fig 7: Power Consumption Vs Frequency at 1.2v for 3-Input OR gate

Table III shows the PDP at supply voltage 1.2v. The ST-DTV circuit at 166 MHz exhibits up to 27.70% less PDP as compared to the DTVS technique. Fig. 9 shows the power delay product of the 3- input OR gate at 1.2v supply voltage. The circuit shows consistent result with the other frequencies.

Table IV shows the power consumption of the above analyzed domino circuits at supply voltage 1.2v with respect to a 4x1 multiplexer. The Stacked Transistor dual threshold voltage technique when implemented with the multiplexer shows prodigious amount of abatement in the power consumption. The ST-DTV approach shows up to 57.75% of reduction in the power consumption at 250 MHz. Fig. 10 shows power consumption Vs frequency for a 4x1 multiplexer at 1.2v supply voltage. Table V shows the PDP at 1.2v at different frequencies. The ST-DTV technique shows up to 28.1% less power delay product as compared up to DTVS technique. The simulation results shows that ST-DTV technique is a high performance approach as compared to the DTV and DTVS techniques for domino logic circuits.

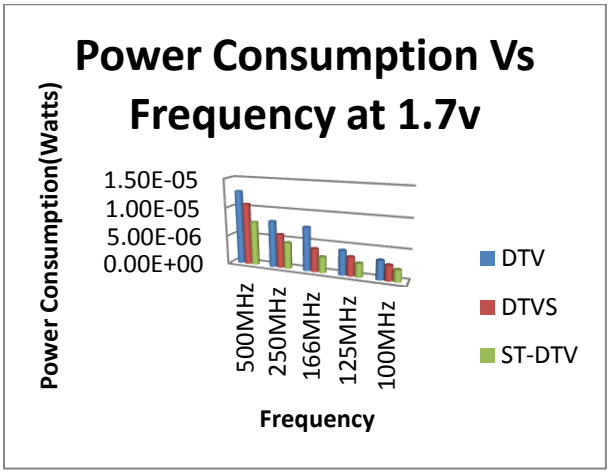

Fig 8 : Power Consumption Vs Frequency at 1.7v for 3-Input OR gate

Table 3. PDP of 3-Input OR gate at 1.2v

Power Delay Product (fWsec) at Supply Voltage 1.2v				
Frequencies	**DTV (fWsec)**	**DTVS (fWsec)**	**ST-DTV (fWsec)**	**PDP Reduction (%)**
500MHz	31.1	27.7	22.5	18.83
250MHz	16.5	15.3	12.0	21.43
166MHz	12.8	10.6	7.64	27.70
125MHz	7.48	7.25	5.51	23.93
100MHz	6.15	5.25	4.38	16.66

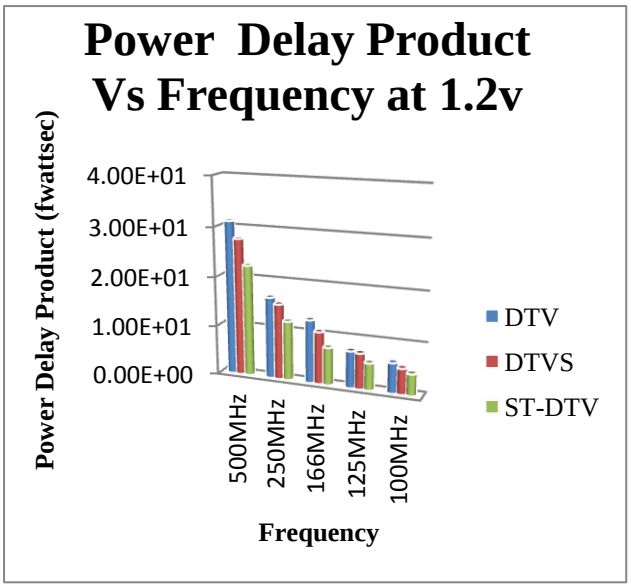

Fig 9: Power Consumption Vs Frequency at 1.2v for 3-Input OR gate

Among the three techniques analyzed that is the DTV,DTVS and the ST-DTV technique it is also necessary that the value of threshold voltages which are used are properly set so as exhibit the correct functioning of the above analyzed circuits.

Table 4. Power Consumption of 4x1 MUX at 1.2v

Power Consumption(µW) at Supply Voltage 1.2v				
Frequencies	**DTV (µW)**	**DTVS (µW)**	**ST-DTV (µW)**	**Power Reduction (%)**
500MHz	12.5	8.93	4.26	52.29
250MHz	7.06	5.87	2.48	57.75
166MHz	4.99	4.02	1.84	54.23
125MHz	4.88	3.84	1.68	56.25

6. CONCLUSION

In this research new technique named Stacked Transistor Dual Threshold voltage (ST-DTV) has been proposed for the domino logic circuit and has been compared with the DTV and DTVS technique. The results are analyzed with respect to a 3- input OR gate and a 4x1 multiplexer. In case of the 3-input OR gate there is prodigious amount of reduction in the power consumption such that is has been reduced up to 28.56% for 1.2v supply voltage and up to 32.33% for 1.7v supply voltage. There is also a colossal improvement in the power delay product such that it has been improved up to 27.70% at 1.2v supply voltage for the 3-input OR gate. In case for a 4x1 Multiplexer the power consumption has been reduced to about 57.75% at 1.2v supply voltage with a power delay product improvement of about 28.1%.

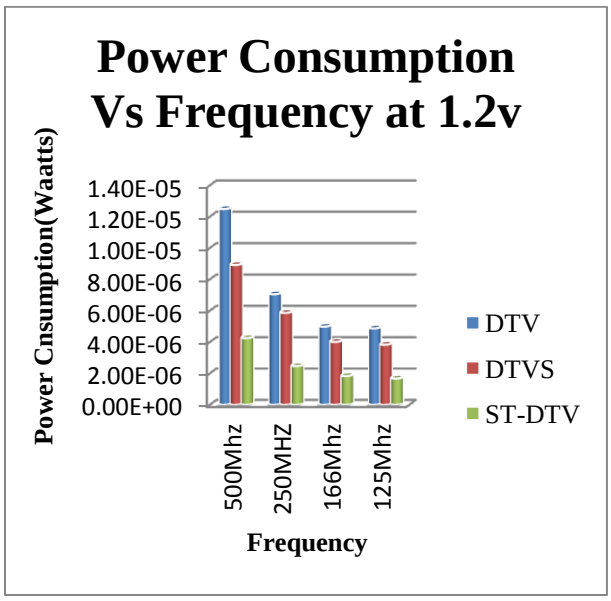

Fig.10:Power Consumption Vs Frequency for 4x1 Mux

Table 5. PDP of 4x1 MUX at 1.2v

Power Delay Product (fWsec) at Supply Voltage 1.2v				
Frequencies	**DTV (fWsec)**	**DTVS (fWsec)**	**ST-DTV (fWsec)**	**PDP Reduction (%)**
500MHz	45.84	35	32.83	6.2
250MHz	28.63	20	17.45	12.5
166MHz	23.13	11.67	9.01	22.79
125MHz	10.90	9.29	6.68	28.1
100MHz	6.68	4.63	4.39	5.18

7. REFERRENCES

[1] S.M. Kang, Y. Leblebici ,"CMOS Digital Integrated Circuits analysis and design," third edition, TMH, 2003.

[2] N.Weste and D. Harris, "CMOS VLSI Design,". Reading, MA: Addison Wesley, 2004.

[3] M. J. Mohannnadzamani, S. M. Tabatabaei and M. Fathipour, "Leakage Current Reduction in Domino Logic," in Proc. ICEE, Tehran, 2012, pp. 198-201.

[4] Y .S. Abdalla , A. A. Dessouki , and E .S. El-Badawy ,"Compensating for the Keeper Current ofCMOS

Domino Logic Using a Well Designed NMOS Transistor," in Proc. NRSC, Egypt , 2009 , pp. 1-8.

[5] V.Kurson and E. G .Friedman ,"Energy Efficient Dual Threshold Voltage Dynamic Circuits Employing Sleep Switches to Minimize Subthreshold Leakage," in Proc. ISCAS, 2004, pp. 417-420.

[6] J. Wang, W. Wu, N. Gong, W. Zhang, and L. Hou, "Effectiveness Analysis of Low Power Technique of Dynamic Logic under Temperature and Process Variations," in Proc. AISCON , 2009, pp. 1236-1239.

[7] G. Yang, Z. Wang, and S. M. Kang, "Leakage-Proof Domino Circuit Design for Deep Sub-100nm Technologies," in Proc. ICVD, 2004, pp.222-227.

[8] P.Arun, S.Ramasamy ,"A Low-Power Dual Threshold Voltage Voltage Scaling Technique for Domino Logic Circuits," in Proc. ICCCNT, 2012, pp.1-6.

[9] S.H.Kim ,V.J. Mooney ,"Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design," in Proc . VLSISOC, 2006, pp.367-372.

[10] S.J. Shieh, J.S. Wang and Y.H. Yeh ,"A contention-alleviated static keeper for high-performance domino logic circuits," in Proc. ICECS ,2001, pp.707-710.

[11] H. Upadhyay, A. Choubey, K.Nigam "Comparison Among Different Cmos Inverter With Stack Keeper Approach in VLSI design," IJERA , Vol. 2, Issue 3, May-Jun 2012, pp. 640-646..

[12] H.Kanno, T.Saeki, H.Abiko, A. Kubo, and K.Tokashiki,"A Voltage-Regulated static Keeper Technique for high-performance ASICs," in Proc. ASIC conference ,1998,pp.361-368.