Transistor Sizing in Order to Hardening CMOS circuit against Soft Error

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ABSTRACT
Due to the shrinking of feature size and reduction in supply voltages, nano scale circuits have become more susceptible to radiation induced transient faults. Transient faults caused by radiation are becoming a major barrier to robust system design manufactured at technology nodes like 90nm, 65nm or smaller. A single event upset (SEU) may cause a bit flips in some latches or memory elements, thereby altering the state of the system, leading to a soft error. Soft errors in memory have traditionally been a much greater concern than soft errors in logic circuits. In this paper we propose an accurate and prompt approach in order to finding minimum transistor size to hardening CMOS circuits against SEU. One of the hardening CMOS circuit methods against SEU is transistor sizing; a large transistor can dissipate the injected charge as quickly as it is deposited so that the transient does not achieve sufficient magnitude and duration to propagate to gates in fan out. Most hardening methods based on transistor sizing have high area overhead. Since the suggested method at this paper is obtained minimum transistor size for hardening, the optimization of area will be done. experimental results show that present mathematical model results are agree well with SPICE simulations, while allowing for very fast analysis.

Keywords
SEU, soft error, particle energies, combinational CMOS circuits

1. INTRODUCTION
Soft errors in combinational circuits are becoming as important as errors in memory elements. Continuous device scaling and increasing pipeline lengths contribute to the increase in soft error rates in data-path structures. The masking effects that prohibit the increase in soft error rates in logic circuits are not sufficient to prevent further rise in error rates. Soft errors are temporary errors caused mainly because of external radiations .Such radiations directly or indirectly induce localized ionization capable of upsetting internal data states. The kinetic energy of the particles hitting silicon substrate generates electron hole pairs as they pass through the p-n junctions. These electron hole pairs generate short duration current pulses that cause soft errors. In memory circuits and latches, these errors are just a flip in the stored values, which result in temporary changes in the output of combinational circuits. In logic circuits, errors occur when the temporary changes in the output are latched[2].

The effect of a particle striking a node in a circuit can be modeled as a narrow current pulse of a given magnitude and duration being injected into a node. For example, a transient pulse caused by an alpha-particle can be modeled as a double exponential injection current given by [3]. with the continuous downscaling of technology, the capacitance values are decreasing. Hence, for a given amount of charge transferred by an energized particle, the voltage change caused at a node is much greater (Q= CV). Hence, nanometer circuits are getting more susceptible to such transient errors. As noted earlier, a transient pulse generated at a node of a combinational circuit can cause error if it propagates and gets captured by a flip-flop. There are three mechanisms in combinational logic circuits which mask the glitches generated by particle strikes [4]: Logical masking, electrical masking and time window masking.

Logical masking: a glitch might not propagate to a latch because of a gate on the path not being sensitized to facilitate such glitch propagation, e.g. one of the inputs of a “and gate” being at zero. Figure 1 illustrates an example of logical masking.

Electrical masking: a generated glitch might get attenuated because of the delays of the gates on the path to the output. Figure 2 illustrates an example of electrical masking.

Time window masking: a glitch that reaches the primary output might not cause an error because of the latch not being open ,Figure 3 illustrates an example of time window masking [4-5].

However, because of the decreasing number of gates in a pipeline stage, logical masking as well as electrical masking has been decreasing for new technology generations. Electrical masking has also been decreasing because of the reduction in node capacitance and supply voltages in every generation. Furthermore, increasing clock frequencies have reduced the time window in which latches are not transparent, thereby reducing latching-window masking. Thus it is clear that soft errors are really important in today’s era of nanometer circuits.[6].

Hardening methods against SEU divided to three categories include: Device level methods, Circuit level methods, System level methods.

Device level methods are methods which consist of fundamental changes or an enhancement to the fabrication process. And mainly, mitigate the effects of charge collection at the site of the particle strike. Proposed techniques include

an extra doping layer to limit substrate charge collection [6]. Hardening methods at system level for logical circuits usually is based on redundancy in to the design to achieve capability of fault detection/ correction. Their most popular ones are error detection and correction codes which usually has a lot of applications at memories [6-7].Circuit level methods include insertion feedback elements such as resistance and capacitance at gate cells to slow propagation of SEU (voltage transient) to circuit output [6-8-9-10]. Considered method at this paper belongs to the category of methods which increase the node critical charge. Critical charge is minimum amount of charge that is needs to be deposited by a particle strike to produce SEU. At this method hardening nodes is conducted by adding a capacitance for increasing critical charge. One of the implementation methods for increasing the size of a capacitance at node is to use transistor sizing [11-12].

This paper, at first, is obtained the governing equations of transistor sizing to find mathematical model which can be easily solved by software such as Matlab and at the second part is applied the equations on an example with respect to the total problem and at last is compared the results with the spice method.

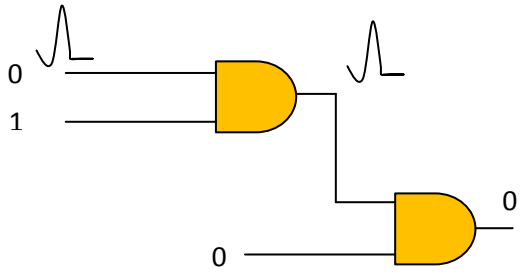

Fig 1: logical masking

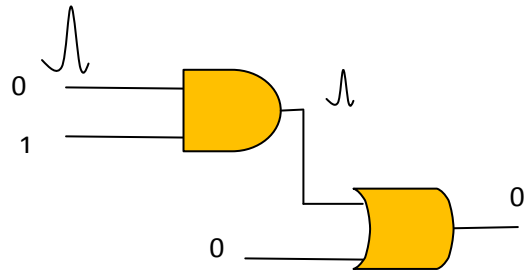

Fig 2: Electrical Masking

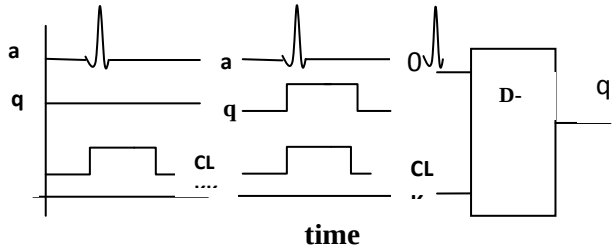

Fig 3: time window masking

2. SIZING FOR HARDENING

Logical gates for designing combination CMOS circuits include: NOT, NAND, AND, NOR, OR. For implementation of this gates, every input of a gate connects to a NMOS transistor and a PMOS transistor that is similar to a NOT gate. So the analysis of NOT gate is not opposite of total problem and equations are the same for other gates. To obtain an exact and efficient mathematical model and for calculating minimum transistor (W/L)min a NOT gate which is shown at figure 4 is used. Cout is the output capacitor at node M and is obtained by scaling the unit output capacitance Cunit. Cp is lumped parasitic capacitance at node M. CL is total capacitance associated with node M.(W/L) is NMOS transistor size. According to figure 4, equations can be written

$$C_{out} = C_{unit} \times (\frac{w}{L}) \qquad (1)$$
$$C_L = C_P + C_{unit} \times (\frac{w}{L})$$

$I_{in}(t)$ denotes the double exponential current pulse produced as a result of a particle strike at M. $I_{in}(t)$ has been approximated by a double exponential current pulse injected into the site of the particle strike.

$$I_{in}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)} \times (e^{(\frac{-t}{\tau_\alpha})} - e^{(\frac{-t}{\tau_\beta})}) \qquad (2)$$

In the above equation, Q is the amount of injected charge that is deposited as a result of a particle strike, τ_α represents the collection time-constant of the junction, and τ_β accounts for the ion-track establishment time-constant. At this paper, the worst condition for SEU at logic "0" and logic "1" is considered. Fault at logic one (zero) happens when inputs are settled at logic one (zero) and outputs are settled at logic zero (one) and SEU cause output value to transfer from zero (one) to one (zero). There is no difference mathematically in changing an output from logic "0" to logic "1" or logic "1" to logic "0" by injecting, so that at this paper a situation considered that a SEU cause the output value to transfer from logic "0" to logic "1" and the input is at logic "1" without fault. This paper is focused on V_{out} because its magnitude and duration will determine how SEU propagates through primary outputs of gates.

According to figure 4, equation3 will be written:

$$C_L \frac{dV_{out}}{dt} = I_{in}(t) - (\frac{w}{L}) \times I_D(V_{out}) \qquad (3)$$

$$I_D(V_{out}) = \beta \times (2 \times (V_{gs} - V_{th}) V_{out} - V_{out}^{\ 2}) \qquad (4)$$
$$\beta = \frac{1}{2} \mu_n C_{ox}$$

$$I_D(V_{out}) = \beta \times (V_{gs} - V_{th})^2 \qquad (5)$$

Because it is assumed that drain transistor voltage cannot be more than threshold voltage value, therefore equation 4 can

be substituted at equation 3. By solving equation 3, Vout for $\tau_\beta < \tau_\alpha$ can be obtained from the below equation [13]

$$V_{out} = \frac{I_0 \times \tau_{\alpha \times R}}{\tau_{\alpha\text{-}R\times C}} \times (e^{(\frac{-t}{\tau_\alpha})} - e^{(\frac{-t}{RC})}) \quad (6)$$

Where R is effective PMOS or NMOS transistor resistance [13]

$$R = 1 \Big/ \mu_n C_{ox} \left(\frac{w}{L}\right) \times (V_{gs} - V_{th}) \quad (7)$$

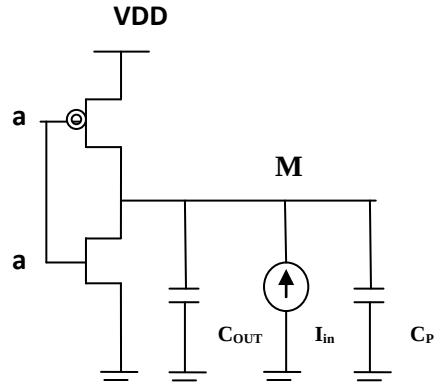

Fig 4: inverter gate

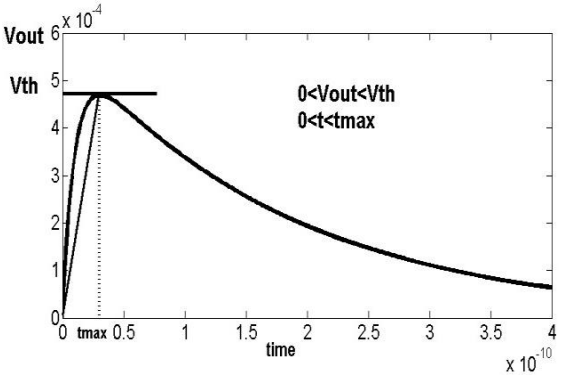

Fig 5: linear approximation of v_{out}

To calculate (W/L) a maximum value of Vout is needed to restrict to a specified value. This paper is assumed that voltage at M point is equal to NMOS transistor threshold voltage. When Vout voltage increases from zero value until Vth (threshold voltage), NMOS transistor is at linear region. Also from a linear approximation which is shown at figure 5 used for calculating (W/L).

$$t_{\max} = \frac{\ln(\frac{\tau_\alpha}{RC}) \times \tau_\alpha \times RC}{\tau_\alpha - R \times C} \quad (8)$$

Tmax is the time when Vout achieve its maximum value. When maxium value of Vout at Tmax point becomes equal to Vth dVout/dt=0 should be confirmed

$$I_{in}(t_{\max}) - (\frac{w}{L}) \times I_D(V_{out}) = 0 \quad (9)$$

$$(\frac{w}{L})_{\min} = \frac{I_{in}(t_{\max})}{I_D(V_{th})}$$

By substituting equation 8 at equation 6, Vpeak can be obtained from below equation [13].

By simplification equation 10, an exact and simple equation

$$V_{\max} = \frac{I_0 \times \tau_\alpha \times R}{\tau_{\alpha\text{-}R\times C}} \times ((\frac{\tau_\alpha}{R\times C})^{\frac{R\times C}{(R\times C - \tau_\alpha)}} - (\frac{\tau_\alpha}{R\times C})^{\frac{\tau_\alpha}{(R\times C - \tau_\alpha)}}) \quad (10)$$

for maximum Vout can be obtained [13].

$$V_{out(\max)} = \frac{I_0 \times \tau_{\alpha \times R}}{\tau_{\alpha + R\times C}} \quad (11)$$

By substituting equation 1,7 and 9 at equation 11 and solving the equations, minimum value of the transistor can be obtained.

3. SIMULATION RESULT

According to the figure 6, by increasing at transistor size, the effect of striking particle energies will be decreased, while increasing transistor size causes increasing in area overhead and delay of original circuit. Here is tried to choose the minimum transistor size that prevent the conversing fault and does not exist overload for final circuit. To simulate at spice and analytical method, 0.18 um TSMC technology parameters are used and $\tau_\beta = 0.0125$ and $\tau_\alpha = 0.05ns$ values are considered [14]. For various injected charge value spice simulation is iterated with various transistor sizes, answer is obtained when output voltage becomes equal to threshold voltage. Figure 7 shows suggested method results and spice simulation results. It is proved that used equations are correct and accurate by approaching suggested method results to spice simulation results. In addition, by using this new method the analysis time will be decreased .hardening against SEU and obtaining the transistor optimized size with spice simulation is very time-consuming at CMOS circuits which have high a lot of logic gates. To extend suggested analysis method to high volume of CMOS circuits, first circuit is synthesized by synthesis tools such as design compiler and is optimized by area, power or delay factors. Then sensitive nodes of circuit are identified by tools such as ATPG. Then by traverse the circuit from the primary outputs to primary inputs and identify sensitive nodes and using suggested analysis model at this paper, minimum transistor size at sensitive node to SEU is calculated and by changing the size of transistor to optimized value, node will be hardened.

4. CONCULATION

Radiation-induced soft errors threaten the reliability of computer systems. As the device sizes are shrinking, combinational logic will also become equally susceptible to soft errors as the memory elements in few years.

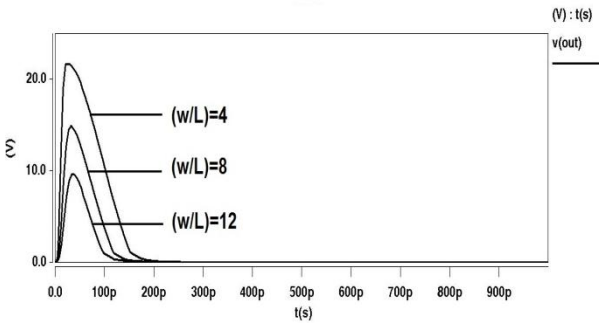

Fig 6: The Effect Of Transistor Sizing On V_{out}

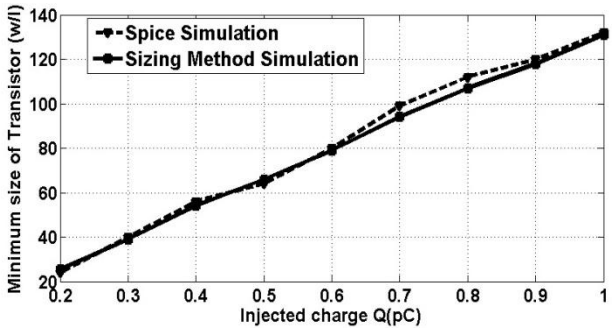

Fig 7: Simulation Result

This paper is suggested an exact and prompt method to find minimum transistor size to harden CMOS circuits. Most hardening methods based on transistor sizing have high area overhead. Since the suggested method at this paper is obtained minimum transistor size for hardening, the area would be optimized. Studying results shows that the result of suggested model is similar to spice but the simulation time is very less than Spice.

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