Design of Efficient Reversible Fault tolerant Adder/Subtractor

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ABSTRACT

In recent years, reversible logic is the most popular and emerging technology and it will be having wide applications in the field of Low power CMOS, quantum computing and optical computing. Circuits with reversible logic gates provide low power dissipation and low energy loss. This paper proposes the Adder/Subtractor designs that are used in many DSP applications. This paper proposes the efficient Adder/Subtractor design in terms of gate count, garbage outputs, constant inputs and quantum cost. The proposed circuits will simulated using ModelSim simulator and implemented on Xilinx FPGA platform.

Keywords

Reversible Logic Gates, Full Adder/Subtractor, Parallel Adder/Subtractor, BCD Adder/Subtractor.

1. INTRODUCTION

In today's life require technology that will offers faster in operating and complex and smaller devices means circuits which occupies less area and consists more number of transistors in that small area. As the faster operating and smaller, complex in terms of area occupation the technology makes increased power dissipation in the circuit. In 1961 R. Landauer [1] proposed that "The logic components that are not reversible during computation process generate heat energy of kTln2 joules of energy for every bit of information that is lost". Where k is Boltzmann's constant and T is absolute temperature, at room temperature T for one bit loss, it will generate 2.86×10^{-21} Joules of energy, this value will be small but we cannot neglect this value. In larger design for bit loss the energy dissipation will be high, this will increases the power dissipation and reduces the life time of the device. In 1973 C. H. Bennet [2] proposed that "If the computation can be done in reversible manner zero energy dissipation is possible". The amount of energy dissipated is related to the number of bit loss in computation. Reversible circuits can be constructed with a set of reversible logic gates. Arithmetic circuits such as Adders, Subtractors and Multipliers are the essential blocks of a computing system. The Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic.

2. REVERSIBLE LOGIC GATES

The reversible logic gates will be having n-input and n-output i.e. equal number of input and equal number of output. In reversible logic inputs can be uniquely recovered from the output. If a reversible gate has k inputs, and therefore k outputs, then it is a k*k reversible gate. In reversible gates fan out are not permitted, if there it must not exceed more than

one. No feedback paths are allowed i.e. circuit is acyclic. Some important factors in reversible logic are Garbage output, constant input, quantum cost etc [3, 4].

Gate Count (GC):
It is the number of reversible gates used to realize the system.

Garbage Output (GO):
It is the unutilized output from the reversible gate, it is very much essential to achieve reversibility and it must be not used for further computation.

Constant Input (CI):
Constant inputs are those inputs that are used to generate a given logical expression using the reversible logic gates. Constant inputs are maintained at either a constant 0 or constant 1.

Quantum Cost (QC):
Each reversible gate has a cost associated with it called quantum cost [5, 6]. The quantum cost of a reversible gate is the number of 2*2 reversible gates or quantum logic gates required in designing it. The quantum cost of all reversible 2*2 gates is taken as unity. The cost of all the 1*1 reversible gates such as NOT gate is assumed to be zero [5].

An efficient design in reversible logic should have the following features [7]:
- Use minimum number of reversible logic gates
- Should have less number of garbage outputs
- Less number of constant inputs and
- Minimization of quantum cost.

The basic reversible logic gates exist in the literature is Feynman Gate [8], Peres Gate [9], Toffoli Gate [10] and Fredkin Gate [11].

Fault tolerant circuit means the system to continue its operation properly when failure occurs in any of the component. In a circuit due to errors system failure happens. The errors can be detected by parity checking. If the system will be made up using fault tolerant components then the error detection and correction process will much easier. B Parhami [12] shown some methods of error detection in reversible circuits, those standard methods of error detection will presents some problems because in reversible logic circuits fan out are not permitted and we have to take care of garbage bits. For parity preserving output data, the data can be checked in a manner i.e. in a computational critical path. For parity preserving gate the ex-or of input will matches with the ex-or of output. For a 4*4 reversible gate it will satisfies the condition of $A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$, where $A \oplus B \oplus C \oplus D$ is input parity and $P \oplus Q \oplus R \oplus S$ is output parity. This means that the gate will be parity preserving. Therefore parity preserving circuits will be future design trends to design fault tolerant

reversible systems. So fault tolerant circuits can be constructed by parity preserving reversible logic gates. Some of the parity preserving reversible gates are 3*3 Feynman double gate (F2G) [12], 3*3 Fredkin gate (FRG) [11], 4*4 IG gate [13], 4*4 Modified IG (MIG) gate [14], 3*3 NFT gate [15] etc.

Feynman Double Gate (F2G):
Feynman double gate (F2G) [12] is a 3*3 gate shown in Figure 1. It has A, B and C as input vector and output vector as P = A, Q = A⊕B, and R = A⊕C. Quantum cost is equal to 2.
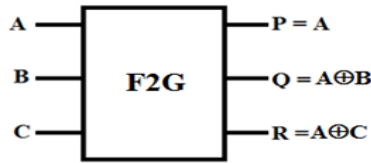
Figure 1: Feynman Double Gate (F2G)

Fredkin Gate (FRG):
Fredkin gate (FRG) [11] is a 3*3 gate shown in Figure 2. It has A, B and C as input vector and output vector as P = A, Q= A′B⊕AC and R = A′C⊕AB. Quantum cost of FRG gate is 5.
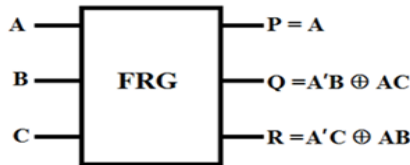

Figure 2: Fredkin Gate (FRG)

Islam Gate (IG):
Islam gate (IG) [13] is a 4*4 gate shown in Figure 3. It has A, B, C and D as input vector and output vector as P = A, Q = A⊕B, R = AB⊕C and S = BD⊕B′(A⊕D). Quantum cost of IG gate is 7.
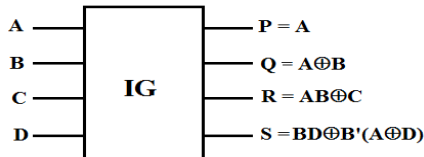

Figure 3: Islam Gate (IG)

Modified IG Gate (MIG):
Modified IG gate (MIG) [14] is a 4*4 gate shown in Figure 4. It has A, B, C and D as input vector and output vector as P = A, Q = A⊕B, R = AB⊕C and S = AB′⊕D. Quantum cost of MIG gate is 7.
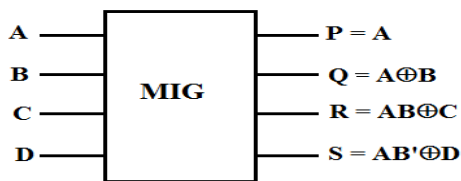

Figure 4: Modified IG Gate (MIG)

New Fault Tolerant Gate (NFT):
New Fault Tolerant gate (NFT) [15] is a 3*3 gate shown in Figure 5. It has A, B, C and D input vector and output vector as P = A, Q = BC′⊕AC′ and R = BC⊕AC′. Quantum cost of NFT gate is 5.
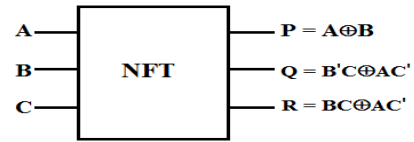

Figure 5: NFT Gate (NFT)

3. PROPOSED DESIGN

The proposed design will work singly a unit which consists of both adder and subtractor. The design will consists of control line ctrl which will selects adder or subtractor according the control logic input i.e. when ctrl is at logic 0, the circuit will acts as adder and when ctrl is at logic 1, the circuit will acts as subtractor. The below section covers the design of reversible fault tolerant half adder/subtractor, full adder/subtractor, 8-bit parallel adder/subtractor and 4-bit BCD adder/subtractor.

3.1 Fault Tolerant Half Adder/Subtractor (FT_HAS)

The Fault Tolerant Half Adder/Subtractor (FT_HAS) [17] is realized using one Modified IG (MIG) gate and one Fredkin gate (FRG) shown in Figure 6. The design will be having two inputs A & B and a control line ctrl which will controls mode of operation i.e. when ctrl is at logic 0, the circuit will acts as half adder and when ctrl is at logic 1, the circuit will acts as half subtractor [16]. It will be having two constant inputs that are forced at logic 0 and three garbage bits g1 to g3. Quantum cost of this circuit is 12.
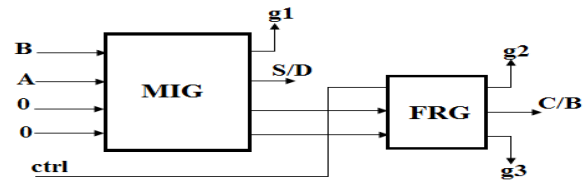

Figure 6: Fault Tolerant Half Adder/Subtractor (FT_HAS) Circuit [17]

3.2 Fault Tolerant Full Adder/Subtractor (FT_FAS)

The Fault Tolerant Full Adder/Subtractor (FT_FAS) is realized using Two Modified IG (MIG) gate, one Fredkin gate (FRG) shown in Figure 7. The circuit will be having three inputs A, B & C_{in} (For full subtractor A, B & B_{in} are inputs) and a control line ctrl which will controls mode of operation i.e. when ctrl is at logic 0, the circuit will acts as full adder and when ctrl is at logic 1, the circuit will acts as full subtractor [16]. It will be having two constant inputs that are forced at logic 0 and four garbage bits g1 to g4. Quantum cost of this circuit is 19.
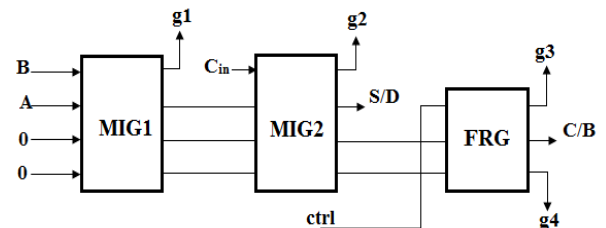

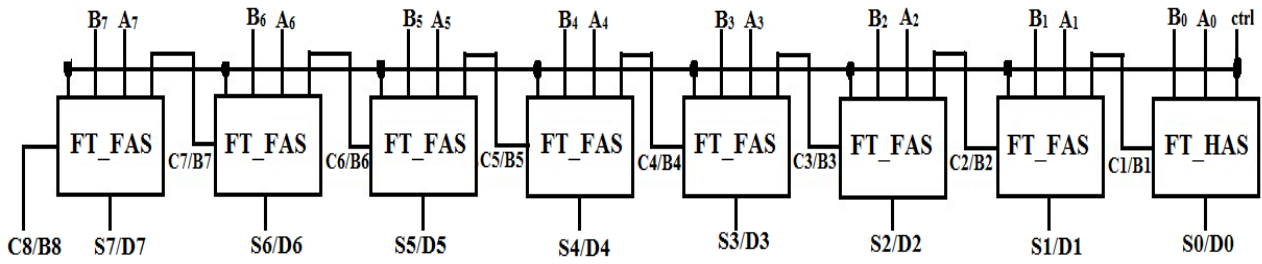**Figure 7: Fault Tolerant Full Adder/Subtractor (FT_FAS) Circuit**

Figure 8: Fault Tolerant 8-Bit Parallel Adder/Subtractor Circuit

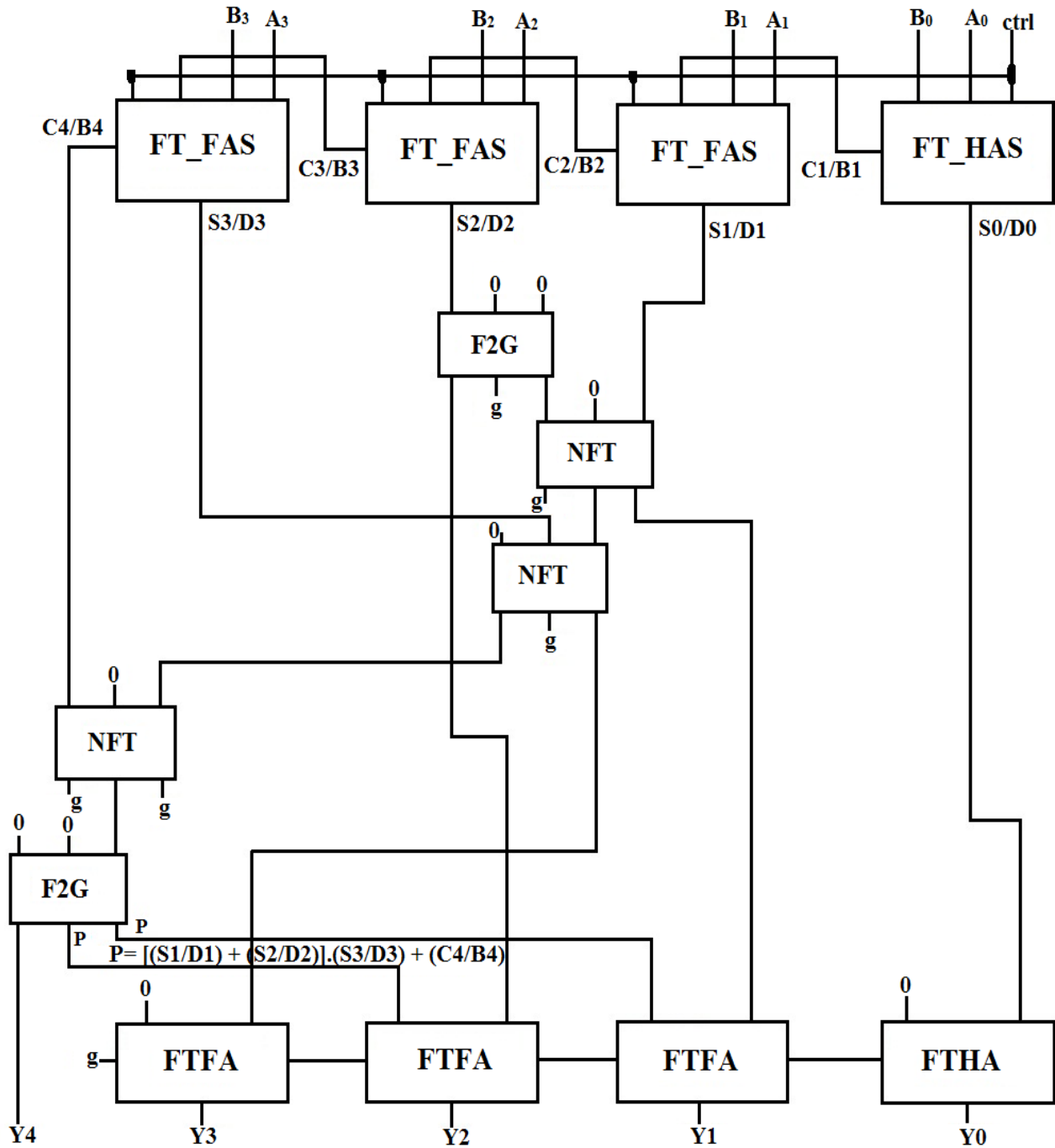$$P= [(S1/D1) + (S2/D2)].(S3/D3) + (C4/B4)$$

Figure 9: Fault Tolerant 4-bit BCD Adder/Subtractor Circuit

3.3 Fault Tolerant 8-bit Parallel Adder/Subtractor

A n-bit parallel adder/subtractor will require chain of n full adders/subtractors and one half adder/subtractor. Therefore 8-bit Fault Tolerant Parallel Adder/Subtractor is constructed by using One Fault Tolerant Half Adder/Subtractor (FT_HAS) and Seven Fault Tolerant Full Adder/Subtractor (FT_FAS). It will having two 8-bit numbers are A_0 to A_7 and B_0 to B_7 as inputs and a control line ctrl which will control the mode of operation i.e. when ctrl is at logic 0, the circuit performs 8-bit addition and when ctrl is at logic 1, the circuit performs 8-bit subtraction. The Carry/Borrow obtained after Addition/Subtraction is represented by C1/B1 to C7/B7. The outputs Sum/Difference and Carry/Borrow are shown as S0/D0 to S7/D7 and C8/B8 respectively [19].The Figure 8 shows the 8-bit Fault Tolerant Parallel Adder/Subtractor.

3.4 Fault Tolerant 4-bit BCD Adder/Subtractor

4-bit Fault Tolerant BCD Adder/Subtractor shown in Figure 9 is constructed using 4-bit Fault Tolerant Parallel Adder/Subtractor and 4-bit Fault Tolerant Parallel Adder (constructed using Seven MIG gate) [20] and BCD error detection circuit (Three NFT and Two F2G gate) [18]. The Sum/Difference of the Fault Tolerant Parallel Adder/Subtractor examined by BCD error (BCD error means non BCD number) detection circuit by using the formula,

$$P= [(S1/D1) + (S2/D2)].(S3/D3) + (C4/B4)$$

If BCD error is there it will shows P=1, then Sum/Difference is added by 0110 in Fault Tolerant Parallel Adder to convert into the BCD value. If there is no BCD error i.e. P=0, then Sum/Difference is added by 0000 in Fault Tolerant Parallel Adder to get the result.

4. RESULTS

The entire design is modeled using Verilog. The coding is done on Xilinx ISE13.2 on Spartan 3 using target device: XC3S400-PQ208 at speed grade of -5. Simulation can be done using ModelSim SE 6.3f simulator.

The simulation result for FT_HAS is shown on Figure 10 & Figure 11 and FT_FAS is shown on Figure 12 & Figure 13 and Parallel Adder/Subtractor is shown on Figure 14 & Figure 15 and BCD Adder/Subtractor is shown on Figure 16 respectively.
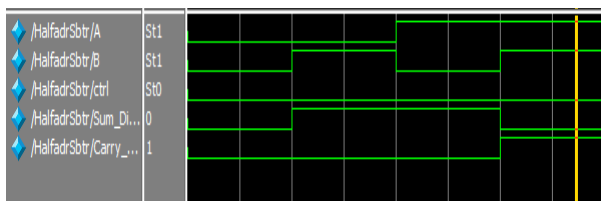

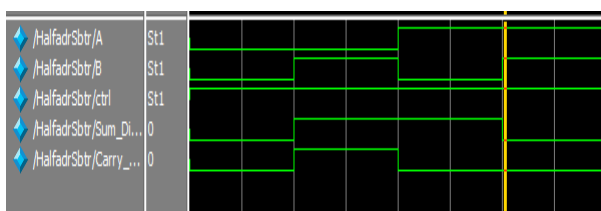**Figure 10: Simulation result of Fault Tolerant Half Adder**

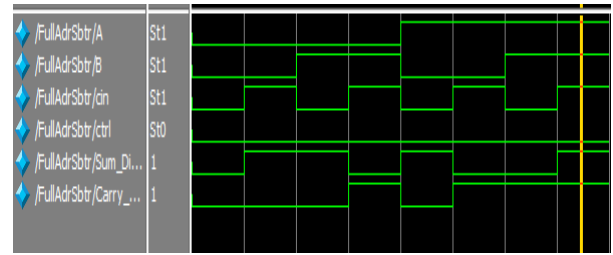**Figure 11: Simulation result of Fault Tolerant Half Subtractor**

Figure 12: Simulation result of Fault Tolerant Full Adder

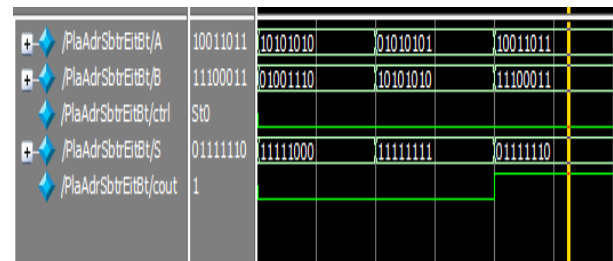**Figure 13: Simulation result of Fault Tolerant Full Subtractor**

Figure 14: Simulation result of Fault Tolerant 8-Bit Parallel Adder
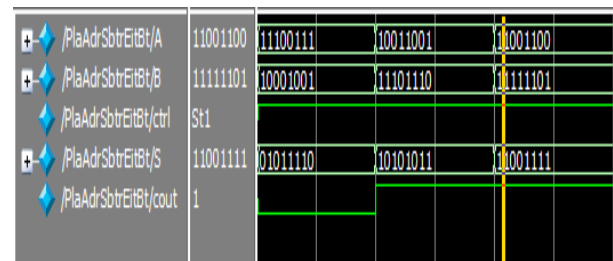

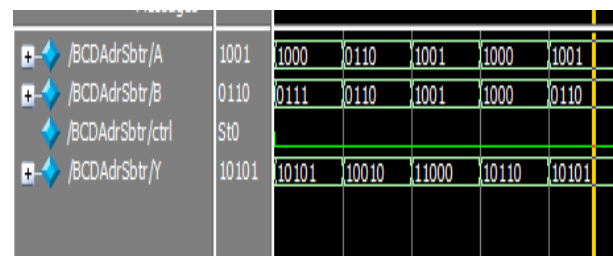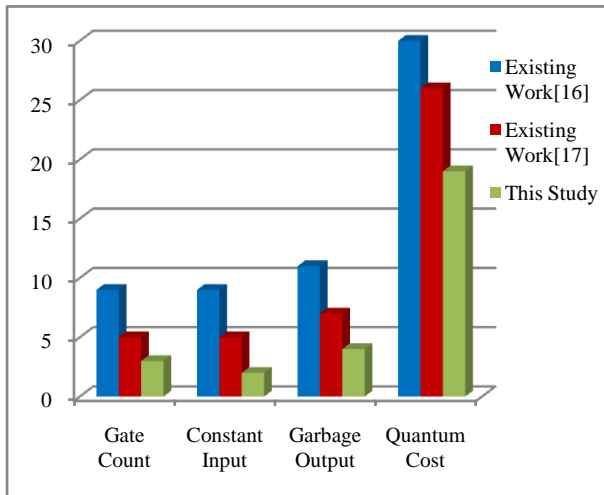**Figure 15: Simulation result of Fault Tolerant 8-Bit Parallel Subtractor**

**Figure 16: Simulation result of Fault Tolerant 4-bit BCD Adder**

Table 1, Table 2 and Table 3 shows the comparison of experimental results of different Fault Tolerant Full Adder/Subtractor, 8-Bit Parallel Adder/Subtractor and 4-bit BCD Adder/Subtractor.

Table 1. Comparative experimental results of different Fault Tolerant Full Adder/Subtractor
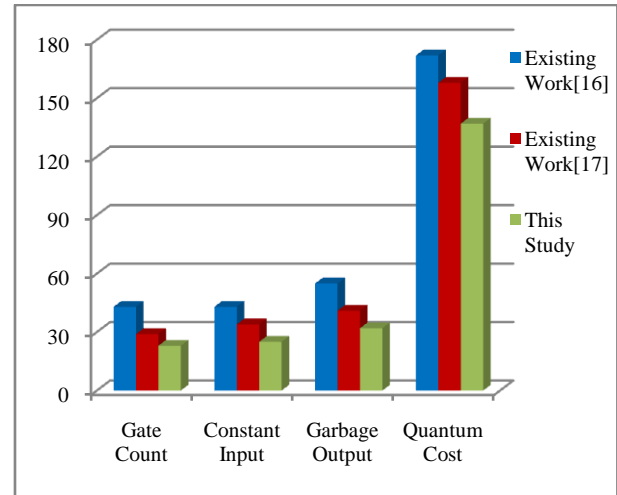
	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work[16]	9	9	11	30
Existing Work[17]	5	5	7	26
This Study	3	2	4	19

Figure 17: Graphical Representation of comparison of different of Fault Tolerant Full Adder/Subtractor

Table 2. Comparative experimental results of different Fault Tolerant 8-Bit Parallel Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work[16]	67	67	82	224
Existing Work[17]	37	37	52	194
This Study	23	16	31	145
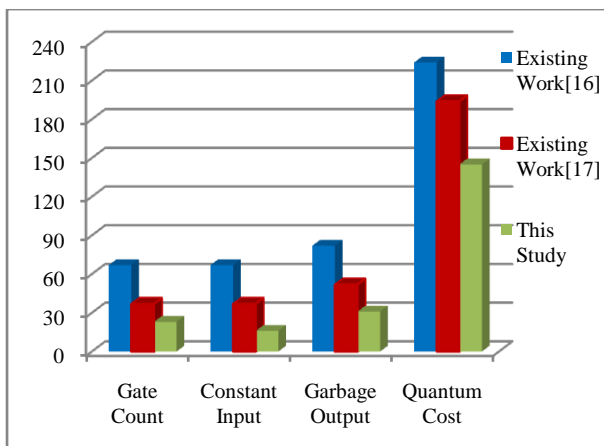
Figure 18: Graphical Representation of comparison of different Fault Tolerant 8-Bit Parallel Adder/Subtractor

Table 3. Comparative experimental results of different Fault Tolerant 4-bit BCD Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Quantum Cost
Existing Work[16]	43	43	55	172
Existing Work[17]	29	34	41	158
This Study	23	25	32	137

Figure 19: Graphical Representation of comparison of different of Fault Tolerant 4-bit BCD Adder/Subtractor

5. CONCLUSION AND FUTURE WORK

This paper presents efficient fault tolerant adder/subtractor in terms of gate count, constant input, garbage output and quantum cost. The proposed design can work as single unit that can act as adder as well as subtractor depending upon the requirement.

The proposed fault tolerant adder/subtractor can be used to design arithmetic components such as carry save adder, carry skip adder and multipliers.

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