8T SRAM Cell Design for Dynamic and Leakage Power Reduction

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ABSTRACT
This paper addresses a, novel eight transistor (8T) CMOS SRAM cell design to enhance the stability and to reduce dynamic and leakage power. For the validation of proposed 8T SRAM cell, compared results with reported data. The parameters used in the proposed cell are comparable to the existing 8T SRAM cell at same technology and design rules. The stability of the proposed cell has been analyzed using N-curve metrics. Write operation is achieved in the proposed 8T SRAM cell by charging / discharging single Bit Line (BL), which results in reduction of dynamic power consumption. The proposed 8T SRAM cell has achieved 38.33% dynamic power reduction and 25.31% reduction in leakage power comparing with the reported data of 8T SRAM cell, which validate the desired design approach.

Keywords
Dynamic power consumption, leakage power, N-curve, SNM, SRAM.

1. INTRODUCTION
The portable devices such as hand held mobile devices and personal digital assistants are gaining more popularity as well as making changes in every aspect of our daily lives. The major concern enhancing the demand for portable device market is multimedia data processing, which includes the image/video applications [1]. Video applications require a large amount of embedded memory access, which results in significant power consumption and thus limits the battery life time. Power dissipation has become an important consideration due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances [2]. Low power design is a, buzzword these days and designing with low power requirements has been always an important aspect of video applications. The overarching reason why the low power design is becoming so important today is the increase of leakage current with the shrinkage of device dimension. Low power design is indispensible to realize battery operated systems. Due to the limited size of handheld devices, it is impossible to use larger batteries in it and short battery life time of a smaller battery limits the use of them [3].Therefore low power design is essential to extend the battery life time. Most of the digital devices consists of memories and hence reducing power consumption of memories as well as area reduction is paramount important as of today to improve system performance, efficiency and reliability. One of the effective ways to reduce the dynamic power consumption is lowering the operating voltage due to its quadratic relationship [4]. In scaled technologies maintaining high SRAM yield becomes more challenging since they are particularly vulnerable to process variations due to the minimum sized devices used in SRAM bit cells [5].

The amount of embedded SRAM in modern Systems on-Chips (SoC) increases to meet the performance requirements in each technology generation [6]. As the International Technology Roadmap for Semiconductors (ITRS) predicts, memory area is becoming 90% of the total chip area [7]. This trend is continuing also for real time video System on Chip (SoC). Two aspects are important for SRAM cell design: (i) the cell area and (ii) stability of cell. In today's technology power dissipation in the memory circuits has become an important design consideration. As technology scaling, more devices are integrated into the system, as a result the corresponding leakage power increases. Lower voltages and smaller device dimensions have a significant effect on data stability, dynamic power consumption and leakage power in SRAM cell [8].

The rest of this paper is organized as follows: section 2 briefly presents the bulk CMOS 6T SRAM cell and its failures. Section 3 presents the 8T SRAM cell reported in [9]. In section 4, describes the proposed 8T SRAM cell and analyze its effectiveness. Section 5 discusses the stability metrics. Section 6 discusses the experimental conclusion between the cell presented in [9] & proposed cell, and finally some conclusions are drawn in section 7. In this work 65nm technology used for the simulation of all results.

2. 6T SRAM CELL DESIGN
As shown in figure 1, 6T SRAM cell design uses bi-stable latching circuitry to store a bit (M1, M2, M5 & M6) and two access transistors (M3 & M4). Word Line (WL) is connected to the access transistors at their respective gate terminals. WL is used to select the cell. Source/Drain terminals are connected to the Bit Lines (BL & BLB), which are used to perform the read and write operations on the cell [5]. The problem associated with bulk MOSFET based 6T SRAM cell during read operation is, when the WL is turned ON , it raises the output voltage at node that stores '0', which could turn ON the opposite inverter pull down transistor, when this happens the voltage at node which stores '1' will be reduced. This voltage may drop little, but it should not drop below the threshold voltage. If it drops below the threshold voltage of MOSFET, it leads to read destructive operation. Due to this stability of the 6T SRAM cell will be degraded. The operation of writing is accomplished by forcing one bit line low while other bit line remains at about V_{dd},which could leads to enhancement in dynamic power consumption. With technology scaling, in the new coming manufacturing process the operating voltage and threshold voltage decrease and it demolishes the stability of the SRAM cell. Due to the direct paths between bit lines to the storage nodes, the data stored in conventional SRAM cell easily deteriorated by the external noise.
Based on the above reasons bulk MOSFET based 6T SRAM cell is not suitable for real time video applications [10]. Hence we require a new design for high stability, low dynamic and leakage power.

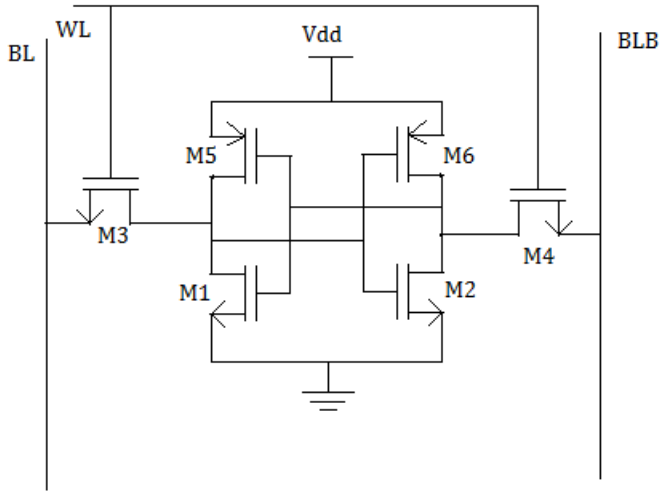


Fig 1: conventional 6T SRAM cell.

3. REPORTED 8T SRAM CELL DESIGN

To address the read destructive problem, the read and write operations are separated by adding transistor stack to the conventional 6T SRAM cell, thus it has the area penalty but operates efficiently than the 6T SRAM cell at lower V_{dd}. The 8T SRAM circuit described in this section [9]. The schematic of the 8T SRAM cell with transistors sized for a 65-nm CMOS technology shown in fig. 2.

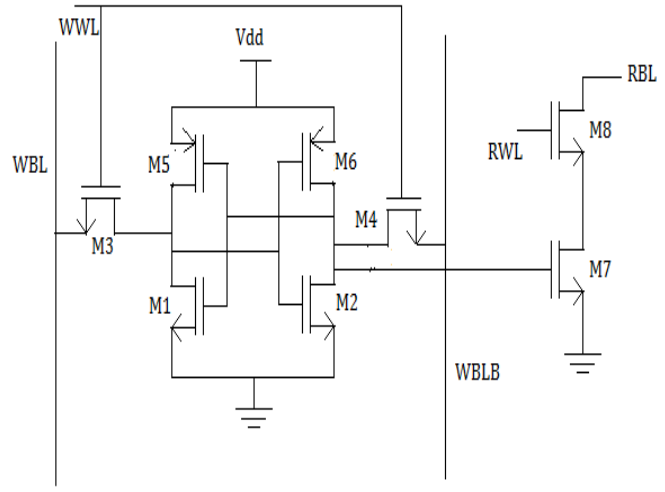


Fig 2: Reported 8T SRAM cell

The disturbance of bit lines during read operation is the primary source of instability problem in SRAM operation. The stability in 8T SRAM cell can be enhanced by isolating the read port from the write bit lines. The 8T SRAM cell composed of conventional 6T SRAM cell for writing operation and a transistor stack, which can be used for read operation. The read and write operations are controlled by separate signals Write Word Line (WWL) and Read Word Line (RWL). During the read operation Read Bit Line (RBL) is pre charged to V_{dd} and WWL is maintained at V_{GND}. Depends on the value stored in cross coupled inverters RBL, discharges (or) maintained at V_{dd}. If RBL discharges, it can be treated as the stored bit is '1', otherwise it is '0'. The storage nodes are completely isolated from the write bit lines, which can increases the stability of the SRAM cell. During the write operation WBL and WBLB lines are pre charged to predetermined values. Then, asserting the write word line WWL and nodes attain the corresponding values from the bit lines. It uses the two additional Word Lines to perform read and write operations, when compared with 6T SRAM cell, which could increase the metal density, wire delay and dynamic power consumption and leakage power [9], [11].

4. PROPOSED 8T SRAM CELL DESIGN:

A novel 8T SRAM cell structure to reduce the leakage current and dynamic power consumption has been reported in this work . The schematic of proposed 8T SRAM cell at 65nm technology is as shown in fig. 3. The proposed SRAM cell composed of write access transistor (M3), controlled by Write Word Line (WWL) and read access transistor (M8) is controlled by the Read Word Line (RWL). During the write operation WWL is transitions to high value and RWL and BLB both are maintained at V_{GND}. Hence, the read access transistor (M8) cut OFF. To write '1' into the cell Bit Line (BL) is pre charged to a high value, then '1' is forced through the write access transistor (M3). Similarly, to write '0' into the cell, BL is discharged. Hence, to perform write operation the proposed cell utilizing single BL, which could leads to reduction in the dynamic power consumption and leakage power.

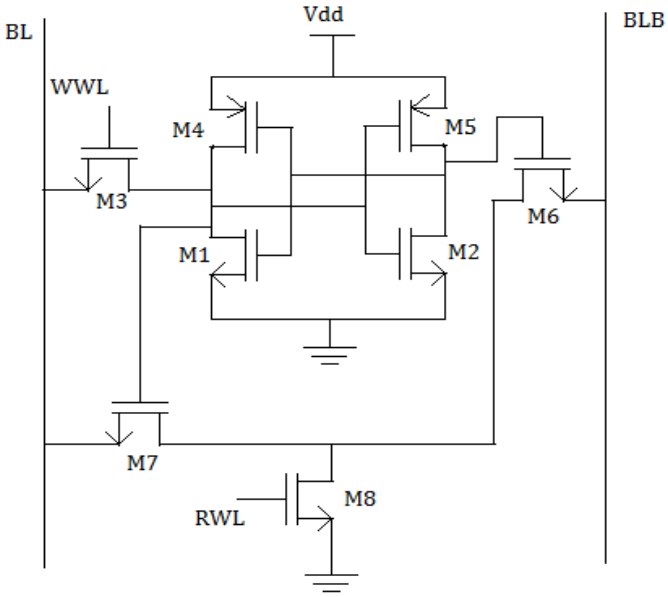


Fig 3: Proposed 8T SRAM cell design

During read operation, RWL is transition to high value and WWL is maintained at V_{GND}. Hence the write access transistor is cut OFF. Prior to read operation BL and BLB are pre charged to V_{dd}. Assume that '1' is stored left and '0' is stored right side, then BL discharged through M7 and M8. Since, 'M6' is cut OFF there is no path to discharge the BLB. Hence BLB is held at high value. Alternatively, if '1' is stored right side, BLB is discharged through 'M6' and 'M8'. Since, 'M7' is cut OFF there is no path exists to discharge the BL. Hence, it can maintain at high value.
With this, storage nodes completely isolated from the Bit Lines (BL) during read operation, hence stability increases significantly.

5. STUDY OF STATIC NOISE MARGIN

5.1 Stability analysis using Butterfly Curve

The immunity of SRAM cell to static noise is expressed in terms of Static Noise Margin (SNM). It is defined as the maximum value of the DC noise voltage that can be tolerated by SRAM cell without altering the stored bits [8]. Graphically, the SNM of SRAM cell can be obtained by drawing the DC characteristics of cross coupled

inverters. The voltage transfer characteristic (VTC) of one inverter is super imposed over the inverse VTC of the other cell. The resulting two-lobed graph is called as "butterfly curve". Then, finding the maximum possible square between them [12]. The side length of the square is considered as SNM. As the technology scaling, cell becomes less stable with lower operating voltage, increasing leakage currents. The SRAM Cell becomes less stable during read operation as shown in fig. 4, because of the voltage dividing effect at the inverter which store '0', will be pulled up. The drawback of the SNM metric using butterfly curve is that it does not contain automatic in-line testers. To measure the Static Current Noise Margin (SINM), still it requires mathematical manipulation from the measured data.

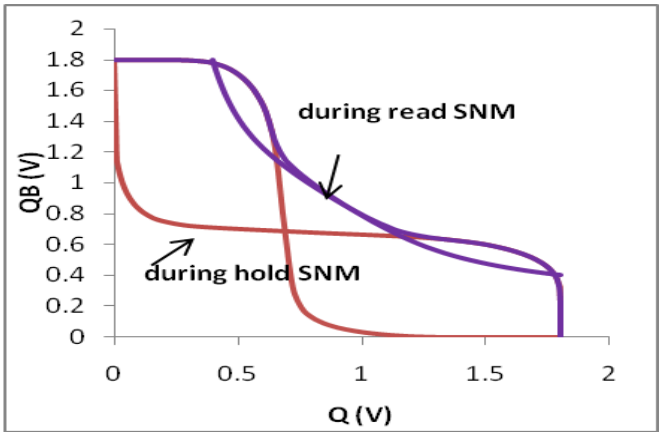


Fig 4: Static Noise Margin (SNM).

5.2 Stability Analysis Using N-Curve:

The N-curve contains the information of both read stability and write ability, thus it overcomes the limitations of SNM metric using butterfly curves [13]. The N-curve gives the complete functional analysis of SRAM cell in a single simulation. A typical N-curve is shown in fig. 5 to describe the important parameters, which are useful to analyze the stability of the SRAM cell.

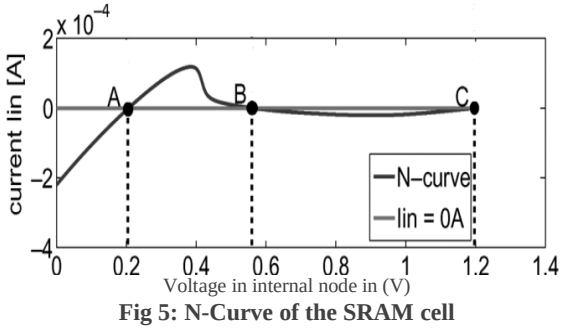


Fig 5: N-Curve of the SRAM cell

The voltage between the points 'A' and 'B' indicates the Static Voltage Noise Margin (SVNM). It can be defined as the maximum tolerable DC noise voltage at the input of the inverter of the SRAM cell before its content changes. The additional current information provided by the N-curve, namely the peak current located between the points 'A' and 'B', this current metrics is called as the Static Current Noise Margin (SINM). It can be defined as the maximum value of DC current that can be injected in the SRAM cell before its content changes [13] . The SRAM N-curve also provides the information regarding the write ability of the cell. Write Trip Voltage (WTV) is the voltage drop needed to flip the internal node '1' of the cell with both the bit lines clamped V_{dd}. It is given by the voltage between the second 'B' and last zero crossing point 'C'. Write Trip Current (WTI) is defined as the amount of current need to write the cell when both bit lines are clamped at V_{dd} [15]. The peak value of I_{in} after the second zero crossing of N-curve gives WTI. For better read stability SVNM & SINM are should be larger. For better write ability WTI are should be smaller.

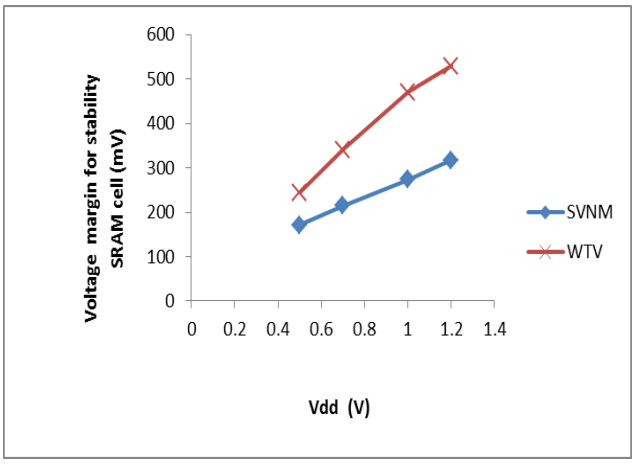
6. RESULTS AND DISCUSSION

This section presents the simulation results of bulk MOSFET based 6T SRAM cell, reported 8T SRAM cell and proposed 8T SRAM cell. We have found the stability metrics using N -curve at different voltages for bulk CMOS 6T SRAM cell and observed that at lower voltages the stability metrics has been reduced , which is shown in Table I.

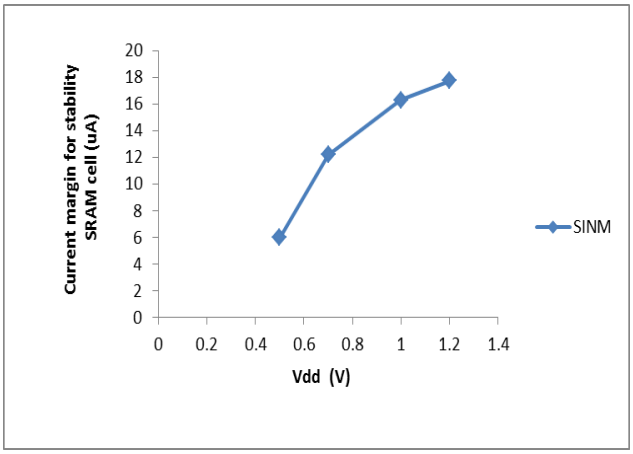
Table-I: Stability Metrics using N- Curve

$V_{dd(V)}$	SVNM (mV)	SINM (µA)	WTV (mV)	WTI (µA)
1.2	317.52	17.72	529.18	-10.41
1	274.25	16.28	470.93	-8.85
0.7	214.8	12.18	340.63	-3.315
0.5	171.03	5.984	244.71	-0.745

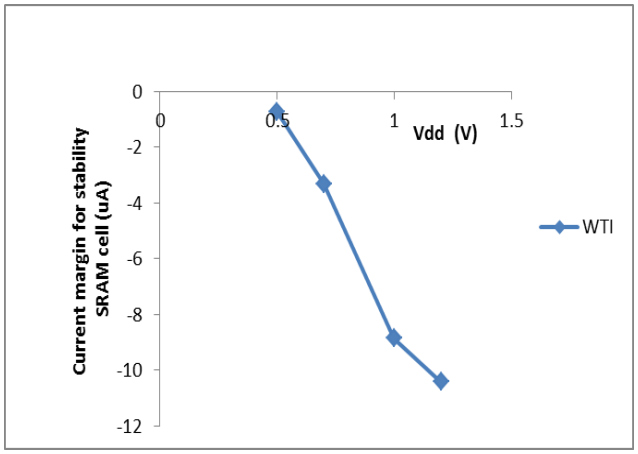
From the N-curve definitions, for read stability and write ability of the SRAM cell, we can draw some conclusions with respect to theV_{dd}. By decreasing the V_{dd} the read stability N-curve metrics degraded. Therefore, the stability of the cell is limited by the V_{dd} scaling. The SINM can be enhanced for lower V_{dd} by increasing the transistor widths, which of course, is at the expense of area. Fig. 6(a), 6(b) & 6(c) shows that an increase in V_{dd} positively affects the read stability. To overcome the read destructive operation the value of the SVNM should as large as possible.



(a)



(b)



(c)

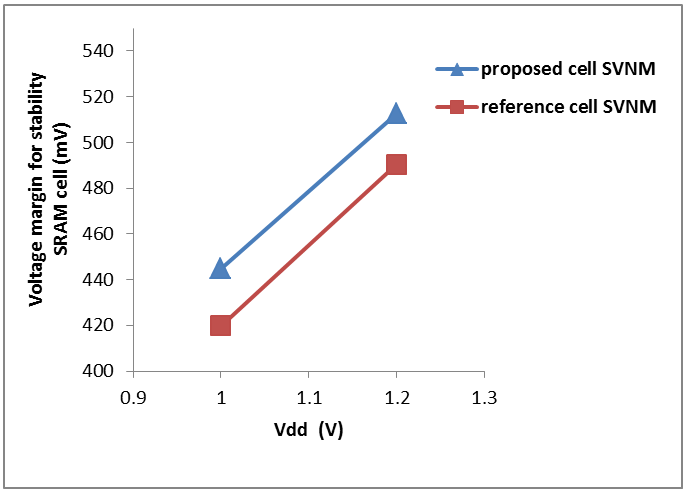
Fig 6 : (a) SVNM and WTV metrics of the SRAM cell versus the supply voltage V_{dd}. (b) & (c) SINM and WTI metrics of the SRAM cell versus the supply voltage V_{dd}. All the N-curve metrics degrade with lower V_{dd}.

The cell is designed for 1V & 1.2V power supply for the analysis of stability metrics using N-curve for both reference SRAM cell and proposed SRAM cell. The proposed cell got the improved results, which is shown in Table II.

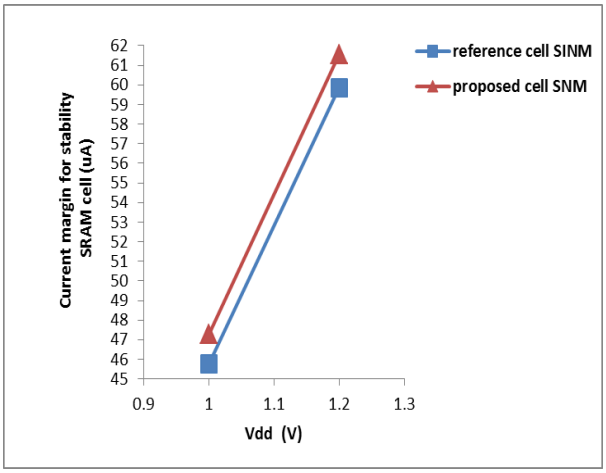
Table-II: Stability Metrics using N- Curve

Parameter	Reference cell at 1V	Proposed cell at 1V	Reference cell at 1.2V	Proposed cell at 1.2V
SVNM (mV)	419.74	444.78	490.51	512.64
SINM (µA)	45.75	47.26	59.87	61.56
WTV (mV)	539.5	541	659.4	662.3
WTI (µA)	-25.65	-27.79	-38.81	-40.83

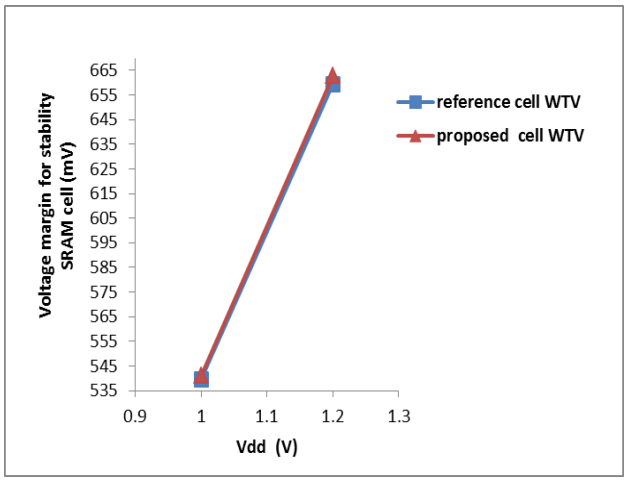
Fig. 7(a), 7(b), 7(c) & 7(d) shows the comparison between reference cell and proposed cell. Proposed achieved the improved results in terms of SVNM, SINM, WTV & WTI .



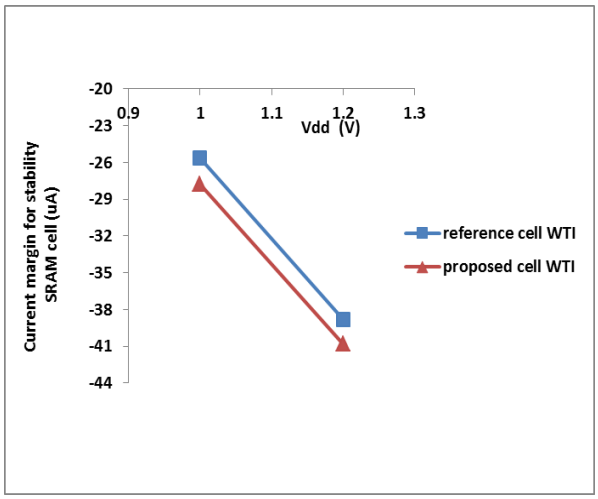
(a)



(b)



(c)



(d)

Figure 7: (a),(b),(c) & (d) are SVNM, SINM, WTV, WTI metrics of proposed and reference SRAM cells respectively versus power supply voltage V_{dd}.

Dynamic Power and Leakage Power :

Dynamic power consumption will be increased by using both the bit lines during write operation. By reducing the switching activity and clock frequency, dynamic power can be lowered but it degrades the performance [14, 16]. The proposed 8T SRAM cell reduces the dynamic power 38.33% and leakage power 25.31%.

Table-III: comparison between reference cell and proposed cell for dynamic and leakage power

parameter	Reference cell at 1V	Proposed cell at 1V
Dynamic power consumption	5.66µW	3.49µW
Leakage Current	10.98nA	8.2nA

7. CONCLUSION

The proposed novel 8T SRAM cell performs the write operation using a single bit line to reduce the dynamic power consumption. The proposed SRAM cell is suitable for real time video applications for statistically similar data. The measurement result of proposed cell verifies a dynamic power saving of 38.33%. The leakage power is reduced by 25.31%. Analyzed the stability metrics using N-curve, which gives the information about read stability and write ability. In future the leakage current reduction techniques can be applied to the proposed SRAM cell to further reduce the leakage current. The proposed 8T SRAM cell can be integrate with the conventional 6T SRAM cell, the human visual system is mostly sensitive to higher bits of luminance pixels in video data. The preferential policy can be used to store the bits, where the higher order luma bits are stored in proposed 8T SRAM bit cells while the lower order bits are stored in conventional 6T bit cells.

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