A SRAM Memory Cell Design in FPGA

Venmathi V.
PG Scholar, Department of EEE,
SNS College of Engineering,
Coimbatore, India

C. Vivekanandan, Ph.D
Professor and Vice Principal
SNS College of Engineering,
Coimbatore, India

Abstract

The main objective of this work is to design a memory cell in Field Programmable Gate Array (FPGA) that consumes lesser power with reduced delay constraint. In the existing system, the FPGA is based on 10T Static Random Access Memory (SRAM) cell configuration in which power consumption is relatively high. The proposed work includes a Self controllable Voltage Level (SVL) circuit along with 10T SRAM cell and asynchronous counters in read circuit memory block instead of shift registers. The stand-by leakage power of 10T SRAM is reduced by incorporating a newly-developed leakage current reduction circuit called SVL circuit, with minimal overheads in terms of chip area and speed, which retains data in standby mode. In asynchronous counters, external clock is connected to the clock input of the first flip-flop only, whereas the successive flip-flops change when it is triggered by the falling edge of the previous counterparts. The various FPGA components are implemented in 180nm technology to evaluate the FPGA performance. Parameters like average power consumption and power delay product are compared with the existing system and it is found that the proposed system consumes lesser power but at the cost of the power delay product. The software tool used for design and simulation of various FPGA components is TANNER S-Edit.

Keywords

10T SRAM, FPGA, nm technology, Self controllable Voltage level circuit (SVL).

1.INTRODUCTION

Power consumption concerns came into play with the appearance of the first portable electronic systems in the late 1980s. In this market, the battery lifetime is a decisive factor for the commercial success of the product. Another fact that became apparent at about the same time was that the increasing integration of more active elements per die area would lead to prohibitively large-energy consumption of an integrated circuit. A high absolute level of power is not only undesirable for economic and environmental reasons, but it also creates the problem of heat dissipation. In order to keep the device working at acceptable temperature levels, excessive heat may require expensive heat removal systems. These factors have contributed to the rise of power as a major design parameter on par with performance and die size. In fact, power consumption is regarded as the limiting factor in the continuing scaling of CMOS technology.

Low-power VLSI design is becoming a key issue in designing battery driven circuits, high performance digital systems and also for storage circuits. It is said that memories, the core section of digital circuits, are the major customers of power in any digital system. Memory blocks consist of Static Random Access Memory (SRAM) cells. The power consumption and speed of SRAMs are the two important issues to be considered while designing low power VLSI circuits. The power consumption of digital CMOS circuits is generally considered in terms of three components. They are 1) dynamic power component, related to the charging and discharging of the load capacitance at the gate output. 2) short-circuit power component, related to the transition of the output line (of a CMOS gate) from one voltage level to the other, there is a period of time when both the PMOS and the NMOS transistors are on, thus creating a path from V_{DD} to the ground, thus creating short circuit may be for a quiet small duration 3) static power component, related to leakage present even when the circuit is not switching.

The first objective of this paper is to analyze the available different structures of SRAM cells and to identify the structure that consumes relatively lesser power compared to the conventional structures of the same technology. The second and major objective of this work is to determine a strategy to minimise the power consumption further. The proposed modification is to be validated using an FPGA. There are different types of techniques available for reducing power consumption in memory cells and after the exhaustive survey it is found that the SVL circuit consumes lesser power than other configurations.

The Differential 10T cell is available as one of the memory cell consists of two NMOS transistors for the Read Bit Line (RBL) and two additional NMOS transistors for inverted RBL are added to the conventional 6T SRAM memory cell. It operates faster when compared to a single end 10T SRAM and in terms of power efficiency the recharge circuit leads to power overhead [3]. The Differential 10T cell proposed by Chang et al (2008) includes read disturb free operation which improves readability and write stability, but leakage current is found to be relatively high. The 12T SRAM cell uses a simple latch to connect to a bit line and also includes two additional NMOS transistors. The average power consumption of 12T SRAM is high when compared to SVL technique.

There are two well known techniques available for reducing stand-by power (P_{st}). One is to use a multi-threshold voltage CMOS (MTCMOS). This technique reduces P_{st} by disconnecting the power supply through the use of p-MOSFET switches (SWs) with higher threshold voltage (V_{th}). However, it has serious drawbacks such as the need for additional fabrication process for higher V_{th} and the fact that storage circuits based on this technique cannot retain data[7]. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) which reduces leakage current by increasing substrate-bias (V_{sub}). This technique also faces some serious problems, such as very low substrate-bias controlling operation, large area penalty and large power penalty due to substrate-bias supply circuits. To decrease the average power consumption, a SVL circuit is employed in this paper. There are three types of SVL circuit. Type I has an upper SVL circuit, Type II has a lower SVL circuit and Type III combines both upper SVL circuit and lower SVL circuit. In this paper Type III is used, to achieve total reduction in leakage current.

CMOS logic is a technology for constructing integrated circuits that has high noise immunity and low static power consumption. FPGA is an integrated circuit which can be used to implement any logical function [6]. The most common FPGA architecture consists of an array of logic blocks (called Configurable Logic Block, CLB, or Logic Array Block, LAB, depending on vendor), I/O pads, and routing channels. A logic block (CLB or LAB) consists of a few logical cells. A typical cell consists of a 5-input LUT, a multiplexer and a D flip flop. In the read circuit memory block, 32 memory cells are present and each memory cell consists of 10T SRAM cells. The proposed work includes a leakage current reduction circuit in the memory cell.

The rest of the paper is organized as follows: Section 2 explains the operation of single end 10T SRAM cell and the read circuit in the memory block. Section 3 explains the operating principle of proposed SVL circuit where single end 10T SRAM cell is the load circuit. Section 4 explains the logic element and its function. Section 5 explains FPGA. In Section 6 we compare the simulation results of average power consumption obtained from existing and proposed work

2. MEMORY BLOCK

2.1 Operation of Single End 10T SRAM Cell

SRAM is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The schematic diagram of 10T SRAM cell is shown in the Figure 1 consists of a 6T SRAM cell, a CMOS Inverter and a transmission gate. The inputs for the memory cell include Read Word Line (RWL), Read Word Line inverse (RWL_N), Write Word Line (WWL) and Write Bit Line (WBL). The outputs are Write Bit Line inverse (WBL_N) and Read Bit Line (RBL). When WWL=1, the NMOS transistors i.e., N1 and N4 turns ON and when WBL=0, the transistors on the upper half of the cross coupled inverters i.e., P2 and P3 transistors turns ON and a *write 0* operation is performed and gives WBL_N=0. The value '1' is given as input to CMOS Inverter to produce the value '0'. When RWL=1 and RWL_N=0, the value '1' is given to the transmission gate to produce the value '1' again without any loss of attenuation and a *read 1* operation is performed. Simultaneously, a *read 1* operation and a *write 0* operation are performed for WBL=1.

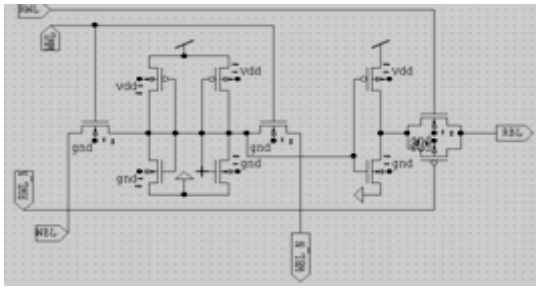

Figure 1 Schematic Diagram for 10T SRAM cell

2.2 Read Circuit In Memory Block

The read circuit in memory block consists of a shift register, and gate, inverter and memory cell as shown in the Figure 2. In read memory circuit the input signals are *d, clk*, Write Enable (w_ en) and Read Enable (r_en) and the output signals are Read Word Line (RWL), Write Word Line (WWL), Write Bit Line (WBL) and Write Bit Line inverse (WBL_N). The first NAND gate requires the d and R_en inputs whereas the second NAND gate requires the d and W_en input. The output value from the NAND gate is given to the corresponding inverter and the values produced from the input value for the memory cell to produce the required output values [8].

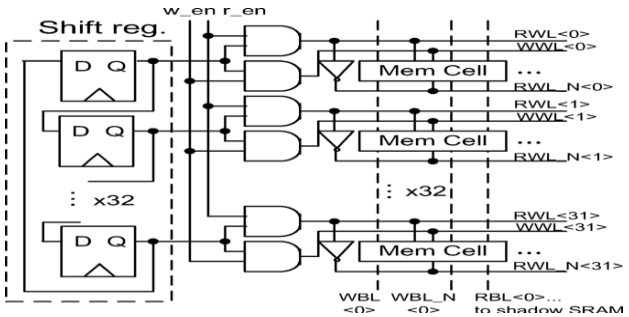

Figure 2 Read Circuit In Memory Block

3. PROPOSED WORK

3.1Operating Principle of SVL Circuit

The Type III SVL circuit along with 10T SRAM cell is shown in Figure 3. The upper SVL consists of a single p-MOSFET switch (p-SW) and m n-MOSFET switches (n-SW) connected in series. The "on p-SW" connects a power supply (V_{DD}) and load circuit in active mode, and "on n-SW" connect V_{DD} and load circuit in standby mode. Similarly, the lower SVL circuit consists of single n-MOSFET switch (n-SW) and m p-MOSFET switch connected in series, is located between a ground level (V_{SS}) and the load circuit. The lower SVL circuit not only supplies V_{SS} to the active load circuit through the "on n-SW" but also supplies V_{SS} to the standby load circuit through the use of the "on p-SWs".

The gate voltage is kept at 0, the p-MOSFET is turned on and n-MOSFET is turned off. When the control signal turns on n-SW and turns off p-SW, V_{DD} is supplied to the load circuit through m n-SWs. Thus, a drain to source voltage can be expressed as $V_{dsn} = V_{DD} - mv$, where v is the voltage drop of the single n-SW and can be changed by varying m or v. Decreasing V_{dsn} by increasing mv will increase the barrier height of the "off n-NMOS" that is it will decrease the drain induced barrier lowering (DIBL) effect and therefore increases V_{thn}. This results in a decrease in the subthreshold current of the n-MOS (I_{dsn}) that is the leakage current through the load circuit decreases. A negative control signal turns on p-SW and turns off n-SW so that V_{SS} is supplied to the load circuit, thus reduced V_{dsn} and reduces I_{stn}. Furthermore, source voltage is increased by mv, so the substrate bias is expressed by $V_{sub} = -mv$ is increased. Both the reduction in the DIBL effect and the increase in the back gate bias leads to further increase in $V_{thn.}$ The DIBL effect of on n-MOS by incorporating Type III SVL decreases V_{dsn} further. This technique not only retains data but also produces high noise immunity [7].

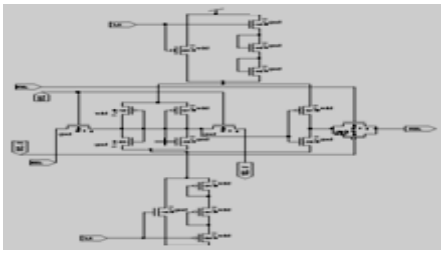

Figure 3 10T SRAM Cell With SVL Circuit

4. LOGIC ELEMENT

The Schematic Diagram of Logic element shown in the Figure 4 contains a five-input LUT, four D flip-flops (DFFs), and several crossbars. A shift register lookup table, also shift register LUT or SRL, is used in FPGA devices. It is essentially a shift register of variable length. The length of SRL is set by driving address pins high or low and can be changed dynamically, if necessary. Different conventional FPGA designs that have only one DFF in each LE, our design includes four. The reason is that, when logic folding is performed, many temporary computation results need to be stored to make easy inter stage communications. The 3-to-1 crossbar select signals to be latched, and the 5-to-1 crossbars determine the output signals of the LE from the LUT or DFFs. The crossbars are constructed using NMOS and PMOS transistors along with the select lines. Among the four LE outputs, two are connected to the interconnection network through the CB and form part of the LB output, while the other two LE outputs are fed back through the local switch matrix to the local Les [8].

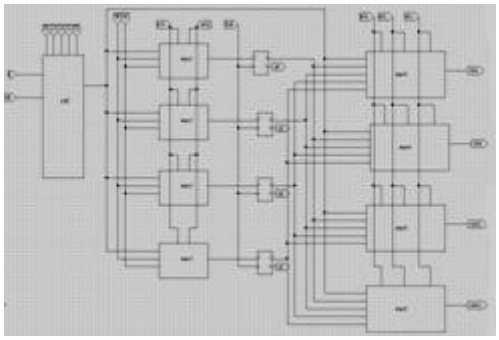

Figure 4 Logic Element

5. FPGA

The FPGA is an integrated circuit which can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (not withstanding the generally higher unit cost), offer advantages for many applications. FPGA contains programmable logic components called logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together. The logic block of an FPGA can be configured in such a way that it can provide functionality as simple as that of the transistor or as complex as that of a microprocessor. It can used to implement different combinations of combinational and sequential logic functions [6]. An LB has eight logic elements (LEs) and a local switch matrix. The LEs performs the logic computations. Since logic folding localizes most of the on-chip communications, the local switch matrix is designed to assist high-speed local communications among LEs. A LE has six inputs, which are selected through the switch matrix. To provide to the 48 inputs needed for the LEs, the local switch matrix designs with 48 56-to-1 bit multiplexers (MUXs), selecting signals from 40 common inputs of the LB and 16 feedback signals (2 feedback signals per LE). The 40 common inputs arrive from the interconnection network outside the LB, and connect to the local switch matrix through CBs. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory [8]. CMOS logic is a technology for constructing integrated circuits that have high noise immunity and low static power consumption.

6. SIMULATION AND RESULTS

The FPGA architecture of the proposed SVL memory cell has been analysed in detail and simulated using Tanner tool version 7. Tanner Tool provides fast, easy creation and editing of circuit schematics and also supports a technology-independent design methodology, allowing the user to choose a specific technology and vendor after completing the design. The circuit is characterized by using the 180nm technology with a supply voltage of 1.8volts. The functionality verification of the designed circuits is done on the Tanner tool. Schematic of the simulation stages is designed using S-Edit and netlist simulation are done by using T-spice and waveforms are analyzed through the W-edit. Both the existing and proposed models have been simulated. The different modules of the proposed stages include 10T SRAM Memory Cell with SVL circuit, Read Circuit in Memory block, Logic Element and FPGA.

The following are the various input parameters used for the simulation stages

- DC Voltage: 1.8V
- Pulse Width: 10µm
- Length: 5µm
- Height: 5µm
- On value: 1.8V
- Off value: 0
- CMOS Technology used: 180nm technology

The table 6.1 shows the average power consumption and the power delay product between the existing and proposed technique among various simulation stages in the memory cell, read circuit in memory block, logic element and FPGA. The appreciable improvement in power consumption is evident from the first section of the comparison table for the memory cell, read circuit in memory block and FPGA. However, with respect to Logic element the power consumption and power delay product remains same. In the second section of the comparison table, the power delay product or speed up product is high when compared to existing technique.

Table 6.1 Power Results

STAGES	AVERAGE POWER CONSUMPTION (Watts)		POWER DELAY PRODUCT (Joules microsecond)	
	EXISTING	PROPOSED	EXISTING	PROPOSED
MEMORY CELL	3.4237	0.14638	1.1974×10^{-3}	1.93722×10^{-3}
READ CIRCUIT IN MEMORY BLOCK	16.022	0.05606	2.2722×10^{-3}	4.96421×10^{-3}
LOGIC ELEMENT	0.1855	0.1855	5.8731×10^{-4}	5.8731×10^{-4}
FPGA	0.5037	0.01958	1.4803×10^{-3}	4.2763×10^{-3}

7. CONCLUSION

In this paper, 10T SRAM cell with SVL circuit has been proposed for low power operation and asynchronous circuits were used for high speed operation. Asynchronous circuits in read circuit increases the speed for computation and therefore delay is reduced. The SVL circuit overcome the problems by dynamically reducing drain source voltages and by increasing the substrate bias of "off MOSFETs". The stand by leakage power of SRAM memory cell architecture based on SVL is reduced. Since the leakage power is an important portion of total power in sub threshold logic, leakage reduction provides considerable total power saving. This results in emergence of portable and high performance computing devices with huge storage needs. Advantages of using SVL circuit include high noise immunity, data retentions in standby mode and also provides high speed operation. The simulation results show that the total power consumption is less when compared to the existing single end 10T SRAM cell. The software tool used to design and simulate the various FPGA components is TANNER S-Edit and implemented in 180nm Technology. It is thus concluded that the developed SVL circuit will play a major role in future CMOS logic circuits and memories.

FUTURE WORK

The various simulation stages like memory cell with SVL circuit, read circuit, Logic element and FPGA was simulated using TANNER tool version 7. It was found that the average power consumption was less when compared to the existing system but the power delay product was relatively high. Since power delay product also plays a vital role in terms of performance, it has to be reduced. This paper may be extended to reduce power delay product by using some other techniques.

REFERENCES

[1] Do Anh-Tuan, Jeremy Yung Shern Low, Joshua Yung Lih Low, Zhi-Hui Kong, Xiaoliang Tan, and Kiat-Seng Yeo An 8T Differential SRAM With Improved Noise Margin for Bit-Interleaving in 65 nm CMOS IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 58, NO. 6, JUNE 2011

[2] H. Noguchi, S. Okumura, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, and M. Yoshimoto, "Which is the best dual-port SRAM in 45-nm process technology? — 8T, 10T single end, and 10T differ-ential," inProc. IEEE Int. Conf. Integr. Circuit Design Technol., Jun.2008, pp. 55–58

[3] H. Noguchi, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, and M. Yoshimoto, "A 10T non-precharge two-port SRAM for 74% power reduction in video processing," inProc. IEEE Comput. Soc. Annu. Symp. VLSI, 2007, pp. 107–112

[4] I. Chang, J.-J. Kim, S. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM array with bit-interleaving and differential read scheme in 90nm CMOS," inProc. Int. Solid State Circuits Conf., Feb. 2008, pp.628–629

[5] Laxmi singh, Ajay Somkuwar, "Dynamic Random Access Memory with Self-controllable Voltage Level to reduce low leakage current in VLSI" Vol. 3, Issue 1, January - February 2013, pp.1893-1897

[6] I.Kuonand J.Rose,"Measuring the gap between FPGAs and ASICs," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 26, no. 2, pp. 203–215, Feb. 2007

[7] Tadayoshi Enomoto, Yoshinori Oka, Hiroaki Shikano, and Tomochika Harada Chuo University, Faculty of Science and Engineering, Tokyo, Japan, A Self-Controllable-Voltage-Level (SVL) Circuit for Low-Power, High-Speed CMOS Circuits".

[8] Ting-Jung Lin, Wei Zhang, and Niraj K. Jha, "SRAM-Based NATURE: A Dynamically Reconfigurable FPGA Based on 10T Low-Power SRAMs" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1