International Journal of Computer Applications (0975 – 8887)
Volume 70– No.21, May 2013

Design and Performance Comparison of 6-T SRAM Cell in 32nm CMOS, FinFET and CNTFET Technologies

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ABSTRACT

In most of the digital circuits, CMOS based design is allowed to be used in practice. Generally, CMOS stands for Complementary Metal Oxide Semiconductor Field Effect Transistor, that is, considered to be as combination of both PMOS as well as NMOS. In CMOS based design, symmetry should be followed in circuit operation. Most of the complex circuits are allowed to design in CMOS, however, there are several drawbacks present in this complementary based design. Also, SRAM cell read stability and write-ability are major concerns in nanometer CMOS technologies, due to the progressive increase in intra-die variability and supply voltage scaling. Therefore, it is necessary to find alternative way suitable for particular design, instead of CMOS. Most of the modern design is based on Carbon nanotube FET or FinFET because of its superior properties interms of power consumption, leakage power, delay etc. The objective of this work mainly focus on designing 6-T SRAM cell in 32nm CMOS, CNTFET as well as FinFET and finally, to compare the parameters such as average power, delay and leakage current.

General Terms

Design, Digital Circuits, Nano Technology, VLSI

Keywords

Carbon nanotube, CMOS, Data Retention, FinFET, Static RAM.

1. INTRODUCTION

From the past decades, CMOS scaling in the VLSI circuits has offered improved as well as better performance from one technology node to the another. However, as device scaling moves beyond the 32nm node, significant technology challenges will be faced. Currently two of the main challenges are: the considerable increase of standby power dissipation and the increasing variability in device characteristics which in turn affects circuit and system reliability [1],[2]. To enable future technology scaling, new device structures for next-generation technology have been proposed. The most promising ones so far include carbon nanotube field-effect transistors (CNFETs), FinFETs, nanowire FETs, III/V compound-based devices, graphene nanoribbon devices, resonant tunneling diodes, and quantum dot devices. Many of these devices have been shown to have favorable device properties and new device characteristics, and require new fabrication techniques [3] and these devices are more efficient for digital circuit design. Static 6-transistor (6T SRAM Cell) full-complementary memory cells are most preferably used in memory designs to satisfy requirements for short access- and cycle times, high frequency data rates, low power dissipation, radiation hardness, operation in space, high-temperature, noisy and other extreme environments [4]. In a 6-T Static RAM cell , the two cross-coupled PMOS pull-up devices retain the value written into a cell. These two cross-coupled p-devices are designed to be strong enough to retain a value in the cell indefinitely without any external refresh mechanism [5]. However, if the p-devices are too weak due to a fabrication defect or a connection to either of the p devices is missing, the static RAM cell will no longer be able to hold its data indefinitely [6],[7]. The resulting fault in defective cell is referred to as a data retention fault or a cell stability fault, depending its on severity. Thus all static RAMS require some form of data retention and cell stability testing.

Traditionally, testing large static CMOS memory arrays for data retention faults and cell stability faults has been a time consuming and expensive effort. Existing test methods have also been partial in their test coverage. The algorithmic test methods currently used for detecting these faults are primarily functional in nature; that is they check the cell stability or retention in a functional manner. These algorithmic test methods are time consuming and require extensive characterization of silicon to determine the worst case test conditions. The following functional tests are commonly used by memory manufacturers [8]:

Read disturb: Write a background to the array, then read the array at a lower or higher Vcc but ignore the data (i.e. tester strobe disabled), thereafter read the array to determine if any cell has changed state.

Long Write: Write a background to the array, then perform a long write on a row, then read all other rows of the array to determine if any cell has changed state. Repeat for all rows in the array.

Pause (Data Retention): Write a background to the array, then after a pause on the order of 100 ms read the array to determine if any cell has changed state.

2. READ STABILITY AND WRITE ABILITY OF SRAM CELL

2.1 SRAM Cell Read Stability

Data retention of the SRAM cell, both in standby mode and during a read access, is an important functional constraint in advanced technology nodes. The cell becomes less stable with lower supply voltage (V_{dd}), increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the SNM as the maximum value of DC noise voltage(V_n) that can be tolerated by the SRAM cell without changing the stored bit. The two DC noise voltage sources (V_n) are placed in series with the cross-

coupled inverters and with worst-case polarity at the internal nodes of the cell [7],[9],[10].

2.2 Write-Ability of the SRAM Cell

Besides the read stability for the SRAM cell, a reasonable write-trip point is equally important to guarantee the write ability of the cell without spending too much energy in pulling down the bit-line voltage to 0 V. The write-trip point defines the maximum voltage on the bit-line, needed to flip the cell content. The write-trip point is mainly determined by the pull-up ratio of the cell while the read stability is determined by the cell ratio of cell; this results in the well-known conflicting design criteria. The SRAM N-curve can also be used as alternative for the write-ability of the cell, since it gives indications on how difficult or easy it is to write the cell [7],[9],[10].

3.FINFET DEVICES

The physical and electrical characteristics of the FinFETs are presented in this section [3], [11]. The FinFETs used in this paper have a symmetrical structure, as shown in Fig. 1. The physical parameters used for MEDICI simulations in a 32nm FinFET technology are listed in Table 1. VDD is 0.8 V.

Table 1. FinFET Device Parameters

Parameter	Value
Channel length(L)	32nm
Effective channel length(L_{eff})	25.6nm
Fin thickness(t_{si})	8nm
Fin height(H_{fin})	32nm
Oxide thickness(t_{ox})	1.6nm
Channel doping	$10^{15}cm^{-3}$
Source/Drain doping	$2x10^{20}cm^{-3}$
Gates work function(N-type FinFET)	4.5eV
Gates work function(P-type FinFET)	4.9eV

The width of a FinFET is quantized due to the vertical gate structure. The fin height determines the minimum transistor width (Wmin). With the two gates of a single-fin FET tied together, Wmin is

$$Wmin = 2 * Hfin + tsi$$

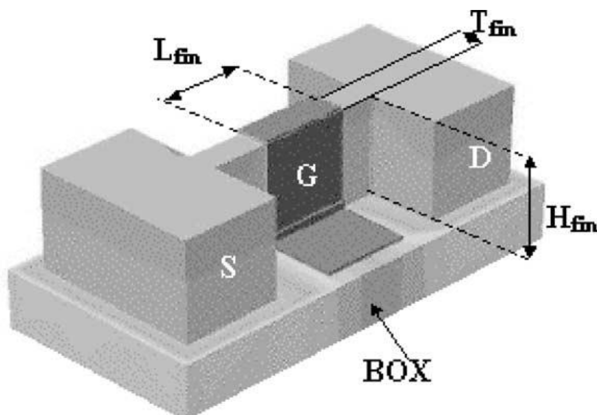


Fig 1. FinFET Device - 3D Configuration

where H_{fin} is the height of the fin and tsi is the thickness of the silicon body as shown in Fig. 1. H_{fin} is the dominant component of the transistor width since tsi is typically much smaller than H_{fin}. Since H_{fin} is fixed in a FinFET technology, multiple parallel fins are utilized to increase the width of a FinFET. The total physical transistor width (Wtotal) of a tied-gate FinFET with *n* parallel fins is

$$W_{total} = n * W_{min} = n * (2 * H_{fin} + T_{si}).$$

The two vertical gates of a FinFET can be separated by depositing oxide on top of the silicon fin, thereby forming an independent-gate FinFET as shown in Fig. 1b. An independent-gate FinFET (IG-FinFET) provides two different active modes of operation with significantly different current characteristics determined by the bias conditions of the two independent gates. In the Dual- Gate- Mode, the two gates are biased with the same signal. Alternatively, in the Single-Gate-Mode, one gate is biased with the input signal while the other gate is disabled (disabled gate: biased with VGND in an N-type FinFET and with VDD in a P-type FinFET). The two gates are strongly coupled in the Dual-Gate-Mode, thereby lowering the threshold voltage (Vth) as compared to the Single-Gate-Mode. The maximum drain current produced in the Dual-Gate-Mode is therefore 2.6 times higher as compared to the Single-Gate-Mode . The switched gate capacitance of the FinFET is also halved in the Single-Gate-Mode due to the disabled back gate. The unique Vth modulation aspect of IG-FinFETs through selective gate bias is exploited in this paper to enhance the SRAM data stability and integration density while lowering the static and dynamic power consumption with minimum sized transistors.

4. CNTFET DEVICES

As one of the promising new devices, CNFET(Carbon Nanotube Field Effect Transistor) avoid most of the fundamental limitations for traditional silicon devices. All the carbon atoms in CNT are bonded to each other with sp2 hybridization and there is no dangling bond which enables the integration with high-k dielectric materials, [12].

4.1 Carbon nanotube

A single-walled carbon nanotube (SWCNT) [13],[14] can be visualized as a sheet of graphite which is rolled up and joined together along a wrapping vector $C_h = n_1a_1 + n_2a_2$, where [*a*1; *a*2] are lattice unit vectors as shown by Fig 1.2, and the indices (n1, n2) are positive integers that specify the chirality of the tube. The length of Ch is thus the circumference of the CNT, which is given by,

$$Ch = a\sqrt{n1^2 + n2^2 + n1n2}$$

Single-walled CNTs [14] are classified into one of their groups (Figure 1.5(a)), depends on the chiral number (n1, n2):

1. armchair (n1 = n2)
2. zigzag (n1 = 0 or n2 = 0), and
3. chiral (all other indices).

The diameter of the CNT is given by the formula:

$$Dcnt = Ch/\pi$$

The electrons in CNT are confined within the atomic plane of graphene. Due to the quasi- 1D structure of CNT, the motion of the electrons in the nanotubes is strictly restricted. Electrons may only move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited. Only

forward scattering and back scattering due to electron phonon interactions are possible for the carriers in nanotubes. The experimentally observed ultra long elastic scattering mean-free-path (MFP) (approximately 1µm) implies ballistic or near-ballistic carrier transport. High mobility, typical in the range of 10^3 (approx. $10^4 cm^2=V/s$) which are derived from conductance experiments in transistors. Theoretical study also predicts a mobility of approx. $10^4 cm^2=V \cdot s$ for semiconduting CNTs.

The current carrying capacity of multi-walled CNTs are demonstrated to be more than $10^9 A=cm^2$ about 3 orders higher than the maximum current carrying capacity of copper which is limited by the electron migration effect, without performance degradation during operation well above room temperature. The superior carrier transport and conduction characteristic makes CNTs desirable for nanoelectronics applications, e.g. interconnect and nanoscale devices.

4.2 CNTFET Technology

CNTs are sheets of graphene rolled into tubes; depending on the chirality (i.e., the direction in which the grapheme sheet is rolled), a single-walled CNT can be either metallic or semiconducting [14]. Semiconducting nanotubes have attracted widespread attention of device/circuit designers as an alternative possible channel implementation for high-performance transistors. A typical structure of a MOSFET-like CNFET device is illustrated in Fig 2. The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. Carbon nanotubes are high-aspect-ratio cylinders of carbon atoms. The electrical properties of a single wall carbon nanotube (SWNT) offer the potential for molecular-scale electronics; a typical semiconducting single-wall carbon nanotube is 1.4nm in diameter with a 0.6eV bandgap (the bandgap is inversely proportional to the diameter). Recent carbon nanotube field effect transistors (CNFETs) have a metal carbide source/drain contact and a top gated structure (Fig 2) with thin gate dielectrics [14], [15] and [16].

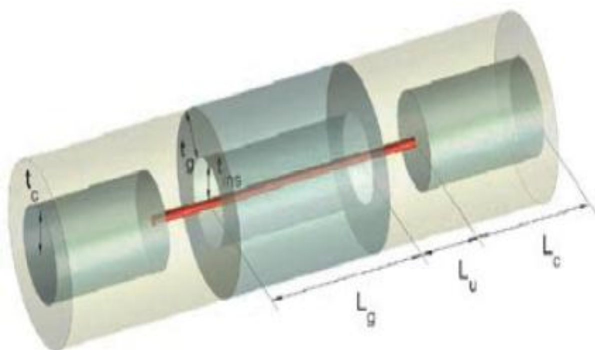
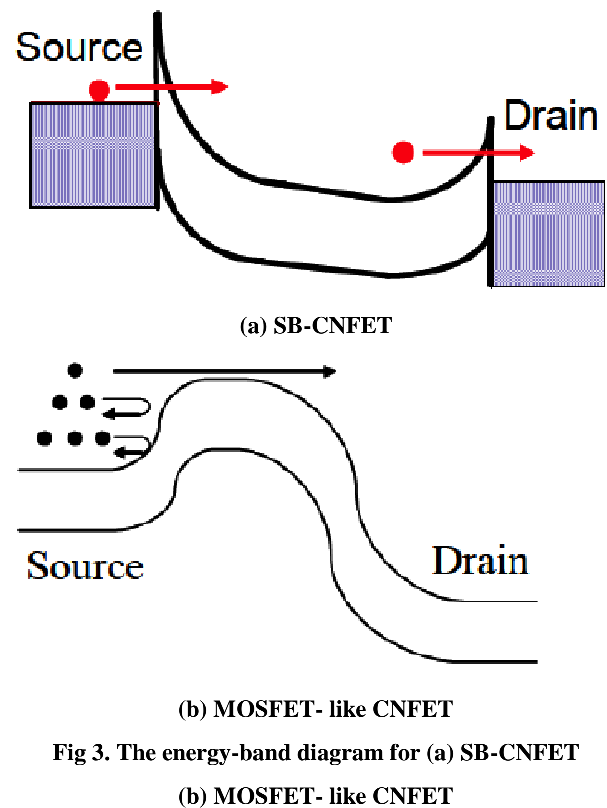


Fig 2. CNTFET Structure

The contact resistance and the subthreshold slope of a CNFET are comparable to those of a silicon MOSFET. While a silicon FETs current drive is typically measured in current per unit device width (e.g. µA=µm), the CNFETs current is measured in current per tube (as reflecting the structure of the CNFET as an array of equal carbon nanotubes with constant spacing and fixed diameter).

4.3 CNFET Features

The operation principle of carbon nanotube field-effect transistor (CNFET) is similar to that of traditional silicon devices [14]. This three (or four) terminal device consists of a semiconduting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The quasi-1D device structure provides better gate electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) structures. In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET (SBCNFET) or MOSFET-like FET. The conductivity of SB-CNFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance, as shown by Fig 3(a).



(a) SB-CNFET

(b) MOSFET- like CNFET

Fig 3. The energy-band diagram for (a) SB-CNFET

(b) MOSFET- like CNFET

height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNFET shows ambi polar transport behavior. The work function induced barriers at the end contacts can be made to enhance either electron or hole transport. Thus both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts. On the other hand, MOSFT like CNFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The non tunneling potential barrier in the channel region, and thereby the conductivity, is modulated by the gate-source bias (Fig 3(b)).

The SBs at source/drain contacts are due to the Fermi level alignment at the metal-semiconductor interface. Both the

5. 6T SRAM MEMORY CELL

The schematic diagram of 6T SRAM cell is shown in Fig.4. During read, the WL voltage VWL is raised, and the memory

cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and BQ.

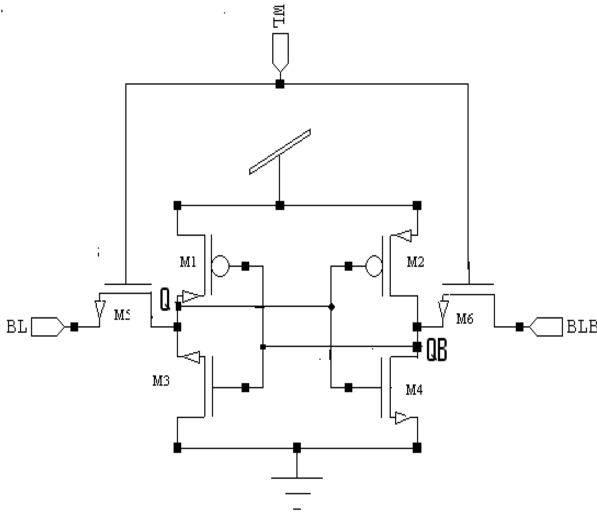


Fig 4. Schematic of 6T SRAM Cell

The sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD. Each bit in an SRAM is stored on four transistors that form two cross-coupled. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit and the explanation here is based on the same. Access to the cell is enabled by the word line which controls the two access transistor M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. A SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. SRAM Memory Cell is designed at suitable technology node by using CMOS [1],[4],[5], FinFET [3],[17],[18],[19] and/or CNTFET [20].

6. SIMULATION RESULTS

The SRAM design is allowed to be defined by using spice code. The model files for CMOS, FinFET and CNTFET at 32nm technology node are added along with the source code before simulation is performed based on [23], [24] and [25].The model files are available as open source from Predictive technology model (PTM) for CMOS and FinFET based design, and Stanford University CNFET Model website for CNTFET based design.

The simulation waveform for 6-T SRAM Cell in CMOS, FinFET and CNTFET is shown in below:

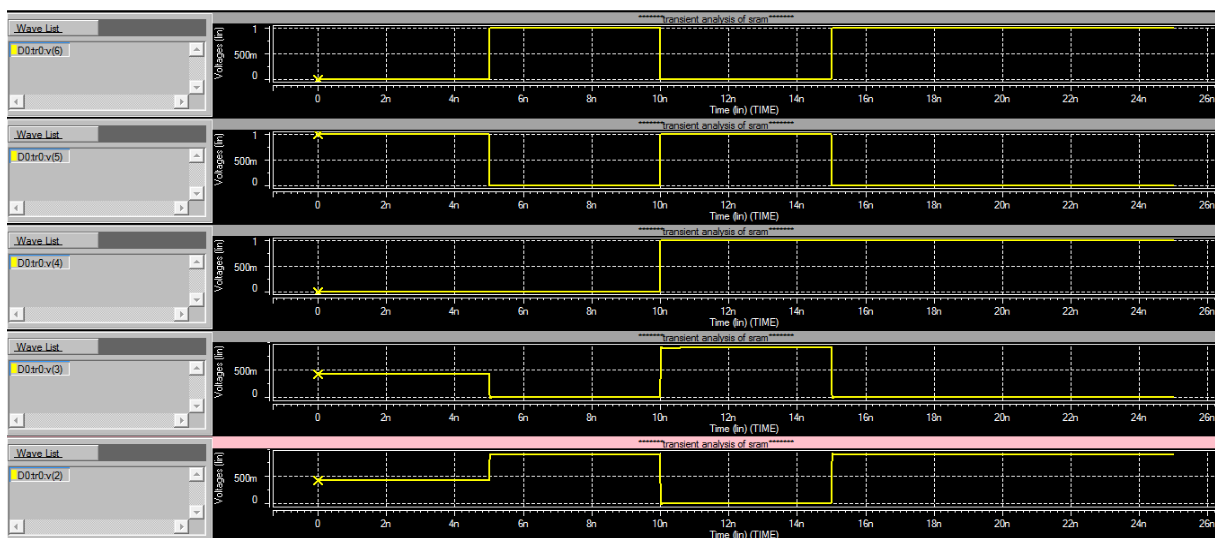


Fig 5. Simulation waveform for 6-T SRAM Cell in 32nm CMOS technology

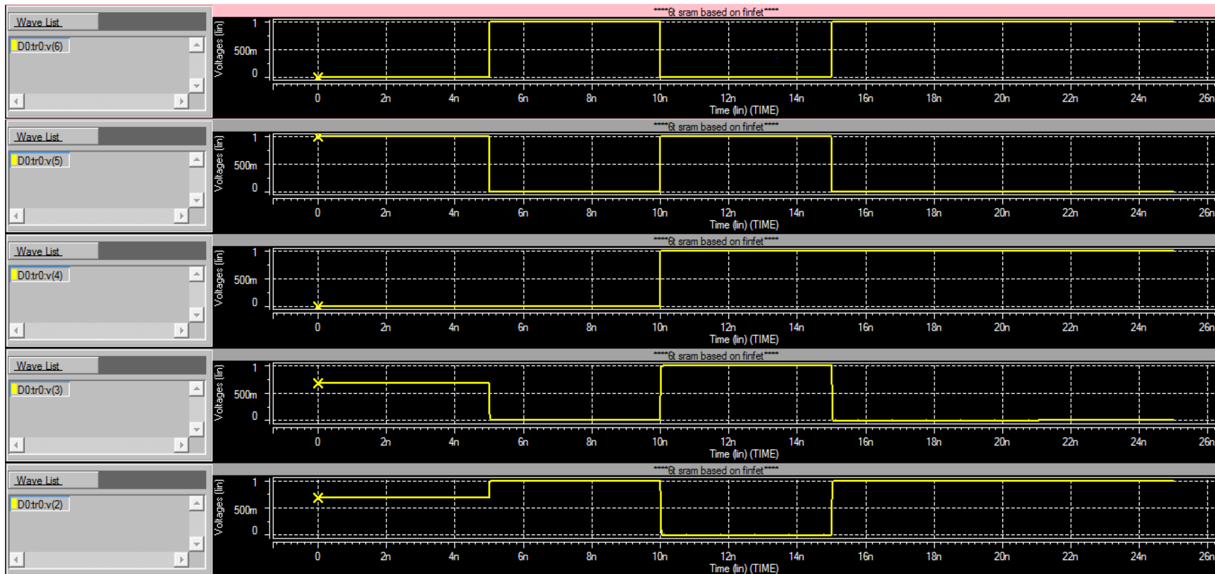


Fig 6. Simulation Waveform for 6-T SRAM Cell in 32nm FinFET technology

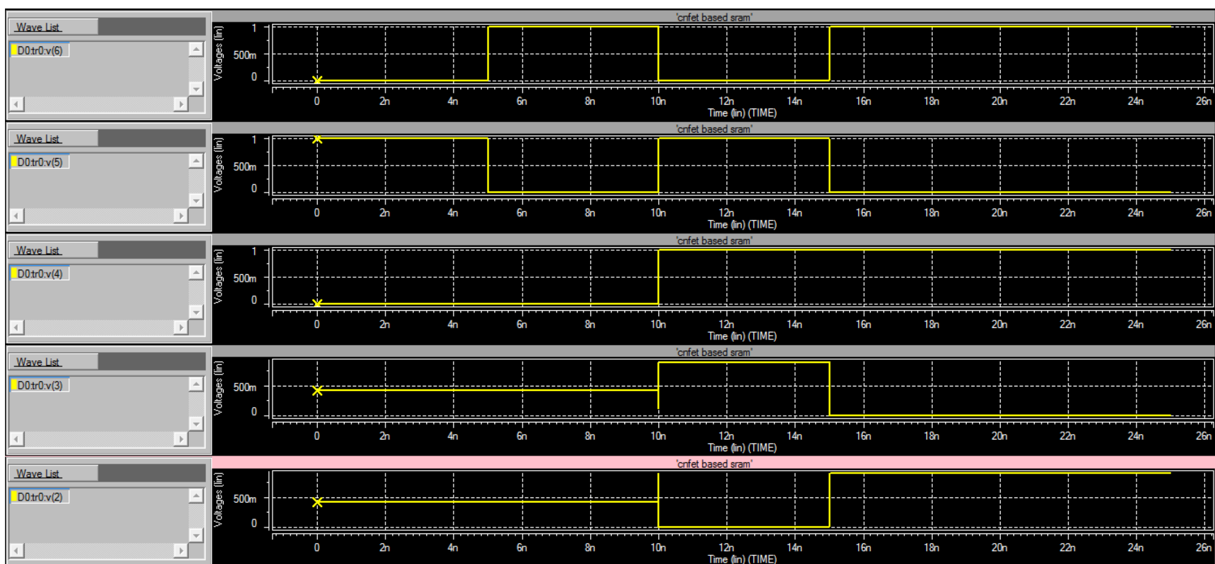


Fig 7. Simulation Waveform for 6-T SRAM Cell in 32nm CNTFET technology

The above simulation waveforms shows the input waveform such as (starting from first), Bit Line(BL), Bitline bar (BLB), Word line(WL) and its corresponding output waveform read at storage node Q and QB of 6T memory cell. CMOS, FinFET as well as CNFET based 6-T SRAM cell is designed at 32nm scale range and allowed to simulate by using HSPICE tool. Finally, the performance of each design is compared based on average power, delay and leakage current.

Table 2. Simulation Results

Parameter/ Technology	Average Power(µW)	Leakage Power(µW)	Average Delay(ns)
CMOS	9.9131	5.4711	6.1728
FinFET	4.3024	2.9526	4.9811
CNTFET	3.5655	2.2578	5.8711

7. CONCLUSION

The above table shows simulation results for 6T SRAM Cell using CMOS, FinFET and CNTFET at 32nm technology node. The designs are simulated by using Hspice Simulation tool and parameters such as average power, leakage power and average delay for three different designs are determined and compared. From the comparison, it is clear that FinFET as well as CNTFET shows better performance in all aspects when compared to CMOS based design. In addition to

Memory design, all complex designs based on CMOS are replaced by using CNTFET or FinFET.

8. ACKNOWLEDGEMENT

Our sincere thanks to Dr. S. Dasgupta, Associate Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology (IIT), Roorkee, Uttarkhand.

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