Computer Interfaced Logic IC Tester and R-C Meter

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ABSTRACT
The circuit described in this paper "Computer interfaced IC logic gate tester and R-C meter" is a device that can test and measure the value of the IC and R-C by connecting directly to the computer through the parallel port and using a software that control the device is a easy process for testing the logic IC, resistor and the capacitor. It may used instead of multimeter.

General Terms
Computer interfacing, Electronic Component Measurement.

Keywords
Logic Gate, Logic Gate IC, Resistor, Capacitor, Parallel Port, Computer interfacing.

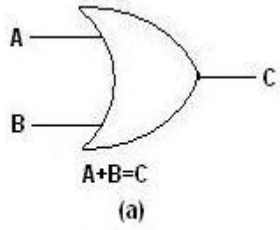
1. INTRODUCTION
Resistor, capacitor and IC logic gate are widely used in the electronic circuit, different values and types are needed to design in practical operation. To get the proper output of the circuit the component must have accurate value, Nowadays Computer is very much available, Peoples especially students take it their everyday life partner. For this reason the computer can be used as a versatile system. To make electronic circuit work properly it is very essential to measure the electronic component accurately. Good operation of any electronic circuit totally depends on good and accurate component. To ensure good and accurate measurement a personal computer can be used as a meter to test logic gate IC, Resister and Capacitor. By using this project you can use our PC as a versatile manner.

2. PRINCIPLE OF THIS DEVICE:
To test the logic gate data are directly put the input value sequentially to each gate of the IC and get the output value by the parallel port, compare the output value with the different gate table data and determined which gate it is by using the program. Now we describe the logic gate:

A logic gate is an electronic circuit that makes the logic decisions. It has one output and one or more inputs. The output signal appears only for certain combinations of input signals. Logic gates are the basic building block from which most of the digital systems are built up. They implement the hardware logic function based on the logical algebra. A unique characteristic of the Boolean algebra is that variables used in it can assume only one of the two values i.e. either 0 or 1. Hence every variable is either a 0 or 1.

2.1 The OR gate
The electronic symbol for a two-input OR gate is shown in fig 1. The two inputs have been marked as A and B and the output as C. it is worth reminding the reader that as per Boolean algebra, the three variables A, B and C can have only one of the two variables i.e. either 0 or 1. The OR gate has an output of 1 when either A or B or both are 1. In other words, it is an any-or-all gate because an output occurs when any or all the inputs are present.

Table 1. Truth table for OR gate



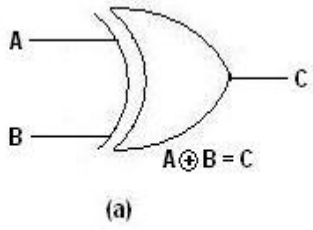
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

(b)

Fig 1: (a) Symbol and (b) Truth table for OR gate.

2.2 The OR gate
Its electronic symbol and truth table is shown in fig 2. In this gate, output is 1 if its either input but not both, is 1. In other words, it has an output 1 when its inputs are different. The output is 0 only when inputs are the same. To put it a bit differently, this logic gate has output 0 when inputs are the same.

Table 2. Truth table for ExOR gate



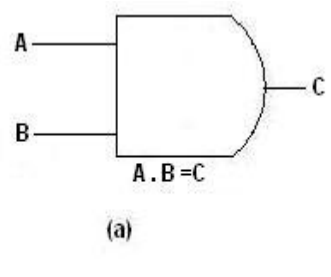
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Fig 2: (a) Symbol and (b) Truth table for ExOR gate.

2.3 The AND gate
The electronic symbol for a 2-input AND gate is shown in fig 3. It is worth reminding the readers once again that the three variables A, B, C can have a value of either 0 or 1.The AND gate gives an output only when all its inputs are present. The AND gate has a 1 output when both A and B are 1. Hence, this gate is an all-or-nothing gate whose output occurs only when all its inputs are present. In True/False terminology, the output of an AND gate will be true only if all its inputs are true. Its output would be false if any of its inputs is false.

Table 3. Truth table for AND gate



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

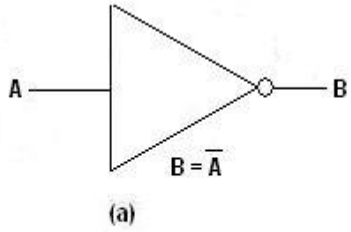
(b)

Fig 3: (a) Symbol and (b) Truth table for AND gate.

2.4 The NOT gate

The NOT gate is so called because its output is NOT the same as its input. It is also called an inverter because it inverts the input signal. It has one input and one output as shown in fig 4 (a). All it does is to invert the input as seen from its truth table of fig 4 (b).

Table 4. Truth table for NOT gate



A	B
0	1
1	0

(b)

Fig 4 : (a) Symbol and (b) Truth table for NOT gate.

The principle of R-C meter is to determine the time duration of the pulse that is depends on the value of resistor and capacitor. For this purpose to generate the pulse we are using the astable multivibrator.

2.5 The Multivibrator

Multivibrator is a device that is very useful as pulse generating, storing and counting circuits. They are basically two-stage amplifiers with positive feedback from the output of one amplifier to the input of the other. This feedback (fig. 5) is supplied in such a manner that one transistor is driven to saturation and the other to cut-off. It is followed by new set of conditions in which the saturated transistor is driven to cut-off and the cut-off transistor is driven to saturation.

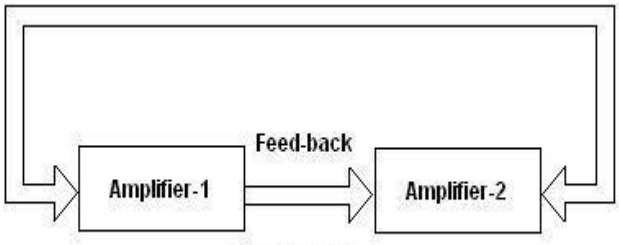


Fig 5 : Multivibrator

There are three basic types of multivibrators distinguished by the type of coupling network employed:

2.5.1 Astable multivibrator.

2.5.2 Monostable multivibrator.

2.5.3 Bistable multivibrator.

2.5.1 Astable multivibrator:

The astable multivibrator is also called free-running relaxation oscillator. It has no stable state but only two quasi-stable states between which it keeps oscillating continuously of its own accord without any external excitation.

In this circuit, neither of the two transistors reaches a stable state. When one is ON, the other is OFF and they continuously switch back and forth at a rate depending on the RC time constant in the circuit. Hence, it oscillates and produces pulses of certain mark-to-space ratio. Moreover, two outputs are available.

Pulse of astable multivibrator:

The output of astable multivibrator (fig. 6) is varying with the value of the resistor and capacitor, by calculating the variation we can easily get the value of the resistor and the capacitor.

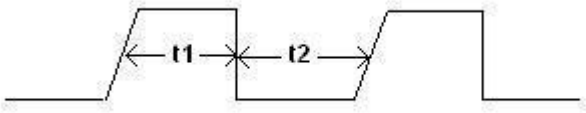


fig 6 : Output pulse of astable multivibrator.

In our project we are calculating the time width of t2 shown in fig 6 by the parallel port by using appropriate program.

3. DESCRIPTION OF THE PROJECT:

To describe our project easily we are dividing the project into two sections. These are:

3.1 Hardware section.

3.2 Software section.

3.1 Hardware section:

In hardware section NE 555 with appropriate arrangement are used as astable multivibrator. The functional diagram of the 555 IC timer is shown in fig. (7).

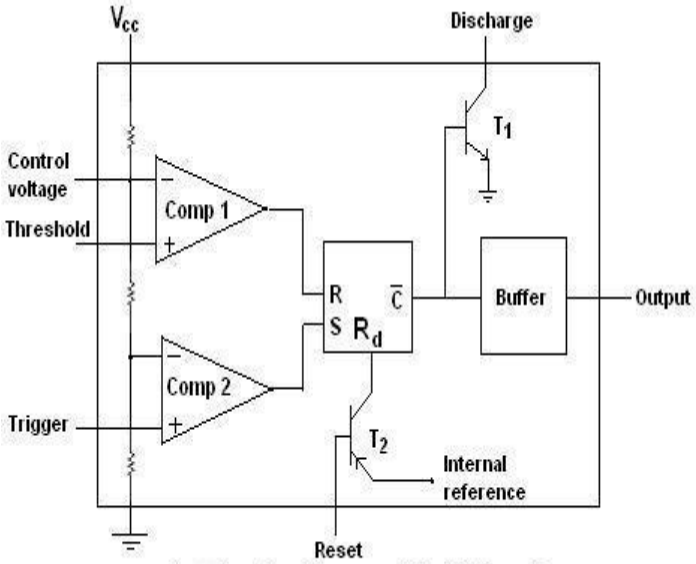


Fig 7 : Functional diagram off the 555 timer IC

The strings of three resistors bridged between the supply voltage Vcc and ground provides reference voltages for the

two comparators. The reference voltage for comparator 1 is Vcc /3 and for comparator 2 is 2Vcc /3. These reference voltages have control over the timings. In applications where timings are to be varied by an external signal, the control voltage input terminal is used. In other applications this input capacitively bypassed to ground.

On the negative going transition of the trigger input and when the trigger voltage passes through Vcc /3, the outputs of Comp.2 sets the flip-flop. On a positive going transition of threshold voltage 2Vcc /3, the output of Comp.1 reset the flip-flop. The reset input of the 555 provides a mechanism to reset the flip-flop in a manner which over-rides the effect of any set input from Comp.2. This overriding effect is obtained when the reset input is less than about 0.4 v. When not used, it should be return to Vcc. The transistor T2 serves as a buffer to isolate the reset input from the flip-flop and the transistor T1. The output buffer stage is able to source currents as high as 200mA and provides logic levels compatible with TTL logic.

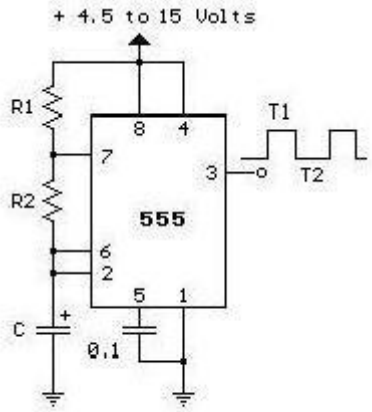


Fig 8 : Astable multivibrator.

An external timing capacitor may be connected between the discharge terminal and ground. When the flip-flop is in reset state, the output is in logic 1 state. The transistor is T1 in saturation and the timing cycle starts when the flip-flop goes to set state and is T1 is off.

The external capacitor is then free to charge through the external resistor. The connection of 555 as an astable multivibrator is shown in fig (8).

The capacitor C charges through R1 and R2 till its voltage reaches 2Vcc /3 when the capacitor is discharged through Rb. The discharge continues till the voltage across C just falls below Vcc /3. The cycle is repeated. The charge and discharge times are:

T1=0.7*(R1 + R2)*C and

T2=0.7*R2* C respectively.

The frequency of oscillation is given by:

f=1/ 0.7*(R1 + 2R2)*C.

According to the astable multivibrator frequency oscillation principle if the capacitor C (2200μF) is keeping fixed and if we collect the value of T2 by the computer through the parallel port then the unknown R2 can be measured by the following relation.

R2=T2/0.7*C.

Where T2 and C are known.

We are using the following (fig 9) astable multivibrator circuit.

Again

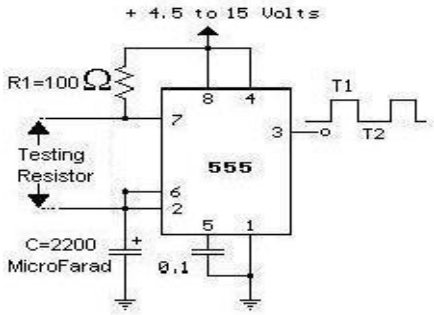


Fig 9: Measuring the resister.

according to the astable multivibrator frequency oscillation principle if the resistor R2 (20MΩ) is keeping fixed and if we collect the value of T2 by the computer through the parallel port then the unknown capacitor C can be measured by the following relation.

C=T2/0.7* R2.

Where T2 and R2 are known.

We are using the following (fig 10) astable multivibrator circuit

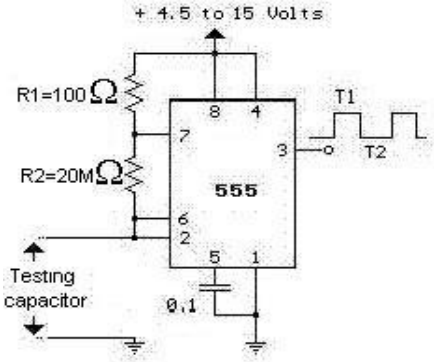


Fig 10: Measuring the capacitor.

For logic gate IC test description we are considering the 7432 that is a two input four OR gate IC the internal structure of 7432 is shown in fig 11.

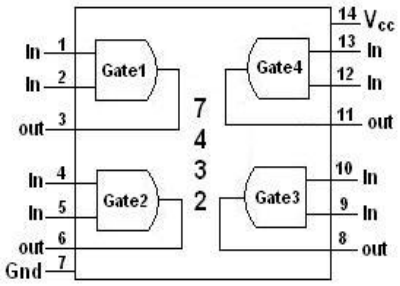


Fig 11: Internal structure of 7432 IC.

We have seen from the fig 11 that each gate has two input and one output so we are giving the sequential value to the input by the parallel port (Data pin) and get the output from the output pin and check the output value by the parallel port (Stack pin), if the value are appropriate for the OR gate truth table then show the gates are perform well. The truth table for 7432 OR gates IC are shown in fig 12.

Table 5. Table for 7432 IC:

Gate no	Input		Output
Gate 1	0	0	0
	0	1	1
	1	0	1
	1	1	1
Gate 2	0	0	0
	0	1	1
	1	0	1
	1	1	1
Gate 3	0	0	0
	0	1	1
	1	0	1
	1	1	1
Gate 4	0	0	0
	0	1	1
	1	0	1
	1	1	1

Fig 12: Table for 7432 IC.

connected to S4 and S5 (stack pin) of the parallel port, these pins read the condition of the output pin of the IC and using these data the program test the IC.

In the section of resistor measuring, the 555 arranging astable multivibrator the capacitor C (2200μF) value is fixed but the resistor R2 is testing as shown in fig 13, the output (pin 3) is connected to the stack pin S4 of the parallel port and measured the time duration between the low to high state. Therefore calculating the value using the equation:

R2=T2/0.7*2200.

In the section of capacitor measuring, the 555 arranging astable multivibrator the resistor R2 (20MΩ) value is fixed but the capacitor C is testing as shown in fig 13, the output (pin 3) is connected to the stack pin S5 of the parallel port and measured the time duration between the low to high state. Therefore calculating the value using the equation:

C=T2/0.7* 20.

4. TYPESET TEXT

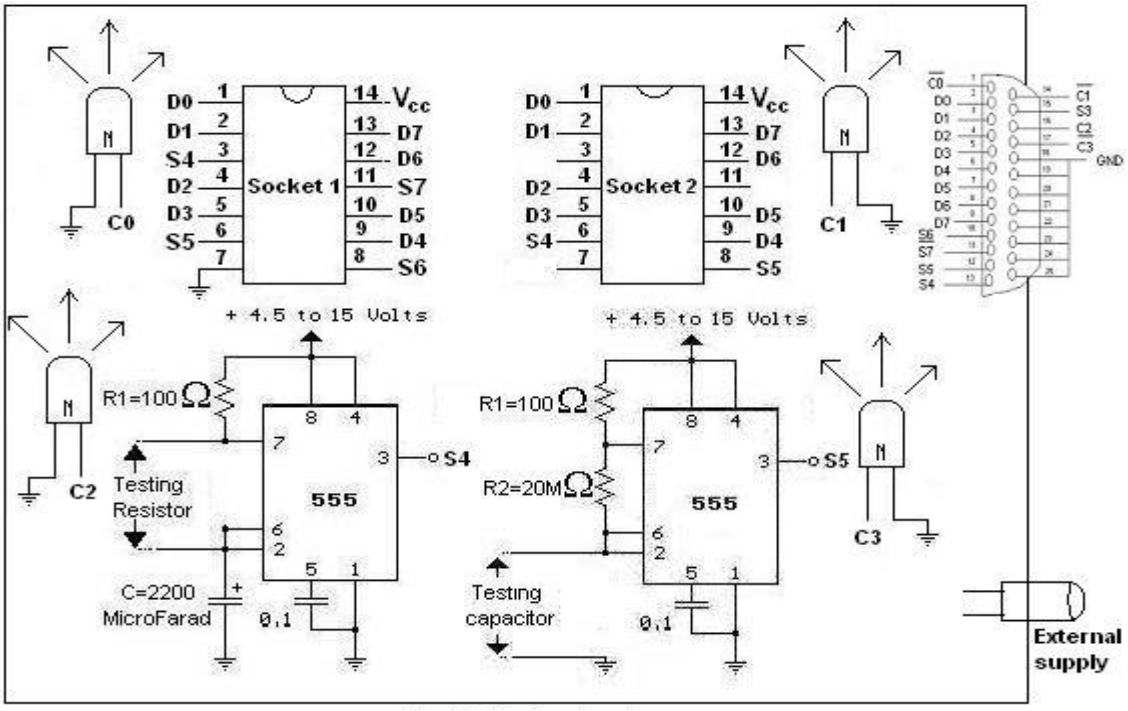


Fig 13: Main circuit.

3.1.1 Main Circuit Operation:

In the section of socket 1 the two input logic gate IC are tested. For this purpose D0, D1 for gate1 D2, D3 for gate2 D4, D5 for gate3 and D6, D7 pins for gate4 of parallel port are used for giving input value sequentially. Our testing criteria is to check first gate then other get for this purpose when a get is tested then the input of the other gates are given such a value that the outputs are high. The outputs of the gates are connected to S4, S5, S6, and S7 (stack pin) of the parallel port, these pins read the condition of the output pin of the IC and use these data the program test the IC.

In the section of socket 2 the four input logic gate IC are tested. For this purpose D0, D1, D2, D3 pin for gate1 and D4, D5, D6, D7 pin for gate2 of parallel port are used for giving input value sequentially. Our testing criteria is to check first gate then other get for this purpose when a get is tested then the input of the other gates are given such a value that the outputs are high. The outputs of the gates are

3.2 Software Section:

The data and instruction that are used by the software generally get through the parallel port so now we describe just the essential part of the computer port.

3.2.2 PC PORT:

To be completely functional the CPU of computer need to accept data and after performing operation, the result need to be displayed or performing the task according to the manner. And for this PC have a number of input and output devices. Those various devices are connected with the computer through a number of ports as required. Those ports are commonly treated as PC port.

Various PC ports:

Parallel port, Serial port, USB port

3.2.3 PC parallel port:

A PC printer/parallel port is an inexpensive and yet powerful platform for implementing projects dealing with the control of real world peripherals. The printer port provides

eight TTL outputs, five inputs and four bi-directional leads and it provides a very simple means to use the PC interrupts structure. Typical view of PC parallel port:

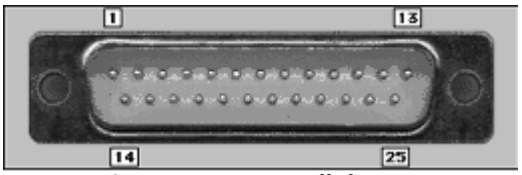


Figure 14: PC parallel port.

The parallel port had the capability to transfer 8 bits of data at time. As technology progressed and the need for greater external connectivity increased, the parallel port became the means by which one could connect higher performance peripherals. These peripherals now range from printer sharing devices, portable disk drives and tape backup to local area network adapters and CD ROM players. The pin configurations of the parallel port are shown below.

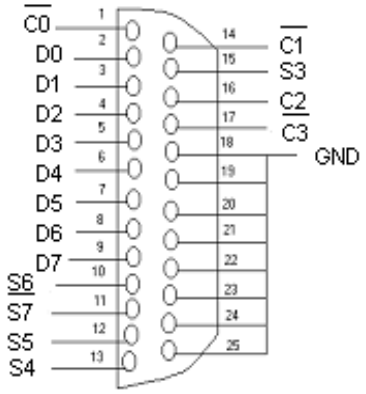


Figure:-pin configuration of the parallel port.

The Parallel Port is the most commonly used port for interfacing homemade projects. This port will allow the input of up to 9 bits or the output of 12 bits at any one given time, thus requiring minimal external circuitry to implement many simpler tasks. The port is composed of 4 control lines, 5 status lines and 8 data lines. It's found commonly on the back of PC as a D-Type 25 Pin.

The table below shows the parallel port pin description. The output of the Parallel Port is normally TTL logic levels. The voltage levels are the easy part. The current you can sink and source varies from port to port. Most Parallel Ports implemented in ASIC, can sink and source around 12mA. However these are just some of the figures taken from Data sheets, Sink/Source 6mA, Source 12mA/Sink 20mA, Sink 16mA/Source 4mA, Sink/Source 12mA. As you can see they vary quite a bit. The best bet is to use a buffer, so the least current is drawn from the Parallel Port.

Table 6: - Pin Assignments of the D-Type 25 pin Parallel Port Connector Parallel Port pins Addresses:

Pin No (D-Type 25)	SPP Signal	Direction In/out	Register	Hardware Inverted
1	Control 0	Out	Control	Yes
2	Data 0	In/Out	Data	No
3	Data 1	In/Out	Data	No
4	Data 2	In/Out	Data	No
5	Data 3	In/Out	Data	No
6	Data 4	In/Out	Data	No
7	Data 5	In/Out	Data	No
8	Data 6	In/Out	Data	No
9	Data 7	In/Out	Data	No
10	Status 6	In	Status	No
11	Status 7	In	Status	Yes
12	Status 5	In	Status	No
13	Status 4	In	Status	No
14	Control 1	Out	Control	Yes
15	Status 3	In	Status	No
16	Control 2	Out	Control	No
17	Control 3	Out	Control	Yes
18 - 25	Ground	Gnd		No

The port is composed of 4 control lines, 5 status lines and 8 data lines. Each type of lines has its separate pin address and these address codes are used to control the pin. These are listed in table 2, below.

Table 7: - Parallel Ports pin Addresses.

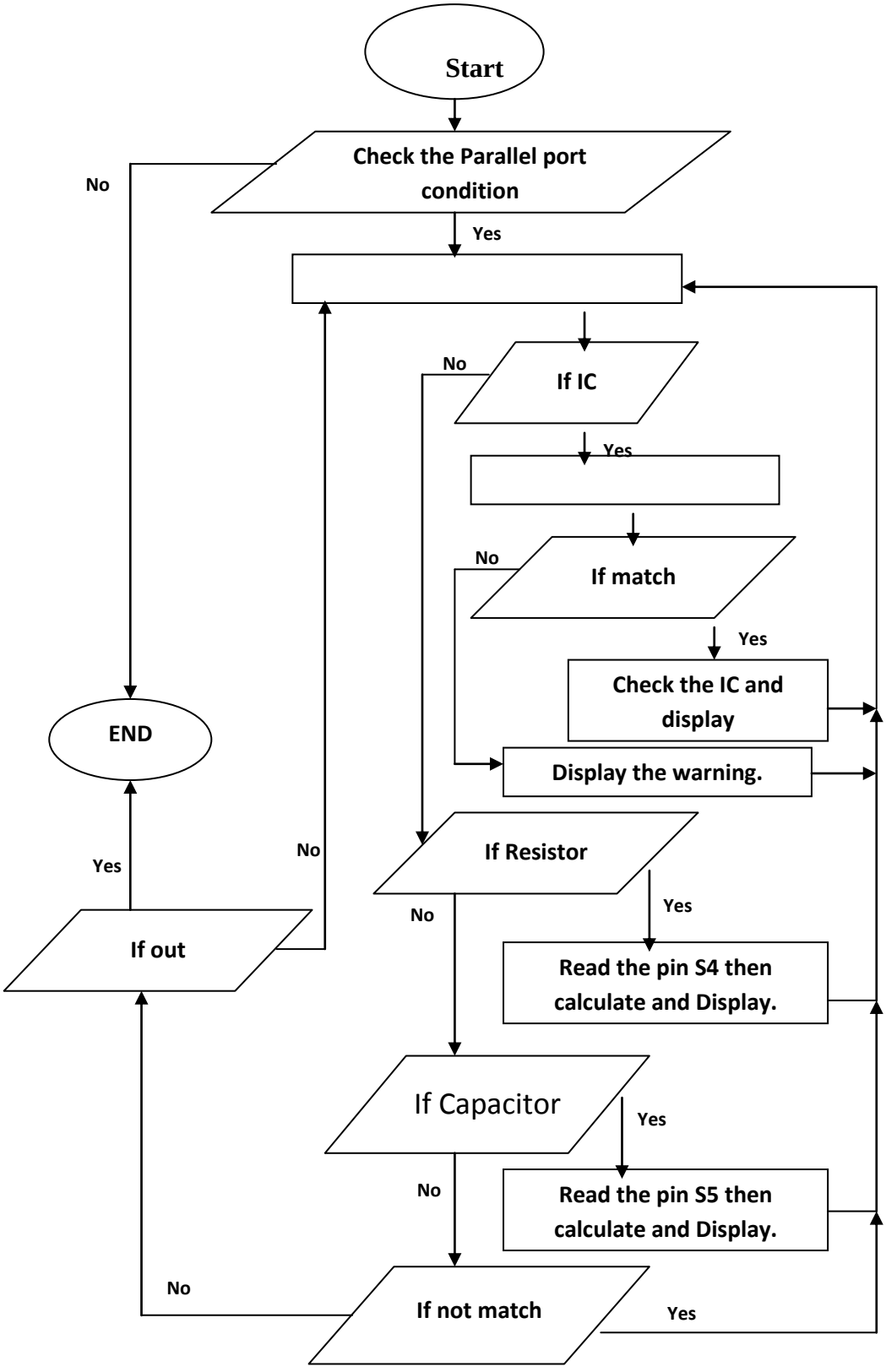
Pin lines	Address
Data lines	0x378
Control lines	0x37a
Status lines	0x379

The 0x denotes that it is in hexadecimal. These addresses we are using in C language to control the pin.

Algorithm of the program:

1. Start.
2. Check the parallel port condition.
3. If parallel port pin condition are ok then go to step 4 else terminate the program.
4. Want the option of operation, for IC test go to step 5, for measuring the resister go to step 8, for measuring the Capacitor go to step 10, for terminating the program go to step 12.
5. Want the IC number
6. Then give the proper input through the parallel port (Data pin D0-D7).
7. Then read the output through the parallel port (stack pin S3, S4, S5, S6) and check the data and display. Return to step 4.
8. Wait for press the Enter.
9. Then read the output for resistor through the parallel port (stack pin S4) and calculate the data and display then return to step 4.
10. Wait for press the Enter.
11. Then read the output for capacitor through the parallel port (stack pin S5) and calculate the data and display then return to step 4.
12. Terminate the program.

Flow chart:


Start
Check the Parallel port condition
No
Yes
No
If IC
Yes
No
If match
Yes
Check the IC and display
Display the warning.
END
Yes
No
If Resistor
Yes
No
If out
Read the pin S4 then calculate and Display.
If Capacitor
Yes
No
Read the pin S5 then calculate and Display.
No
If not match
Yes

4. How to operate the hardware and program:

The main hardware is operated by +5 volt dc so at first the hardware is connected to the dc supply then connected with the computer through the parallel and run the software. The handle the program is shown step by step in fig 16, 17, 18, 19.

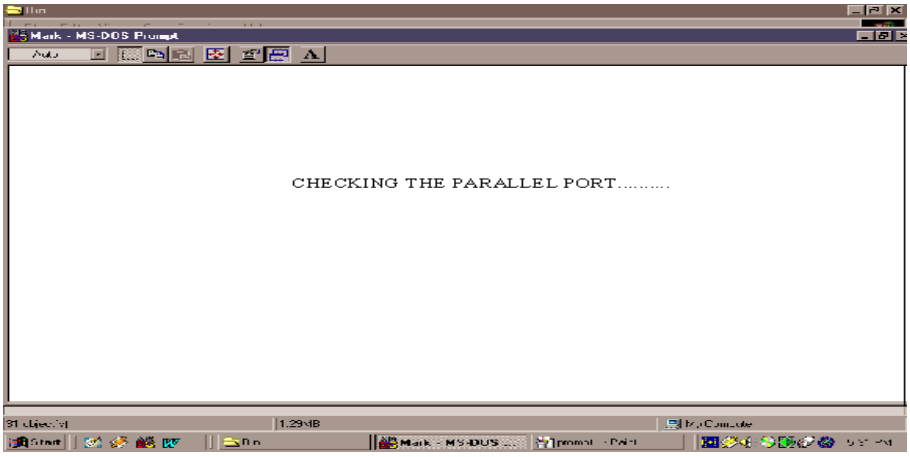


Fig 16: Checking the parallel ports condition.

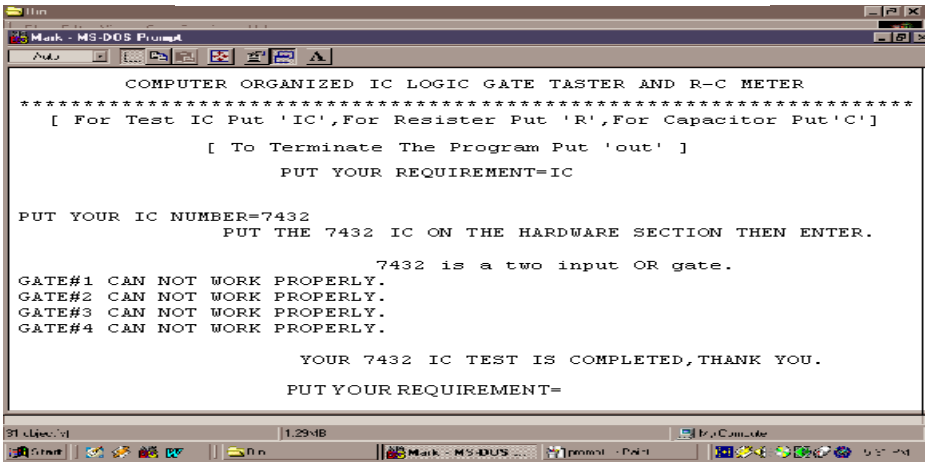


Fig 17: Want the required command for operation.

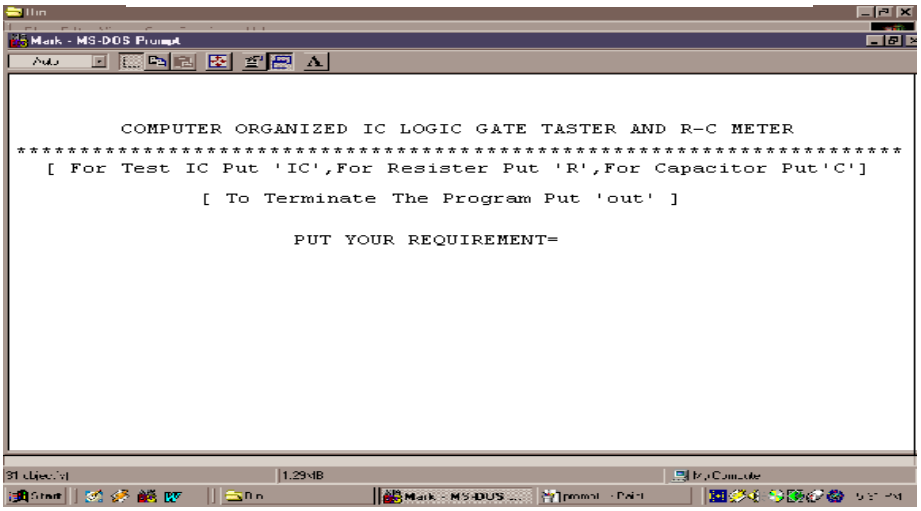


Fig 18: IC operation works.

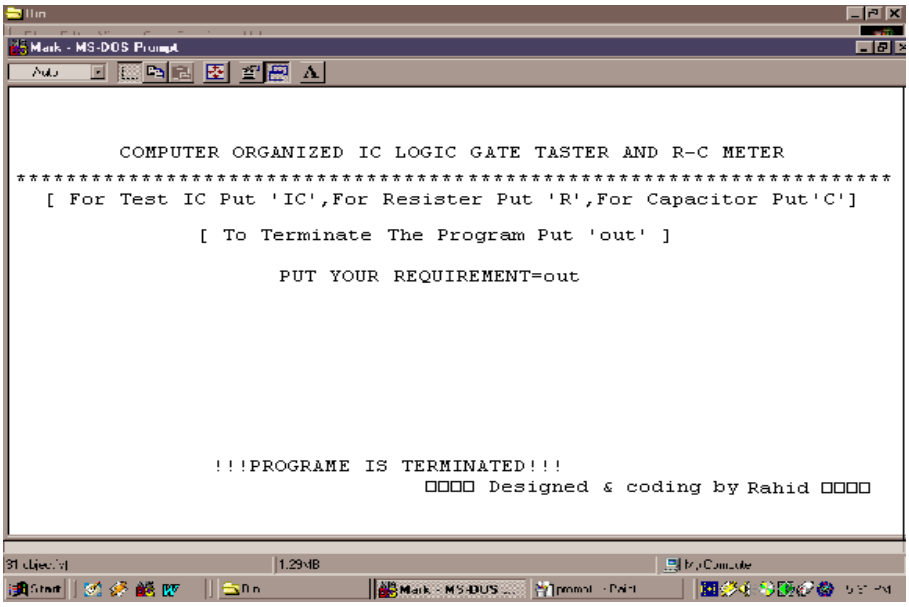


Fig 19: Program terminating process.

5. CONCLUSION

The process is able to test and measure the logic gate IC and can test resistor and capacitor. Furthermore develop this process and principle also can measure the other electronic components and different IC's.

6. REFERENCES

[1] Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, Digital systems : principles and applications —10th ed.by Pearson Prentice Hall.

[2] Herbert Schildt, Teach yourself C, 3rd edition, McGraw - Hill publication.

[3] Dr. k. jain, An Introduction to switching theory and digital electronics.