A New Design of Full Adder based on XNOR-XOR Circuit

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ABSTRACT
This paper presents pre-layout simulations of a proposed 8T full adder design using a proposed 3T XNOR gate cell. The proposed design remarkably reduces power consumption hence power-delay product (PDP) over various input voltages and frequencies. It also improves temperature sustainability as compared to the existing 8T full adder. This proves to be a viable option for low power and energy efficient applications. It also shows nearly 82% improvement in threshold loss as compared to the existing 8T full adder. All simulations have been performed on 45nm standard model on Tanner EDA tool version 12.6.

General Terms
Power consumption and full adder.

Keywords
2T (2 Transistors), 3T, 8T, XNOR and PDP.

1. INTRODUCTION
The demand and popularity of portable electronic circuits systems is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability [1]. Power is one of the premium resources for designing a portable system.

Low power VLSI circuits have become important criteria for designing the energy efficient electronic circuits for high performance in other electronic systems. All battery operated mobiles and implanted devices require maximum battery life [2]. Extended battery life can be achieved by operating the circuit at low power.

With the advancement of VLSI technology, many computing intensive applications such as multimedia processing, digital communication can now be realized in hardware to either speed up the operation or reduce the power/energy consumption. The essence of the digital computing lies in the design of full adder. The design criteria of a full adder are usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many functional units such as multiplier and compressor [3], [4], [5]. Two other important, yet often conflicting, design criteria are power consumption and delay. A better metric is the power-delay product or energy consumption per operation to indicate the optimal design tradeoffs.

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI circuits and systems such as comparators, parity checkers, application-specific DSP architectures and microprocessors. Full adders are often in the critical paths of complex arithmetic circuits for subtraction, multiplication, division, exponentiation, address calculation, etc. In most of these systems, the adder is part of the critical path that determines the overall performance of the system [6]. Enhancing the performance of the 1-bit full adder can significantly affect the system performance. The performance of a full adder circuit depends on the type of the design style used for implementation as well as the logic function realized using the particular design style. So, it is very important to choose the adder topology to yield the desired performance.

2. EXISTING CIRCUIT
The structure of a general full adder has three inputs a, b, c_{in} and two outputs sum and carry. The input signals a, b and c_{in} will be added together logically [1], [3], [6], [7]. The output signals of the full-adder sum and carry can be expressed as in Eq. (1) and Eq. (2)

$$sum = a \oplus b \oplus c_{in} \tag{1}$$
$$carry = (a \oplus b)c_{in} + ab \tag{2}$$

The diagram of existing 8T full adder is shown in Figure 1. The sum output has been implemented using two numbers of 3T XNOR gate in cascade and the carry output has been implemented using 3T XNOR gate and 2T multiplexer [8], [9], [10].

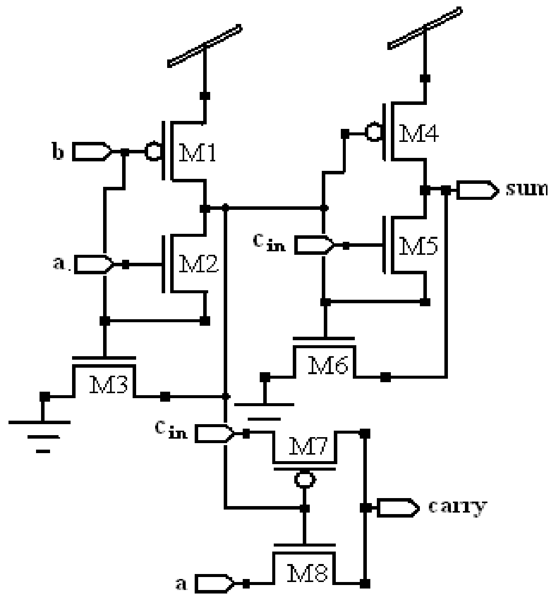

Fig 1: Existing 8T Full Adder

This full adder design is confronted with problems for certain input vectors. The outputs have good logic level for only certain input vectors. There is a major degradation in output voltage that may lead to functional failure as well as increased power consumption for the remaining input vectors.

For example, when ab=11, the first stage gives the degraded output. Since nMOS is a weak '1' device it will not pass complete logic ‘1’ signal at the first stage and as nMOS is strong ‘0’ device, it will pass compete ‘0’. This results in the degraded output at the first stage. As both nMOS M2 and M3 get enabled and try to transfer opposite signals on the first stage output result into voltage degradation. Similarly, for ab=10, transistor M1 and M2 get enabled and try to transfer opposite signals resulting into voltage degradation. This degraded output when given to the second XNOR stage, the output sum is further degraded. This leads to increase in power consumption as well as in PDP. Figure 2 shows the input-output waveform of the existing 8T full adder.

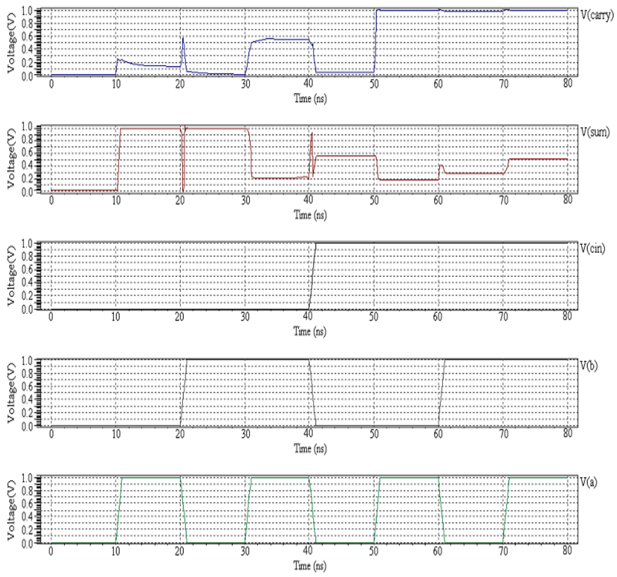

Fig 2: Input-output waveform of existing 8T full adder

3. PROPOSED 3T XNOR CELL AND 8T FULL ADDER DESIGN

The proposed design of XNOR gate is shown in Figure 3. It consists of 3 transistors as one pMOS and two nMOS. The Out terminal is connected to drain of all transistors.

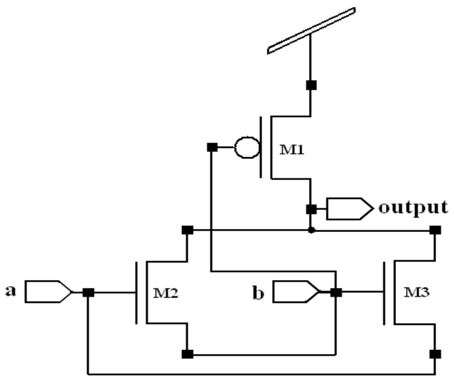

Fig 3: Proposed 3T XNOR gate

When ab=00, nMOS M2 is OFF and pMOS M1 is ON on account of higher gate voltage than the corresponding threshold. As pMOS is strong ‘1’ device it will pass complete logic “high” signal at the output.

When ab=01, nMOS M2 is OFF but nMOS M3 becomes ON. As nMOS is strong ‘0’ device, it will pass complete logic “low” signal at the output. When ab =10, both nMOS M2 and pMOS M1 are ON. As mobility of nMOS is nearly three times higher than pMOS, it will drive the output ignoring the effect of ON pMOS transistors which results into complete zero output.

When ab=11, both nMOS transistors are ON and only nMOS will be responsible for driving the output. Table 1 describes the performance of proposed 3T XNOR gate.

Table 1. Performance table of proposed 3T XNOR gate

a	b	Expected Output	Obtained Output
0	0	1	**1.00**
0	1	0	**0.00**
1	0	0	**0.15**
1	1	1	**1.00**

Figure 4 shows the schematic of the proposed 8T full adder that have been implemented with the help of another proposed 3T XNOR gate. The sum output has been implemented using 3T XNOR gate in cascade and the carry output is designed by 3T XNOR gate and 2T multiplexer.

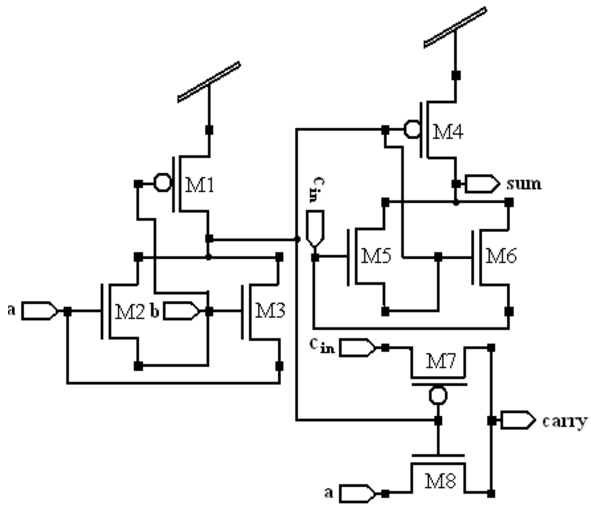

Fig 4: Proposed 8T full adder

The output of first stage is simply the XNORing of the input ‘a’ and ‘b’. For generation of the sum output, the output of the first stage is further XNORed with ‘c_{in}’. The output of the first stage is used as a selector circuit for the carry output. When the output of the first stage i.e $a \odot b$ is “0”, the carry output is equal to the carry in i.e. ‘c_{in}’. When the output of the first stage i.e $a \odot b$ is “1”, the carry output is equal to the input ‘a’. Figure 5 shows its input-output waveform and Table 2 gives the comparison of performances of the existing 8T and proposed 8T full adder, which reveal that the threshold loss is remarkably reduced in the proposed 8T full adder design than the existing 8T full adder design. This is important for the complex circuit design.

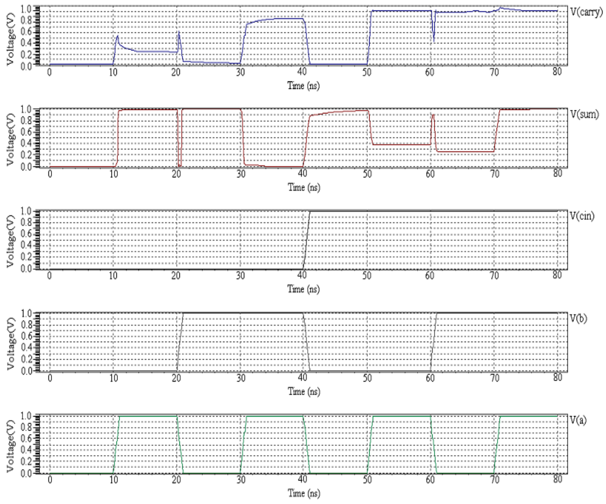

Fig 5: Input-output waveform of proposed 8T full adder

Table 2. Performance table of existing and proposed 8T full adder

Input			sum output	
c_{in}	b	a	existing 8T	proposed 8T
0	0	0	0.00	0.00
0	0	1	1.00	1.00
0	1	0	1.00	1.00
0	1	1	**0.21**	**0.00**
1	0	0	**0.55**	**0.98**
1	0	1	0.17	0.36
1	1	0	**0.28**	**0.24**
1	1	1	**0.51**	**1.00**

This circuit reduces the overall PDP at varying input voltages and operating frequencies and also improves the temperature sustainability. The average power consumption in VLSI circuits is expressed as sum of three components as shown in Eq.(3)

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (3)$$

where $P_{switching}$ represents the average switching power consumption, $P_{short\text{-}circuit}$ represents short circuit power consumption and $P_{leakage}$ represents leakage power consumption. The average power consumption is given by Eq.(4)

$$P_{avg} = \alpha_T C_L V_{DD}^2 f + I_{short-circuit} V_{DD} + I_{leakage} V_{DD} \quad (4)$$

4. SIMULATIONS AND COMPARISON

All schematic simulations have been performed on Tanner EDA tool version 12.6 at 45nm technology with input voltage ranging from 0.6V to 1V in steps of 0.1V. To establish an impartial testing environment both circuit have been tested on the same input patterns which covers all combinations of the input stream. In order to prove that proposed design is consuming low power along with better performance, simulations are carried out for power, power-delay product at varying supply voltages, temperatures and frequencies. Figures 6 through 11 reveal that the proposed 8T full adder cell proves its superiority in terms of power consumption, power delay product at various input voltages and frequencies, and temperature sustainability over the existing 8T full adder. Figure 7 and Figure 11 are plotted on logarithmic scale to show better view of comparison.

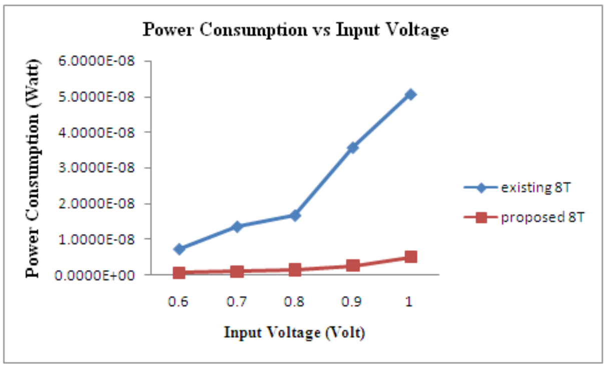

Fig 6: Power consumption vs input voltage of existing 8T and proposed 8T full adder

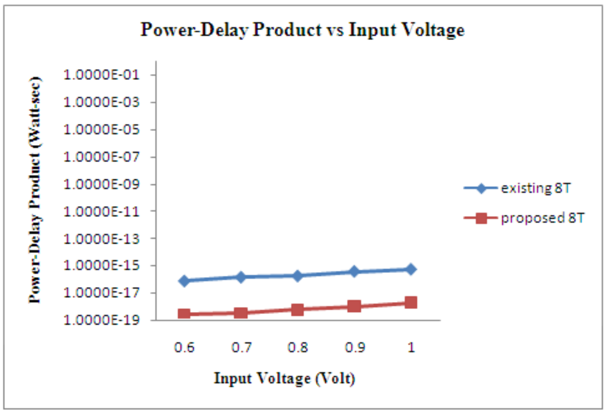

Fig 7: Power-delay product vs input voltage of existing 8T and proposed 8T full adder

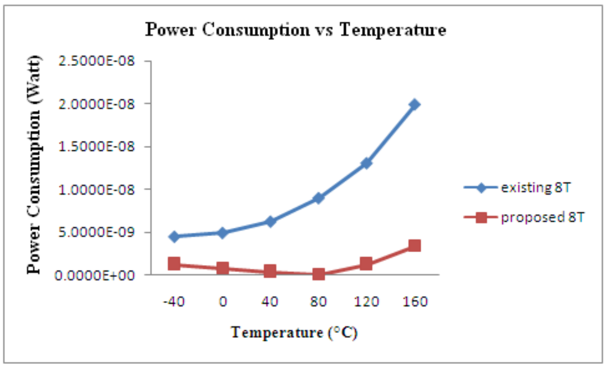

Fig 8: Power consumption vs temperature of existing 8T and proposed 8T full adder

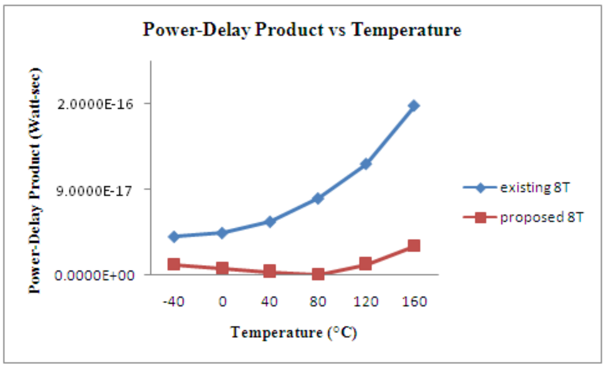

Fig 9: Power-delay product vs temperature of existing 8T and proposed 8T full adder

Figure 6 and Figure 7 show that the power consumption and power-delay product of the proposed 8T full adder is 90% to 95% and 99% reduced than the existing 8T full adder design respectively. The graph shown in Figure 8 and Figure 9 reveal that the proposed 8T full adder design have 72% to 99% better temperature sustainability compare to the existing 8T full adder design.

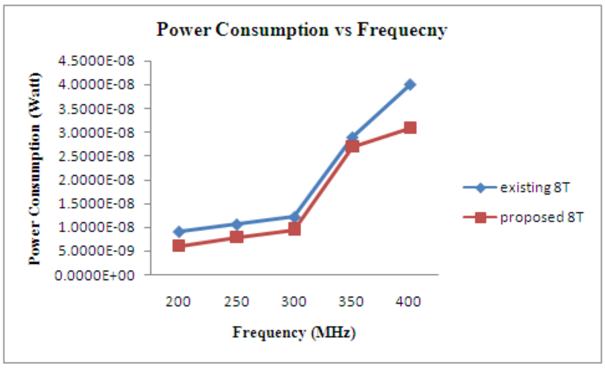

Fig 10: Power consumption vs frequency of existing 8T and proposed 8T

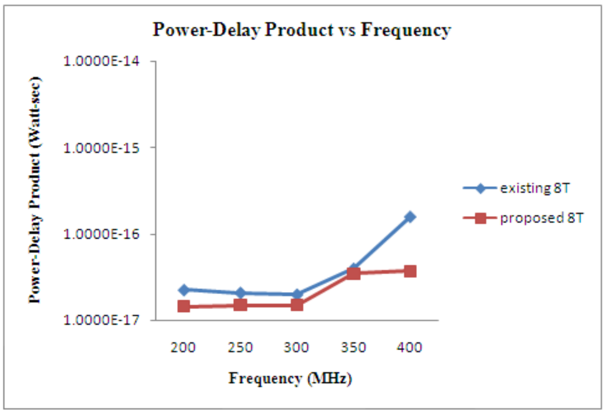

Fig 11: Power-delay product vs frequency of existing 8T and proposed 8T

Eq.(4) states that the increase in frequency will result into increased power consumption, but as power consumption and delay are inversely proportional to each others, resulting the PDP curve. Figure 10 and Figure 11 reveal that the power consumption and power-delay product with varying operating frequency of the proposed 8T full adder design is 12% to 76% better than the existing 8T full adder design.

5. CONCLUSION

The proposed 8T adder has been designed and simulated on Tanner EDA tool version 12.6 at 45nm technology. The proposed 8T 1-bit full adder is found to give better performance than the existing 8T full adder. It has been tested to have better temperature sustainability and significantly less power and power-delay product at various input voltages and frequencies. It gives 82% improvement in threshold loss than the existing 8T full adder.

6. REFERENCES

[1] Sumeer Goel, Ashok Kumar, Magdy A. Bayoumi, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 14, No. 12, pp. 1309-1321, Dec. 2006.

[2] H Boddapati, A Naregalkar, Raju B L, "Novel Asynchronous Adders," *International Conference and Workshop on Emerging Trends in Technology*, pp. 1055-1058, 2011.

[3] Jin-Fa Lin, Yin-Tsung Hwang, Ming-Hwa Sheu, Cheng-Che Ho, "A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design," *IEEE Transactions on Circuits and Systems*, Vol. 54, No. 5, pp. 1050-1059, MAY 2007.

[4] A. Bellaour, Mohamed I. Elmasry, "*Low-Power Digital VLSI Design: Circuits and Systems*," second edition, Wesley.

[5] D. Radhakrishnan and A.P. Preethy, "Low Power CMOS Pass Logic 4-2 Compressor for High-Speed Multiplication," *Proc. 43rd IEEE Midwest Symp. on Circuits and Systems*, pp. 1-3, Aug. 2000.

[6] Ahmed M. Shams, Tarek K. Darwish and Magdy A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 1, pp. 20-29, Feb. 2002.

[7] Walid Ibrahim, Valeriu Beiu and Mawahib Hussein Sulieman, "On the Reliability of Majority Gates Full Adders," *IEEE Transactions on NANOTECHNOLOGY*, Vol. 7, No. 1, pp. 56-67, Jan. 2008.

[8] Riya Garg, Suman Nehra, and B. P. Singh, "Low Power Full Adder using 9T Structure," *International Journal on Recent Trends in Engineering and Technology*, Vol. 8, No. 2, pp. 52-55, Jan. 2013.

[9] Riya Garg, Suman Nehra, and B. P. Singh, "1-bit Full Adder using 9T Structure," *International Conference on Technical and Executive Innovation in Computing and Communication (TEICC)*, pp. 560-564, Dec. 2012.

[10] Manoj Kumar, Sandeep K. Arya, Sujata Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," *International Journal of VLSI Design & Communication Systems*, Vol. 2, pp. 47-59, Dec. 2011.