Design of New Low Leakage Power Domino XOR Circuit

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ABSTRACT
In this paper, a new XOR gate is proposed. Proposed circuit adopts mixed N-type and P-type transistors in the pull down network and current mirror at the footer transistor. This topology reduces leakage power consumption. Simulation parameters are measured at 25°C and 110°C. Proposed circuit reduces leakage power consumption up to 51.7% at 25°C and 56% at 110°C as compared to standard N-type domino XOR gate. Similarly, proposed circuit reduces leakage power consumption up to 47.28% at 25°C and 51.1% at 110°C as compared to standard P-type domino XOR gate.

Keywords
Domino, Delay, Gate oxide leakage current, Leakage power consumption, A.C noise margin.

1. INTRODUCTION

XOR gate is one of the arithmetic unit and it is used in many VLSI applications such as microprocessors [1], adders [2] etc. Design of XOR gate using static CMOS [3], [4], [5] required pull up and pull down network and hence layout area, power consumption increases while speed decreases. Design of XOR gate using domino CMOS required small layout area due to the elimination of pull up network. As the elimination of pull up transistors, parasitic capacitance at dynamic and output node get reduced hence it enhanced the speed of the domino XOR gate. A Domino circuit consists of clocked pull up and footer transistor, and the pull down network [6], [7], [17]. Clock loading increases the power consumption of the domino circuit. Due to the high speed and low area requirement of domino circuit, it is used in large VLSI applications. Standard domino XOR gate inputs required two phase signals, one is original and other is inverted signal. Inverted signal required extra hardware. This Extra hardware not only increased the power consumption but also deviates the performance of the domino XOR circuit.

Power supply is reduced with the scaling of CMOS technology. Power consumption of the CMOS circuit is directly proportional to the square of the supply voltage. As the power supply decreases, power consumption decreases at the cost of speed. To overcome the delay, threshold voltage of the transistor is lowered but it leads an exponential increase in subthreshold leakage current (Isub). Many circuit level techniques are implemented to compensate the high subthreshold leakage current such as input vector control [8], dual threshold technique [9], and body bias control [10].

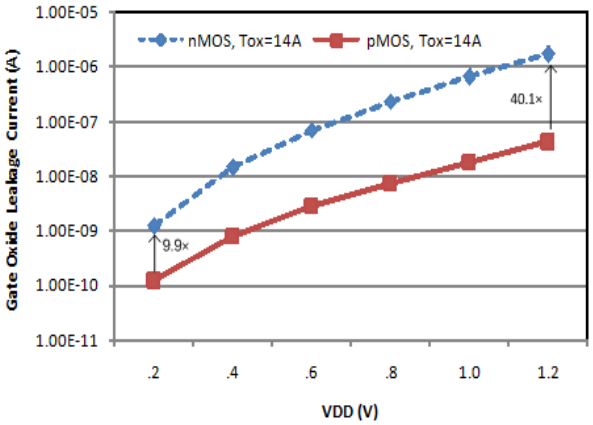

Figure 1. Comparison of gate oxide leakage current for an nMOS and pMOS [11].

Technology scaling also lowers the gate oxide thickness (tox). Gate oxide leakage current (Igate) is caused by direct tunneling of electron and hole through the gate oxide membrane. In CMOS technology, gate oxide thickness greater than 20Å have negligible Igate as compared to Isub. Reducing the gate oxide thickness increases the gate oxide leakage current. Igate of an nMOS transistor is dominant over pMOS transistor because tunneling probability of electron from valence band is higher in compared to tunneling probability of hole from conduction band. Depending on the voltage difference across the gate oxide [11], [12], Igate produced by an nMOS transistor is 9.9x to 40.1x times greater in compared to Igate of a pMOS transistor as shown in Fig.1. Fig.2 shows the variation of Isub and Igate of an nMOS transistor with supply voltage at two different temperatures. At 110°C, the Isub is 6.7 times greater in compared to Igate at nominal supply voltage [11]. Similarly, at the room temperature, the Igate is 2.5 times greater in compared to Isub at nominal supply voltage. Many circuit techniques are implemented to compensate both subthreshold and gate oxide leakage current [11] - [15], [19].

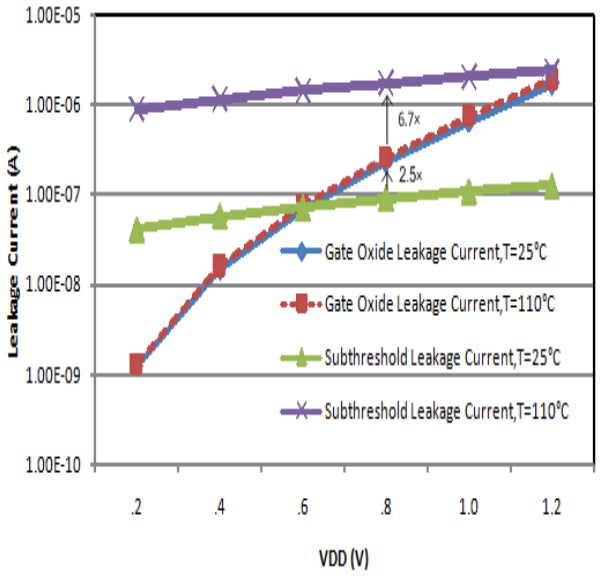

Figure 2. Comparison of subthreshold and gate oxide leakage current of an nMOS at two different temperatures [11].

In this paper, a low leakage domino XOR circuit is proposed. Proposed circuit employed mixed N and P type transistors in the pull down network and current mirror in the footer transistor. The paper is organized as follows: Section 2 describes the operation of the standard domino XOR CIRCUIT. In Section 3, proposed circuit is illustrated in details. Simulation results are presented in section 4, and the conclusion is presented in Section 5.

2. STANDARD XOR CIRCUIT

The standard n-type domino XOR gate (DXN) as shown in Fig. 3[16]. M2 act as charge keeper. Pull down network consists of combination of n-type transistors. Here dynamic node gives XNOR logic and output node gives XOR logic. Operation of the circuit (precharge and evaluation phase) depends on the state of clock signal. When clock is low, the circuit is in precharge phase. Dynamic node is charged to high voltage by the pull up transistor M1. Footer transistor M5 turns OFF to avoid short circuit current in the circuit. When clock is high, the circuit is in evaluation phase. M1 turns OFF and M5 turns ON. Discharging of dynamic node is decided by the combination of inputs of the circuit. If A=0, B= 1 or A=1, B= 0, dynamic node turns to low voltage and output node turns to high voltage. Output node remains low for the other input states.

The standard p-type domino XOR gate (DXP) as shown in Fig. 4[16]. M2 act as charge keeper. Pull up network consists of combination of p-type transistors. Working of the circuit is explained as follows: During precharge phase, charging of dynamic node depends on the combination of inputs. If A=0, B=0 or A=1, B=1, dynamic node is charged to high voltage and output node is discharged to low voltage. For other inputs state, output remains high. During evaluation phase dynamic node is discharged to low voltage and output node is charged to high voltage.

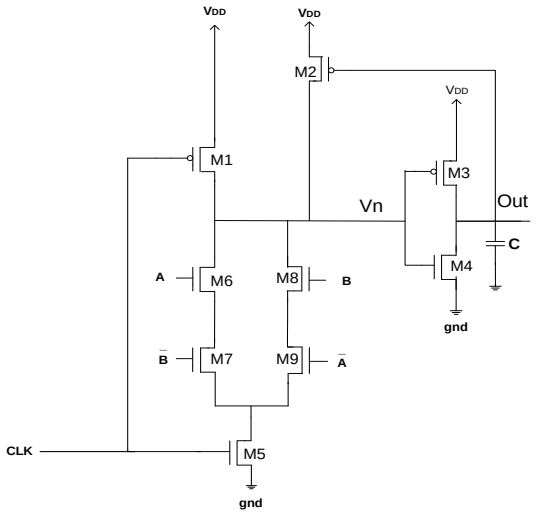

Figure 3. Standard N-type domino XOR gate (DXN) [16].

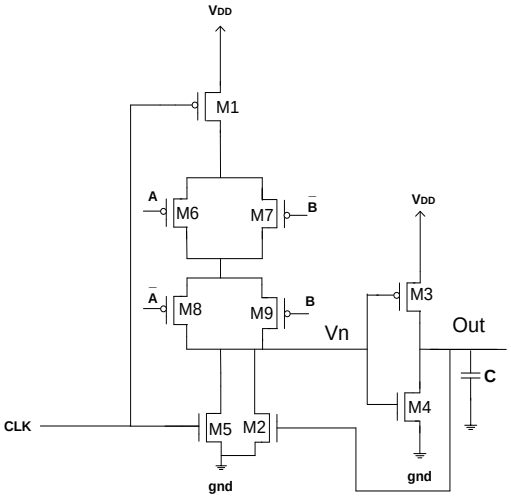

Figure 4. Standard P-type domino XOR gate (DXP) [16].

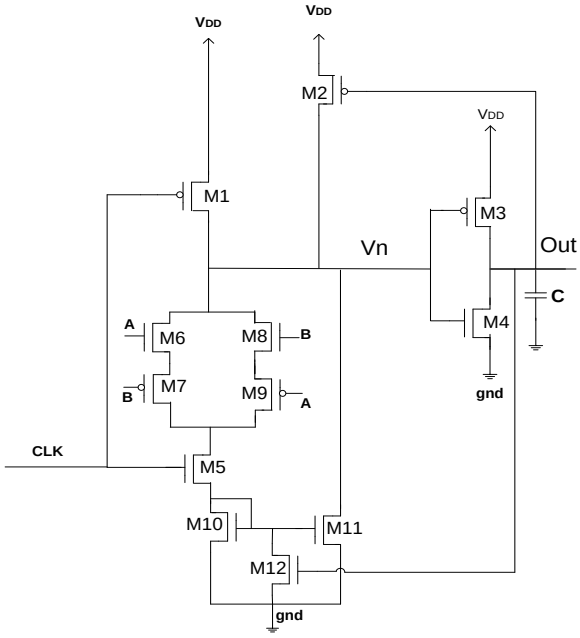

Figure 5. Mixed domino XOR gate (DXM).

3. PROPOSED XOR CIRCUIT

P-type domino XOR effectively suppresses both subthreshold and gate oxide leakage current because of higher barrier height for holes tunneling from conduction band in compared to electron tunneling from valence band. N-type domino XOR has higher speed due the higher electron mobility. Another drawback of p-type and n-type domino XOR is that the inputs signal must be in two phases, one is original and other is inverted. Extra inverter has been required to obtain both phases. To overcome all this problems a mixed topology has been proposed which contains the property of both p and n-type domino XOR gate.

The proposed XOR gate adopts N and P type mixed transistors in the pull-down network (DXM) as shown in Fig.5. In this circuit, two series combination paths of N and P type transistors are connected in parallel. Transistor M10 is connected in series to footer transistor for leakage reduction due to stacking effect at the cost of speed. To increase the speed, a current mirror M11 is added in parallel to the pull down network to increase the discharging current. Transistor M12 provides feedback from the output node. This helps to avoid short circuit current on the static inverter.

The operation of the proposed circuit is explain as follows: when clock is low, the circuit is in precharge phase, dynamic node V_n is charged to high voltage .Transistor M10 is OFF and therefore current mirror M11 is also OFF. When clock is high, the circuit is in evaluation phase, dynamic node is discharged depending on the inputs of the XOR gate. If inputs A=0, B=1 or A=1, B=0, dynamic node is discharged to low voltage and output node is charged to high voltage. Current mirror M11 pulls large current from the dynamic node resulting high speed. For other combination of inputs, dynamic node is high and output node is low. M10 reduces the leakage current of the pull down network due the stacking effect. Logical expression at dynamic and output node is given as

$$V_n = \overline{(A.\overline{B}) + (\overline{A}.B)} \quad (1)$$

$$V_n = A.B + \overline{A}.\overline{B} \quad (2)$$

Output node gives XOR logic: $V_{OUT} = A.\overline{B} + \overline{A}.B$ (3)

4. EXPERIMENTAL RESULTS

In this section, proposed circuit and previous circuits such as DXN and DXP is simulated respectively using HSPICE tool in the 45nm predictive technology [18]. 1GHz clock frequency is applied to all the circuits with load capacitance 1fF. Threshold voltage for an nMOS and a pMOS transistor are set as 0.22V and - 0.22V, respectively. To have reasonable comparison, all the circuits have similar size. Leakage power consumption is measured at 25°C and at 110°C, respectively. Active mode power consumption, A.C noise margin, delay and PDP are measured at 110°C.

At 25°C, gate oxide leakage current is more significant over subthreshold leakage current. In table 1, at 25°C, the value of leakage power consumption of proposed circuit and previous circuits for different clock and input states are listed. From the table it is clear that the proposed circuit have lower leakage power consumption as compared to the previous circuits. The optimal leakage power consumption states of DXN, DXP and DXM are {clock=0,input=(0,1)},{clock=0, input=(1,0)} and{clock=0,input=(1,1)} respectively. DXM reduces leakage power consumption by 51.7% and 47.28% as compared to DXN and DXP respectively. Therefore, at low temperature, DXM has minimum leakage power consumption as compared to other techniques.

Table 1. Leakage power consumption (µW) of three XOR circuits in different Input States and Clock States at 25°C.

	DXN		DXP		DXM	
	CLK=0	CLK=1	CLK=0	CLK=1	CLK=0	CLK=1
A=0,B=0	2.06	3.50	1.93	1.91	1.27	1.56
A=0,B=1	2.01	3.08	1.92	2.57	1.70	5.59
A=1,B=0	2.46	3.08	1.84	2.05	1.31	5.59
A=1,B=1	2.43	3.13	2.57	2.55	0.97	1.30

At 110°C, subthreshold leakage current becomes more significant over gate oxide leakage current. In table 2, at 110°C, the value of leakage power consumption of proposed circuit and previous circuits for different clock and input states are listed. From the table it is clear that DXM have lower leakage power consumption as compared to the previous circuits. The optimal leakage current states of DXN,DXP and DXM are {clock=0,input=(1,1)},{clock=1, input=(1,0)} and {clock=0,input=(0,0)} respectively. DXM reduces leakage power consumption by 56% and 51.1% as compared to DXN and DXP respectively. Therefore, at high temperature, DXM has minimum leakage power consumption as compared to other previous techniques.

Table 2. Leakage power consumption (µW) of three XOR circuits in different Input States and Clock States at 110°C.

	DXN		DXP		DXM	
	CLK=0	CLK=1	CLK=0	CLK=1	CLK=0	CLK=1
A=0,B=0	14.87	21.22	16.81	14.72	6.39	9.37
A=0,B=1	19.07	17.78	16.94	14.41	7.93	15.38
A=1,B=0	16.11	17.58	16.46	13.08	7.93	15.38
A=1,B=1	14.55	21.37	18.02	15.93	6.83	9.73

A.C noise margin is defined as the level of noise signal for which output is decreased by 10% of its maximum value. Noise signal is applied to all inputs of the circuits and to be set as 1GHz square wave with 60% duty cycle at 110°C. A.C noise margin is calculated for the proposed circuit and previous circuits are listed in Table 3. DXM technique increased A.C noise margin by 17.77% and 10.41% as compared to DXN and DXP circuits.

Table 3. A.C noise margin of three XOR circuits at 110°C.

XOR	DXN	DXP	DXM
A.C noise margin	0.45V	0.48	0.53

Active mode power consumption and worst case delay is measured when a conditional discharging path is established between the dynamic node and ground during evaluation phase. Table 4 shows comparison of active mode power consumption, delay and PDP of three XOR circuits at 110°C.From the table it is clear that DXM reduces active mode power consumption by 8% and 2.4% as compared to DXN and DXP circuits. Drawback of DXM technique is that it has lower speed and higher PDP as compared to the previous techniques.

Table 4. Comparison of active power consumption, delay and PDP for proposed circuit and existing circuits at 110°C.

XOR	Active power(μW)	Delay(ps)	PDP(fJ)
DXN	81.81	68.18	5.57
DXP	77.10	72.69	5.60
DXM	75.23	76.32	5.74

5. CONCLUSION

At low temperature, gate oxide leakage current is more significant over subthreshold leakage current. Similarly, at high temperature, subthreshold leakage current is more significant over gate oxide leakage current. Technology scaling increases both subthreshold and gate oxide leakage current. In a 45nm CMOS technology, both leakage currents are needed to be suppressed. In this paper, a new XOR circuit is proposed to reduce leakage power consumption and active mode power consumption as compared to standard XOR circuits. Proposed circuit utilizes mixed N and P type transistors in the pull down network and current mirror at the footer of the circuit. Circuits are simulated in HSPICE tool based on 45nm technology. At 25°C, proposed circuit reduces leakage power consumption by 51.7% and 47.28% as compared to N-type domino XOR and P-type domino XOR respectively. At 110°C, proposed circuit reduces leakage power consumption by 56% and 51.1% as compared to N-type domino XOR and P-type domino XOR respectively. Proposed circuit reduces active mode power consumption by 8% and 2.4% as compared to standard N-type and P-type XOR gate. Similarly, proposed circuit increases A.C noise margin by 17.77% and 10.41% as compared to standard N-type and P-type XOR gate.

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