# FPGA Implementation of Fuzzy Logic Controller for Temperature Control

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#### **ABSTRACT**

This paper describes FPGA implementation of a Fuzzy Logic Controller (FLC) using VHDL for temperature control (FTC). The system is built up with major modules namely fuzzification, inference, implication and defuzzification. The VHDL code is downloaded into FPGA board of SPARTAN-3 XC3S400 in PQ208 pin package. The FTC is also modeled in C and matlab. Output of FTC in VHDL, C and Matlab are compared for different input conditions for verifying the functionality of the FTC chip,

#### **Keywords**

FPGA, FLC, FTC, Fuzzification, implication, defuzzification..

#### 1. INTRODUCTION

For many years, fuzzy logic has been an attractive technology for designers of industrial, consumer and automotive products. However, achieving the right balance between cost and performance has not always been easy. Dedicated fuzzy processor chips can meet the most demanding performance needs. VHDL-based logic synthesis is an efficient method for designing complex hardware.

This paper describes FPGA realization of a Fuzzy Logic Controller (FLC) using VHDL for temperature control (FTC). A fuzzy system improves the relative performance of a temperature control process with respect to the conventional scheme [1]. It compensates non-linear errors, accelerates the response and reduces the steady-state error and maintains temperature constant at the desired value regardless of changes in the load or environment.

FLC structure with closed loop control system and realization of small rules for industrial temperature control system demonstrated that the fuzzy logic control is much more capable than the current temperature controllers. Four control schemes namely PID, fuzzy logic control(FLC), FLC using genetic algorithms (FLC-GA) and Neuro-Fuzzy control (NFC) presented by Thyagarajan for regulating the temperature of the Air Heat Plant highlighted superiority of FLC over PID, FLC-GA FLC and NFC schemes. All these schemes are evaluated with respect to set-point tracking using performance indices [2] [3].

In this paper, the control system is implemented using VHDL, aiming for FPGA implementation. There are several advantages for this approach. Field programmable Gate Array (FPGA) is used as hardware platform, because FPGA allows very high logic capacity (the amount of digital logic that can be mapped into a single FPD [4] [5]. FPGAs offer more flexibility than ASICs, as when a design is not needed any

more; the chip can be reprogrammed for a new hardware. Thus, the FPGA based systems are flexible and can be reprogrammed number of times [6]. Fuzzy algorithms can be executed on low-cost conventional microcontrollers, but as these have architectures that were not designed to handle fuzzy logic, the software overhead often makes the performance inadequate. Dedicated fuzzy processor chips can meet the most demanding performance needs.

#### 2. Development of the FTC Algorithm

Here the algorithm is developed for controlling the temperature. The models of the controller based on fuzzy rules are known as, the Fuzzification module, Inference module, Implication module, and Defuzzification module [7] [8]. All the relevant and crucial parameters are explained and illustrated, including the set of fuzzy rules applicable. The fuzzy model has been coded in C also presented in this paper.

Difference between set temp and current temp (Error) is taken as input in the model. Input "Error" consists of two trapezoidal membership functions (negative and positive) and one triangular membership functions (zero) over a range from -64 to 64. Figure 1 illustrates the fuzzy variables. Based on these, the fuzzy logic model determines the amplitude of the voltage signal that is necessary to be sent to the heater in order to maintain a constant temperature in the industrial process. This is provided by "Output" (output signal) from the model, with a range of [-1.8 to 3.6]. The "Output" signal has 3 triangular membership functions (low, medium and high) spaced over this range as shown in figure 2.

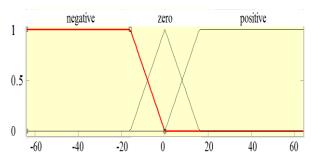


Figure 1: Input "error"

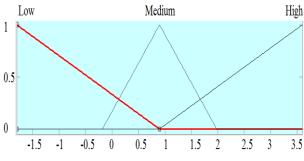


Figure 2: Output

Three fuzzy rules (IF/THEN) used in the model are shown in figure 3. The connective OR is maximum operation interpretation. While the connective AND is given a minimum interpretation. The output is produced based on various combinations of the fuzzy inputs.

- 1 if (input is negative) then (output is low)
- 2 if (input is zero) then (output is medium)
- 3 if (input is positive) then (output is high)

Figure 3: Fuzzy IF - THEN rules

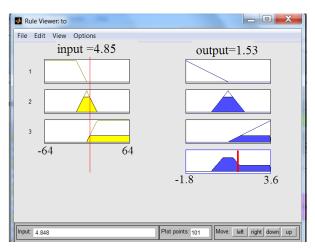


Figure 4: Matlab rule view

Fig. 4 is a Matlab generated input output relation by firing the rules. (For specific value, input = 4.85 and output=1.53). And fig 5 shows the matlab generated plot that shows the surface of the fuzzy rules used in the model [9]. It is important to note that the surface changes in a gradual and smooth manner with fuzzy variable "error". This smooth change in the surface indicates that the rules as a whole are consistent and hence an accurate output might be produced by the system. In addition, both inputs and output range can be normalized so that system becomes adaptable to various input/output parameters, through the use of appropriate simple conversion circuits. Hence, the model can be used for different processes with simple change in algorithm.

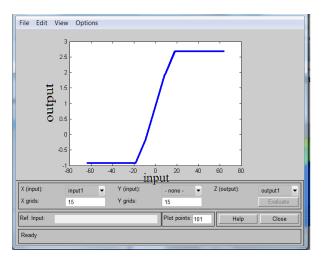


Figure 5: Matlab surface view

# 3. Modeling of the FTC in C

Here the FTC algorithm developed in C is used as a reference and verification tool for the VHD model. For developing VHDL algorithm input "error" is normalized to the range from 0 to 128.

The FTC has been divided into four modules according to function, i.e. Fuzzification, Inference, Implication, and Defuzzification. It accepts input "error", and produces a crisp output value "Output", using rules as shown below.

R[1] = E[n]

R[2] = E[z]

R[3] = E[p]

Where n, z and p refers to membership functions negative, zero and positive for error . The C statement, R[1] = E[n], corresponds to the rule 1: If input (error) is negative then output is R1.

#### 3.1 Fuzzification module

This module accepts two crisp (i.e. real world) signals ("set" and "Actual" temp) and produces output "Error" (difference between set temp and actual temp), as shown in figure 6. Fuzzified values of "error" are forwarded to Implication module. In this model, input signal discourse upon 2 membership functions

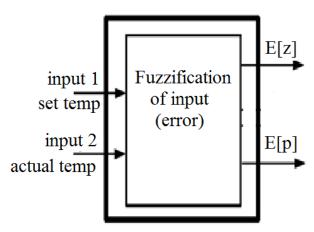


Figure 6: Fuzzification

Where E[n], E[z] and E[p] are membership functions for negative, zero and positive value of error. For example if "error" = 4, then membership function for Fuzzy variable error zero is E[z] = 0.75 and membership function for Fuzzy variable error positive is E[p] = 0.25 as shown in figure 7.

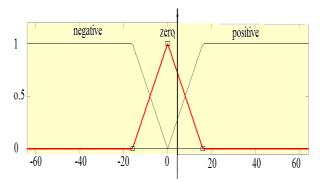


Figure 7: Membership function of "error"

#### 3.2 Inference module

In this module, appropriate rules are fired according to fuzzy variables. Only two fuzzy variables are activated at any given time. Hence each fuzzy variable results in firing two rules. Here the universe of discourse is divided into 2 regions where each region containing only two fuzzy variables

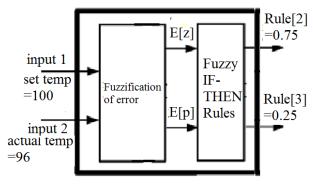


Figure 8: Inference

Here in figure 8, error = 4 with membership functions zero (E[z] = 0.75) and positive (E[p] = 0.25). Hence according to IF-THEN rules of the system (figure 4), rules 2 and 3 are selected.

### 3.3 Functional and timing simulation

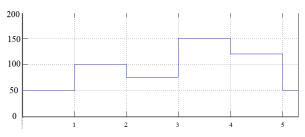


Figure 9: set temp

The fuzzy algorithm is simulated for different input conditions. the timing response of set temp, current temp, error and output signal are shown in fig.9 to fig.12.

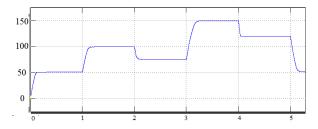


Figure 10: actual temp

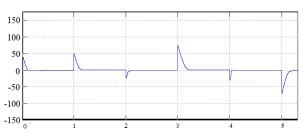


Figure 11: error

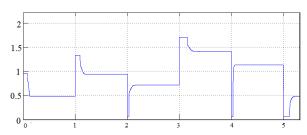


Figure 12: output signal

#### 4. Modeling of the FTC in VHDL

FTC Algorithm is developed in VHDL with two input variables (set temp and actual temp) and one output variable. The difference between set temp and actual temp is error, after fuzzification error is divided in to three Fuzzy sets, as negative, zero and positive. Based on these Fuzzy sets 3 rules are fired and output is produced after Defuzzification. Upon successful completion of the VHDL coding functional simulation is performed to verify the correct functionality and to determine the deviation or tolerance parameters of the FTC using VHDL test bench.

A set of stimuli as inputs (functional vectors that changes with at fixed time duration) is fed into the test bench. The waveform in Fig 13 shows the values of the inputs and the corresponding output in hex form at the various instances determined by the stimuli in the test bench.

Now: 1000 ns		0	20	00	400		600	
■ <b>5/</b> set[7:0]	8'h50	8'h00	8'h50					
<b>■   </b>	8'h20	8'h00	8'h50	8'h48	8'h40	8'h38	8'h30	8'h28
<b>□ ◊(</b> i[7:0]	8'h0D	8'h14		8'h00	8'h03	8'h05	8'h08	8'h0A
<b>■ [</b> led0[7:0]	8'h30	8'h00		8'h08	8'h10	8'h18	8'h20	8'h28
■ <b>첫</b> led1[7:0]	8'h0D	8'h14		8'h00	8'h03	8'h05	8'h08	8'h0A

Figure 13: VHDL test bench output.

Input to matlab and C	normalized Input to VHDL	Matlab output	C output	VHDL output	De- normalized VHDL output
-4	8	0.339	3.4	03	0.375
-2	16	0.58	0.58	05	0.625
0	24	0.9	0.9	08	1
2	32.	1.2	1.2	10	1.25

Table 1: Inputs and the corresponding output in hex form at the various instances

For verifying the functionality of the VHDL code, output of VHDL, C, and Matlab are compared for different input conditions, as shown in table below. For VHDL coding the input is normalized to the range of 0 to 128.

# 5. FPGA Implementation.

The generated VHDL code of the FTC has been downloaded into FPGA (SPARTAN- 3 XC3S400 in PQ208 pin package). Two inputs are connected to I/O pins through A to D converter, as shown in figure 14. The photograph of FPGA development board is shown in figure 15. Note that the FPGA board contain a built-in 16 digital output LED's, 32 Input switches, 72 Free I/Os, 2 Serial interface, Communication Interface UART (RS-232) and is Configuration through Flash PROM and JTAG Port

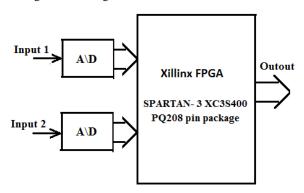


Figure 14: FLC system



Figure 15: FPGA Development board (SPARTAN-3 XC3S400 in PQ208 pin package.)

The I/O pins of FPGA board are connected to input 1, input 2 and output for verifying the correct functionality of the FTC chip for FPGA implementation.

## 6. Applications

This fuzzy Logic temperature control system implemented using FPGA Applied in any kind of environment to get improved performance with respect to the conventional scheme. The FLC is also able to keep the temperature constant at the desired value regardless of changes in the load or environment. Thus overshooting problem can be solved up to great extent. The FLC system implemented in FPGA can be applied to variety of industrial applications.

#### 7. Conclusions

The efficient design of the Fuzzy Logic controller according to the desired specifications using VHDL and its implementation on FPGA is useful for realizing a prototype of the Fuzzy Logic controller, applicable in real time systems. A fuzzy logic temperature controller has been designed for controlling the temperature. After de normalization VHDL output is used to control the current for maintaining the temperature at desired value.

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