A New Dual-Threshold Technique for Leakage Reduction in 65nm Footerless Domino Circuits

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ABSTRACT

A new dual-threshold circuit technique is proposed in this paper for reducing the subthreshold and gate oxide leakage currents in idle and non idle mode of operation for footerless domino circuits. In this technique a p-type and an n-type leakage controlled transistors (LCTs) are introduced between the pull-up and pull-down network and the gate of one is controlled by the source of the other. For any combination of input, one of the LCT will operate near its cut off region and will increase the resistance between supply voltage and ground resulting in reduced leakage current. Furthermore, the leakage current is suppressed at the output inverter circuit by inserting a transistor below the n-type transistor of the inverter offering more resistive path between supply voltage and ground. The proposed technique is applied on benchmark circuits reduction of active power consumption is observed from 34% to 57.5% at different temperature variations. For same benchmark circuits, operating at two clock modes and giving low and high inputs at 25^0C and 110^0C temperatures the maximum leakage power saving of 99.97% is achieved when compared to standard dual-threshold domino logic circuits in a 65nm CMOS technology.

Keywords

Dual-Threshold, Domino logic, Subthreshold leakage, Gate oxide tunneling, Leakage current.

1. INTRODUCTION

For high-speed chip performance domino circuits are employed and can be classified into footerless and footed domino [1-3]. For better timing characteristics footed domino is used because here the footer transistor isolates the pull-down network (PDN) from ground preventing the change in the state of the dynamic node by PDN during precharge phase. In addition if the footer transistor is omitted, the footerless domino reduces both the circuit evaluation delay and the power consumption. Having different characteristics, the footerless and footed domino based domino circuits both are extensively in high performance processors. For multistage domino circuits, the first stage is typically kept footed and others are footerless [3].

High leakage current in nanometer regime becomes a significant contributor to power dissipation in CMOS circuits as threshold voltage, channel length, and gate oxide thickness are scaled down. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. Leakage power especially depends on gate length and oxide thickness and it varies exponentially with threshold voltage and other device parameters. Reduction of supply voltages and threshold voltages for MOS transistors helps to reduce dynamic power dissipation but simultaneously leakage power increases. Leakage mechanism includes the following:

Subthreshold leakage current (I_{sub}) in MOS transistors, which occurs when the gate voltage is below the threshold voltage and mainly, consists of diffusion current [4]. Off-state leakage in present-day devices is usually dominated by this type of leakage. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short channel device. The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the subthreshold current [4].

$$I_{sub} = \mu_0 . C_{ox} . \frac{W}{L} . V^2 . e^{1.8} . e^{\frac{(V_{gs} - V_T)}{nV}} \quad (1.1)$$

where, μ_0 is the zero bias mobility, C_{ox} is the gate oxide capacitance, and (W/L) represents the width to the length ratio of the leaking MOS device. The variable V in equation 1.1 is the thermal voltage constant, and V_{gs} represents the gate to the source voltage. The parameter n in equation 1.1 is the subthreshold swing coefficient given by $1 + (C_d/C_{ox})$ with C_d being the depletion layer capacitance of the source/drain junction. One important point about equation 1.1 is that the sub threshold leakage current is exponentially proportional to $(V_{gs}-V_T)$. Shorter channel length results in lower threshold voltages and increases subthreshold leakage. As temperature increases, subthreshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse biased, there is a body effect that increases the threshold voltage and decreases subthreshold leakage.

Gate oxide tunneling current (I_{gate}) in which tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band [5].

Junction leakage that results from minority carrier diffusion and drift near the edge of depletion regions, and also from generation of electron hole pairs in the depletion regions of reverse-bias junctions. When both n regions and p regions are heavily doped, as is the case for some advanced MOSFETs, there is also junction leakage due to band-to-band tunneling (BTBT) [6].

Hot-carrier injection occurs in short-channel transistors. Because of a strong electric field near the silicon/silicon oxide interface, electrons or holes can gain enough energy to cross the interface and enter the oxide layer. Injection of electrons is

more likely to occur, since they have a lower effective mass and barrier height than holes [7].

Gate-induced drain leakage (GIDL), which is caused by high field effect in the drain junction of MOS transistors. In a negative- channel metal-oxide-semiconductor (NMOS) transistor, when the gate is biased to form accumulation layer in the silicon surface under the gate, the silicon surface has almost the same potential as the p-type substrate, and the surface acts like a p region more heavily doped than the substrate. When the gate is at zero or negative voltage and the drain is at the supply voltage level, there can be a dramatic increase of effects like avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate are swept to the substrate, completing the GIDL path [8]. Thinner oxide and higher supply voltage increase GIDL.

Punch through leakage, which occurs when there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions. This occurs in short-channel devices, where this separation is relatively small. Increased reverse bias across the junctions further decreases the separation. When the depletion regions merge, majority carriers in the source enter into the substrate and get collected by the drain, and punch through takes place [9].

In this paper, we study the sources of leakage current in dual-threshold (dual-V_t) domino and show that I_{sub} and I_{gate} are actually a function of not only inputs applied but also dependent on the clock signal state.

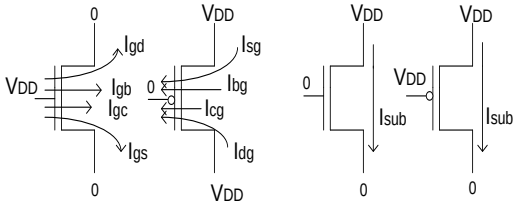
The remainder of the paper is organized as follows. In the next section leakage current analysis in dual-V_t domino is analyzed. In Section 3 proposed low leakage domino circuit is explained. Simulation results are given in Section 4. Finally the conclusions are offered in Section 5.

2. Leakage current analysis in dual-V_t domino CMOS circuit

This section is divided into two subsections namely 2.1 and 2.2. In Section 2.1 comparison of sub threshold and gate oxide leakage current produced by PMOS and NMOS transistors for low-V_t and high-V_t is shown. In Section 2.2 working of standard dual-V_t domino is discussed.

2.1 Leakage current characteristic comparison of P-channel and N-channel devices

Maximum gate oxide leakage and sub threshold leakage currents produced by PMOS and NMOS is shown in Figure 1. In Figure 1(a) four components of I_{gate} are shown: Gate to channel tunneling current (I_{gc}), gate-to-source tunneling current (I_{gs}), gate-to-drain tunneling current (I_{gd}) and gate-to-body tunneling current (I_{gb}) [10]. $I_{gs\ and}$ I_{gd} are the edge tunneling currents from gate to source and drain terminals respectively, through the gate-to-source and gate-to-drain overlap areas. I_{gc} is shared between source and drain terminals [11]. I_{gb} is smaller than the other three components of gate tunneling current and it is typically several orders of magnitude.



(a) **(b)**

Figure 1. State of maximum gate oxide and subthresold leakage current, in NMOS and PMOS transistors. (a) Maximum gate oxide leakage current state. (b) Maximum subthresold leakage current state.

As shown in Figure 1(a) maximum gate oxide leakage current flows when the transistor is turned ON and maximum potential difference between gate-to-source and gate-to-drain terminals. As shown in Figure 1(b) maximum sub threshold leakage current flows when the transistor is turned OFF and maximum the potential difference between source and drain terminals.

A comparison of normalized gate oxide and subthreshold leakage currents produced by NMOS and PMOS transistors for low-V_t and high-V_t in a 65nm dual-V_t CMOS technology is listed in Table 1. The data are measured for low and high die temperatures.

Table 1. Normalized gate oxide and subthreshold leakage currents for NMOS and PMOS (low-V_t and high-V_t) transistors at low and high die temperatures.

	NMOS Transistor		**PMOS Transistor**	
	Low-V_t	**High-V_t**	**Low-V_t**	**High-V_t**
I_{sub} (110^0C)	1.53	1.98	1.16	1
I_{gate} (110^0C)	.89	.098	.011	.0003
I_{sub} (25^0C)	1.18	1.41	1.17	1
I_{gate} (25^0C)	2.61	.29	.036	.0011

Transistor Length = 65nm, Width = 1µm, Low-V_t = 0.22V, High-V_t = 0.423V, V_{DD} = 1V. For each temperature, leakage currents are normalized by subthreshold leakage current produced by a high-V_t PMOS transistor.

Firstly, the I_{gate} produced by a low-V_t NMOS is 81x and 72.5x higher than the I_{gate} produced by a low-V_t PMOS at 110^0C and 25^0C respectively, as illustrated in Table 1. It shows that the probability of hole tunneling is much smaller than the probability of electron tunneling through the gate insulator. Therefore, the I_{gate} produced by a PMOS device is much smaller than the I_{gate} produced by a NMOS device with similar physical dimensions (width, length and t_{ox}) in a 65 nm technology and at the same potential difference across the gate insulator [12].

Secondly, the I_{gate} produced by a low-V_t NMOS is 9.1x at 110^0C and 9x at 25^0C higher than I_{gate} by a high-V_t NMOS transistor. Relatively higher gate tunneling barrier for the electrons is exploited in this paper by using a high-V_t NMOS transistor at the input of a domino circuits to reduce the gate oxide leakage current overhead of the proposed dual-V_t domino circuit technique.

2.2 Standard Dual-V_t Domino Logic

The standard dual-V_t domino logic shown in Figure 2. The first dual-V_t domino logic circuit was proposed by Kao [13] employing dual-V_t transistors for reduction of subthreshold leakage circuit. For maintaining the same delay as in standard footerless domino circuit the critical signal transition should occur through low-V_t during evaluation phase. Alternatively, during precharge phase signal transition is not a critical issue for maintaining in the performance of the circuit and the transistors that are active during precharge phase having high-V_t transistor [14]. The feedback keeper transistor parallel with precharge transistor whose gate is biased with the output voltage is employed to maintain the dynamic voltage against coupling noise, charge sharing problem and subthreshold leakage current [15].

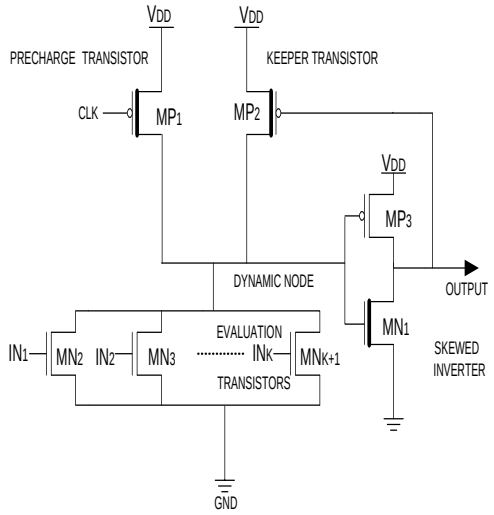


Figure 2. Standard Dual-V_t Domino Logic OR Gate. High-V_t transistors are represented by thick line in channel region.

The working of standard dual-V_t domino circuit is as follows: When the clock is low or during non-ideal mode the prechrage transistor MP_1(high-V_t) is ON and charges the dynamic node, this phase is called precharge phase. During the precharge phase output node goes low and MP_2 (high-V_t) transistor turns ON maintaining the dynamic node in the high state. The output of the domino logic is independent of the inputs applied at the evaluation network only the leakage current is dependent on the input vectors applied. Now when the clock is high or during ideal mode transistor, MP_1 is OFF and transistor MP_2 is dependent on the output of the domino circuit, this phase is called evaluation phase. The dynamic node charging will depend on the input vectors applied and according to that output node will be low or high. The subthreshold and gate oxide leakage will also depend on the applied input vectors.

3. Proposed Dual-V_t Domino Logic

The proposed circuit technique effectively enhances the reduction of subthreshold and gate oxide leakage simultaneously. The proposed circuit is illustrated in Figure 3. The concept behind the approach is the reduction of leakage power using

the effective stacking of transistor between the path from supply voltage to ground. The observation is based on [16], [17] and [18] in which a state with only one transistor is OFF between the supply voltage and ground is more leaky then the state with more than one transistor is OFF in a path from supply voltage to ground.

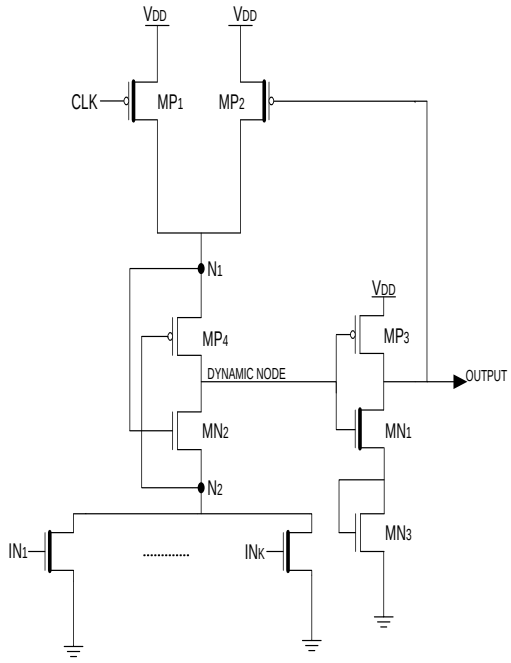


Figure 3. Proposed Dual-V_t Domino Logic OR Gate. High-V_t transistors are represented by thick line in channel region.

In our approach a low-V_t MP_4 (PMOS) and MN_2 (NMOS) LCTs are introduced between the precharge and evaluation network and the gate of these transistors are controlled by the source of each other. The drain node of MP_4 and MN_2 are connected together to form the input of the inverter. In this configuration, transistor MP_4 and MN_2 switching will depend on the voltage potential at node N_2 and N_1 respectively. So for any combination of input in the pull-down network one of the LCT will operate near its cut-off region and increase the resistance between V_{DD} and ground rails leads to the reduction of leakage current. High-V_t NMOS transistors replaces the low-V_t input transistors of pull-down network to reduce the gate oxide leakage current. Low-V_t MN_3 (NMOS) transistor in diode configuration is added below the high-V_t MN_1 transistor to further suppress the leakage current of the output invertor.

The working of proposed domino circuit is as follows: When the clock signal is low or during non-ideal mode the dynamic node is charged high through the transistor MP_1 (high-V_t) and MP_4 (low-V_t). The charging of dynamic node is almost independent of the previous clock input state. Suppose if the inputs are low before the clock sets low then node N_2 will be at low potential and transistor MP_4 offers the less resistance path for charging of dynamic node or if the inputs are high before the clock sets low then the voltage at node N_2 is not sufficient to turn MP_4 completely to OFF state (MP_4 is operating near its cut off region). The resistance of MP_4 will be lesser than in OFF resistance allowing the dynamic node to get charge high. The charging of the dynamic node is called precharging phase. In this case output of the domino circuit is independent of the inputs applied at the evaluation network only the leakage current is dependent on the input vectors applied as shown in Figure 4 and Figure 5.

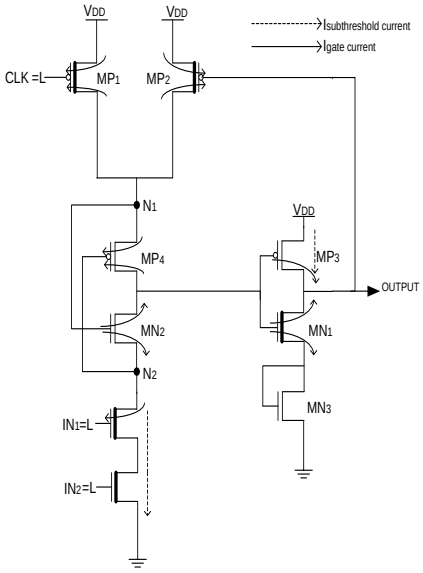


Figure 4. A two- input proposed Dual-V_t domino AND gate with low inputs during non-ideal mode. The most significant components of subthreshold and gate oxide leakage currents are illustrated with arrows. High-V_t transistors are represented by thick line in channel region.

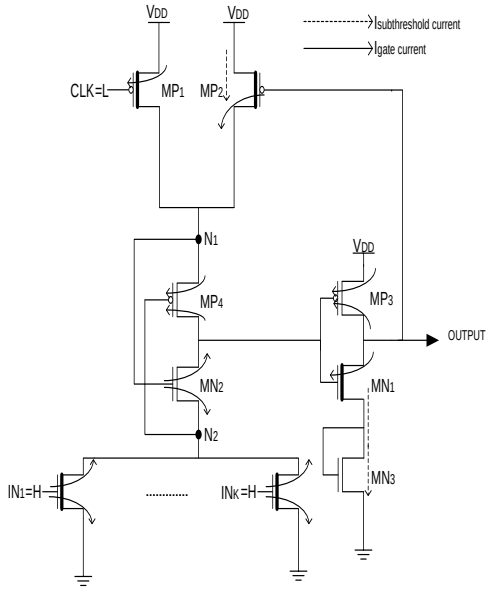


Figure 5. A k- input proposed Dual-V_t domino OR gate with high inputs during non-ideal mode. The most significant components of subthreshold and gate oxide leakage currents are illustrated with arrows. High-V_t transistors are represented by thick line in channel region.

Now when the clock turns high or during ideal mode this is called evaluation phase, depending on the inputs the dynamic node gets charged or discharged. If all the inputs are low the dynamic node will not be discharged by the evaluation network and the output of the inverter will be low and it turn ON the transistor MP_2 (high-V_t), the voltage at node N_1 will turn ON the transistor MN_1 (high-V_t) but the voltage induced at node N_2 will not cut off the transistor MP_4 it will operate near cut-off region offering high resistance path between V_{DD} and ground reducing sub threshold and gate leakage current. If all the inputs are high the dynamic node will be discharged through the evaluation network and the output of the inverter will be high. Transistor MP_2 will turn OFF, the voltage at node N_1 will operate the transistor MN_2 near its cut off region again offering high resistance path. The potential at node N_2 will turn ON the transistor MP_4. So by introducing the low-V_t LCTs the resistance between V_{DD} and ground is increased and simultaneously propagation delay of the domino circuit is also increased. The propagation delay will be controlled by sizing of the LCTs. Transistor MN_3 is added in the footed-diode configuration below transistor MN_1 producing the stacking effect in the inverter and reducing the sub threshold and gate oxide leakage current. In this case, the leakage will also depend on the input vectors as shown in Figure 6 and Figure 7.

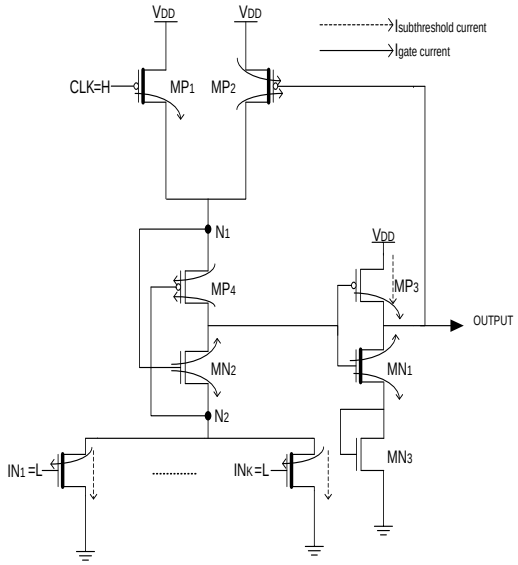


Figure 6. A k- input proposed Dual-V_t domino OR gate with low inputs during ideal mode. The most significant components of subthreshold and gate oxide leakage currents are illustrated with arrows. High-V_t transistors are represented by thick line in channel region.

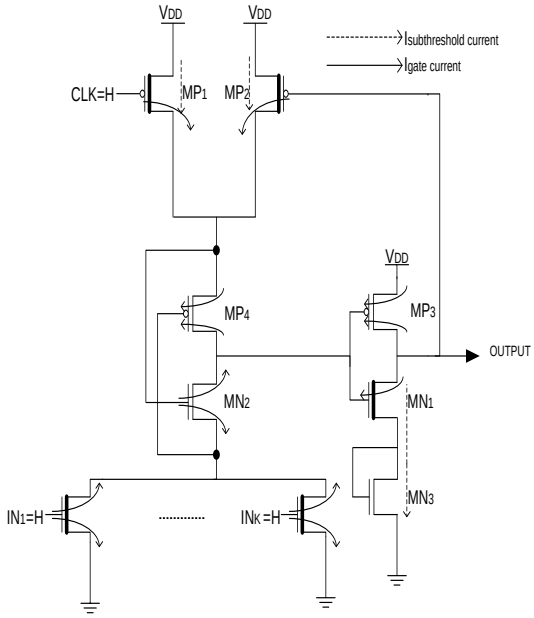


Figure 7. A k- input proposed Inverter Dual-V_t domino OR gate with high inputs during ideal mode. The most significant components of subthreshold and gate oxide leakage currents are illustrated with arrows. High-V_t transistors are represented by thick line in channel region.

4. Simulation Results

BISM4 device model is used for simulating the standard dual-V_t domino logic and proposed technique circuits for accurate estimation of subthreshold and gate oxide leakage currents. Following currents are simulated in a 65nm CMOS technology (V_{tnlow}=$|V_{tplow}|$=0.22V, V_{tnhigh}=0.423V, $|V_{tphigh}|$=0.365V, V_{DD}=1V and output capacitance C_{out}=1fF) 2-input domino AND gate (AND2), 2-input, 4-input and 8-input domino OR gates (OR2, OR4 and OR8 respectively). All these circuits are designed with standard dual-V_t domino and proposed dual-V_t technique. To have a reasonable comparison the sizing of NMOS and PMOS are equal in both the technique circuits. For measuring active power consumption clock pulse of 30ns is applied and measured for low and high inputs at low and high die temperatures. Comparison is done for total leakage power consumption in all the circuits by both the techniques during ideal and non ideal mode for low and high inputs at 25^0C and 110^0C.

4.1 Active Power Consumption

Active Power Consumption of the domino circuits are shown in Figure 8 and Figure 9 at 25^0C and 110^0C respectively. The result shows that active power in proposed dual-V_t circuits is reduced as compared with the standard dual-V_t domino circuits. At 25^0C the active power consumption decreases by 42% in AND2 , 43% in OR2, 50.7% in OR4, 57.5% in OR8 and at 110^0C 37.4% in AND2, 34% in OR2, 40.7% in OR4, 47% in OR8 when compared with standard dual-V_t domino circuits.

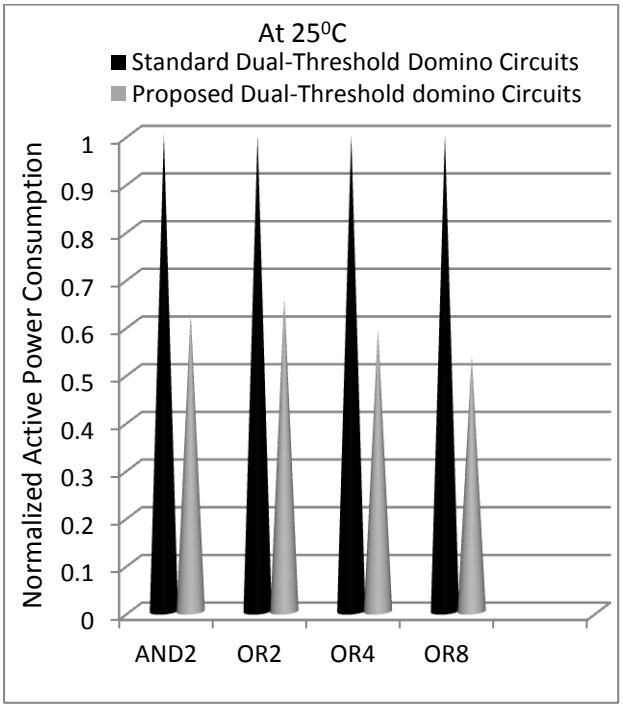


Figure 8. Active power consumption of two domino circuit techniques at 25^0C. For each circuit power consumption is normalized to the power consumed by standard dual-V_t domino technique.

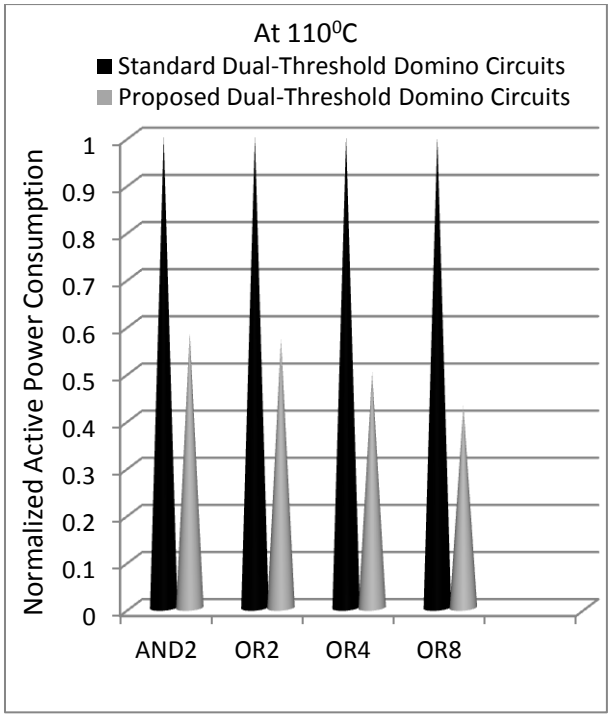


Figure 9. Active power consumption of two domino circuit techniques at 110^0C. For each circuit power consumption is normalized to the power consumed by standard dual-V_t domino technique.

4.2 Ideal Mode Leakage Power Consumption at 25^0C

In ideal mode the clock is high and precharge transistor is OFF and the voltage in dynamic node depends on the inputs. Two input conditions are simulated to evaluate the leakage current in ideal mode. The first condition is that all the inputs are low (dynamic node voltage goes high) and in the second condition when all the inputs are high (dynamic node voltage goes low). The leakage power reduction offered by the proposed circuit technique is listed in Table 2.

Table 2. Leakage power saving during ideal mode for low and high inputs at 25^0C compared with standard dual-V_t domino circuits

	AND2 %	OR2 %	OR4 %	OR 8 %
Proposed Domino Technique (Low Inputs)	84.79	42.29	46.58	50.77
Proposed Domino Technique (High Inputs)	99.56	81.62	72.08	82.24

The proposed dual-V_t domino techniques reduces the total leakage power by 42.29% to 84.79% driven with low inputs and when driven with high inputs total leakage power reduction varies from 72.08% to 99.56% as compared with standard dual-V_t domino circuits. Based on the results, during idle mode at room temperature if high inputs are maintained very low leakage current will flow in the circuit.

4.3 Ideal Mode Leakage Power Consumption at 110^0C

Under same conditions as at 25^0C simulations are done for 110^0C. The leakage power reduction offered by the proposed circuit technique is listed in Table 3.

Table 3. Leakage power saving during ideal mode for low and high inputs at 110^0C compared with standard dual-V_t domino circuits

	AND2 %	OR2 %	OR4 %	OR 8 %
Proposed Domino Technique (Low Inputs)	67.66	12.04	18.52	24.94
Proposed Domino Technique (High Inputs)	99.97	74.82	72.37	83.91

The proposed dual-V_t domino technique reduces the total leakage power 12.04% to 67.66% driven with low inputs and when driven with high inputs reduces the total leakage power by 72.37% to 99.97% as compared with standard dual-V_t domino circuits. Same as in 25^0C if high inputs are maintained at high die temperature very low leakage current will flow in the circuits in comparison with low inputs.

4.4 Non Ideal Mode Leakage Power Consumption at 25^0C

In non ideal mode the clock is low and precharge transistor is ON charging the dynamic node and the node voltage goes high. At the same time leakage current of the circuit depends on the input vectors applied at the input of the evaluation network. Based on the input conditions the circuits are simulated for the evaluation of the leakage current in non-ideal mode. In the first condition the inputs are low and in the second condition all the inputs are high. The inputs applied in the evaluation network will not put any effect on the voltage of dynamic node during non ideal mode it will remain at the high voltage potential. The leakage power reduction offered by the proposed circuit technique is listed in Table 4.

Table 4. Leakage power saving during non-ideal mode for low and high inputs at 25^0C compared with standard dual-V_t domino circuits

	AND2 %	OR2 %	OR4 %	OR 8 %
Proposed Domino Technique (Low Inputs)	98.34	60.61	26.52	7.41
Proposed Domino Technique (High Inputs)	70.08	69.85	83.25	82.96

The proposed inverter dual-V_t domino technique leads to the reduction of total leakage power by 7.41% to 98.34% driven with low inputs and 69.85% to 83.25% driven with high inputs when compared with standard dual-V_t domino circuit. Based on the simulation result at room temperature if high inputs are maintained during non-ideal mode very low leakage current will flow in this circuit compared with low inputs except in AND2 circuit low inputs should be maintained for low leakage current.

4.5 Non Ideal Mode Leakage Power Consumption at 110^0C

Based on same condition as non-ideal mode at 25^0C simulations are performed for 110^0C. The leakage power reduction offered by the proposed circuit technique is listed in Table 5.

Table 5. Leakage power saving during non-ideal mode for low and high inputs at 110^0C compared with standard dual-V_t domino circuits

	AND2 %	OR2 %	OR4 %	OR 8 %
Proposed Domino Technique (Low Inputs)	67.5	45.3	44.7	31.5
Proposed Domino Technique (High Inputs)	52.2	52.6	3.3	73.3

The proposed dual-V_t domino technique leads to the reduction of total leakage power by 31.5% to 67.5% driven with low inputs and 3.3% to 73.3% driven with high inputs when compared with standard footerless domino circuit. Simulation result analysis show that at high temperature (110^0C) OR 2,8 gates at high inputs low leakage current flows in the circuit in comparison to low inputs. For AND2 and OR4 gate the condition is vice versa.

5. Conclusion

In the 65nm technologies both the gate dielectric and subthreshold leakage currents must be suppressed for reducing power consumption during idle and non ideal mode. Therefore, a new domino technique is proposed for simultaneously reducing gate oxide and subthreshold leakage currents in domino logic circuits in same mode (ideal or non-ideal) with different input conditions.

The proposed domino circuit technique exploits the lector stacking effect employed between precharge and evaluation network and characteristics of high-V_t NMOS transistors used as input transistors of domino circuits. During non-ideal mode gate tunneling current is suppressed by using high-V_t input transistors both at 25^0C and 110^0C. For further reducing the leakage power consumption a transistor in diode-footed configuration is introduced in the pull-down of the output inverter for better reduction of subthreshold and gate oxide leakage of the overall domino circuits. Result shows reduction of active power by 42% to 57.5% at low and 34% to 47% at high die temperatures. In ideal mode 42.29% to 99.56% and 12.04% to 99.97% reduction of leakage with low and high inputs at 25^0C and 110^0C respectively and in non-ideal mode 7.41% to 98.34% and 3.3% to 73.3% with low and high inputs at 25^0C and 110^0C respectively when compared with standard dual-V_t domino circuits. This technique can be used for very high speed low power applications.

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