Thyristor Compact Modeling based on Gummel-Poon Model Including Parameter Extraction Procedure

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ABSTRACT
In this paper, an improved approach for the modeling of power thyristors is presented. A modified two-transistor configuration based on the Gummel-Poon model is applied. This model takes into account the conductivity modulation and carrier-carrier scattering by using nonlinear current sources. The current gain of the transistor is studied relating it to the injection level in order to provide a more insight of some SPICE parameters. The design parameters of the thyristor are related to circuit parameters using some analytical expressions. Then, the SPICE model parameters are extracted using Silvaco. The simulation results are compared with measurements showing good agreement indicating that the developed model could efficiently describe the performance of the thyristor under various practical operating conditions.

General Terms
Thyristor Modeling, TCAD, PSPICE.

Keywords
Modeling, Gummel-Poon, Conductivity Modulation, Design Parameters, Parameter extraction.

1. INTRODUCTION
Several thyristor models have been developed for use in circuit simulators. Some models were developed by solving the semiconductor equations numerically. Ma and Lauritzen [1] developed a physical SCR (Silicon Controlled Rectifier) model by employing the Lumped-Charge modeling technique to simplify the device physics. The model parameters were few and didn't describe the performance of the device completely. A model based on the Fourier-series approach was implemented for system simulation using Matlab [2]. This approach was first proposed by Kallala [3] whose model was implemented in ESACAP [4].

Other models were based on the two-transistor configuration assuming Ebers-Moll model. Williams [5] developed a dc and ac model by applying the Ebers-Moll BJT model to the two-transistor configuration. Because relatively few model parameters can be extracted from measured data, this model is not proper for simulation purposes. Brambilla *et al.* [6] developed a numerical SCR model based on the Ebers-Moll equations and a topology represented by the three-junction devices. The parameter extraction of these models was not provided which limits the applicability of these models.

The two-transistor model based on Gummel-Poon BJT model was a motivation for many published papers. The first who considered that modeling technique was Hu and Ki [7]. Then, a composite model for the GTO (Gate Turn OFF) was introduced by Xiangning *et al.* [8]. A parametric sensitive analysis was performed with the complete composite model, and comparison between experiment and SPICE simulations was provided. Good results of this model indicate the validity of the model and the superiority to use the Gummel-Poon model instead of the Ebers-Moll model.

Recently, Sayah *et al.* [9] proposed a SPICE model based also on the Gummel-Poon model and taking conductivity modulation into account. The advantage of this work is that a full parameter extraction sequence is provided [10]. This modeling technique is chosen in this paper as a starting point for the model. Some effects are added by modeling the conductivity modulation of the base region including the carrier-carrier scattering which is important to accurately adjust the static characteristics. Also, a detailed study is provided to demonstarte the variation of the current gains of the two transistor components of the model with the injection level in order to provide an accurate identification of the SPICE parameters of the model. An extraction of the design parameters is provided based on some analytical expressions and a trimming of these parameters is done using measurements. Finally, a case study is taken and its design parameters are extracted. Static and dynamic behaviors using SPICE simulations are compared with measurements showing good agreement.

2. MODEL DESCRIPTION

2.1 Main Structure
The basic structure of the thyristor is shown in Fig. 1(a) which also indicates the emitter short appearing as a simple resistance R_{sh}. The resistance of the lightly doped n-base layer of the thyristor to the anode current flow is modeled by the resistance R_{nb}. The complete model is represented in Fig. 1(b) where the two transistors are modeled using Gummel-Poon equivalent circuits. Actually, the two transistor model could be used very efficiently in modeling the thyristor and other relating devices. But it needs some modifications to accurately predict the terminal characteristics both static and dynamic.

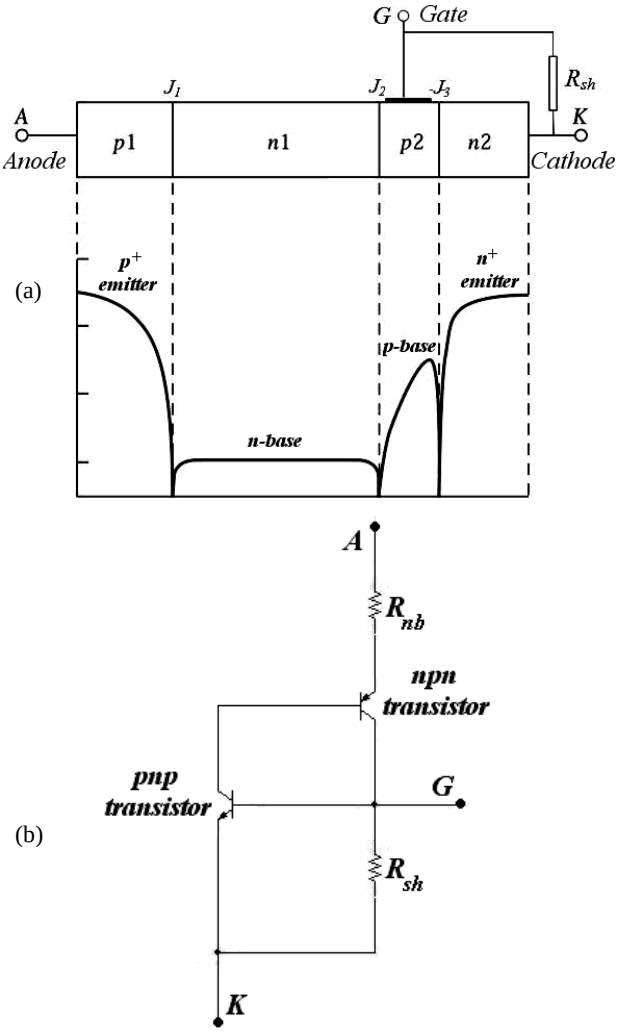


Fig 1 (a) Basic structure of the thyristor and (b) The two-transistor SPICE model

2.2 Conductivity Modulation and Carrier-Carrier Scattering

Concerning the resistance of the low-doped *n*-base, it could be modeled as follows:

$$R_{nb} = \frac{W_{nB}}{qA[(\mu_n + \mu_p)\Delta p + \mu_n N_{DB}]} \quad (1)$$

where Δp is the average excess hole concentration in the *n*-base. The sum of mobilities could be expressed in terms of the average excess hole concentration as [11]:

$$\mu_n + \mu_p = \frac{n_o \mu_o}{\Delta p + n_o} \quad (2)$$

Then inserting Eq. 2 into Eq. 1 leads to:

$$\frac{1}{R_{nb}} = \frac{qA\mu_n N_{DB}}{W_{nB}} + \frac{qA\mu_o n_o \Delta p}{W_{nB}(\Delta p + n_o)} \quad (3)$$

It could be deduced from the previous equation that the n-base resistance could be expressed in terms of three basic resistances; R_{onb}, R_{lim}, and R_{mod}. R_{onb} is the unmodulated base resistance, R_{lim} is a limiting resistance resulting from carrier-carrier scattering, and R_{mod} is resistance resulting directly from the excess hole concentration. In conclusion, the n-base total resistance including both effects of conductivity modulation and carrier-carrier scattering could be expressed as follows:

$$R_{nb} = R_{onb} // (R_{lim} + R_{mod}) \quad (4)$$

where

$$R_{onb} = \frac{W_{nB}}{qA\mu_n N_{DB}} \quad (5)$$

$$R_{lim} = \frac{W_{nB}}{qA\mu_o n_o} \quad (6)$$

$$R_{mod} = \frac{W_{nB}}{qA\mu_o \Delta p} \quad (7)$$

The excess hole concentration can be approximately expressed in terms of the anode current as [12]:

$$I_A = \frac{qA(W_{nB} + W_{pB})\Delta p}{\tau_p} \quad (8)$$

Finally the voltage drop on the conductivity modulated n-base is modeled as:

$$V_{nB} = I_A R_{nb} \quad (9)$$

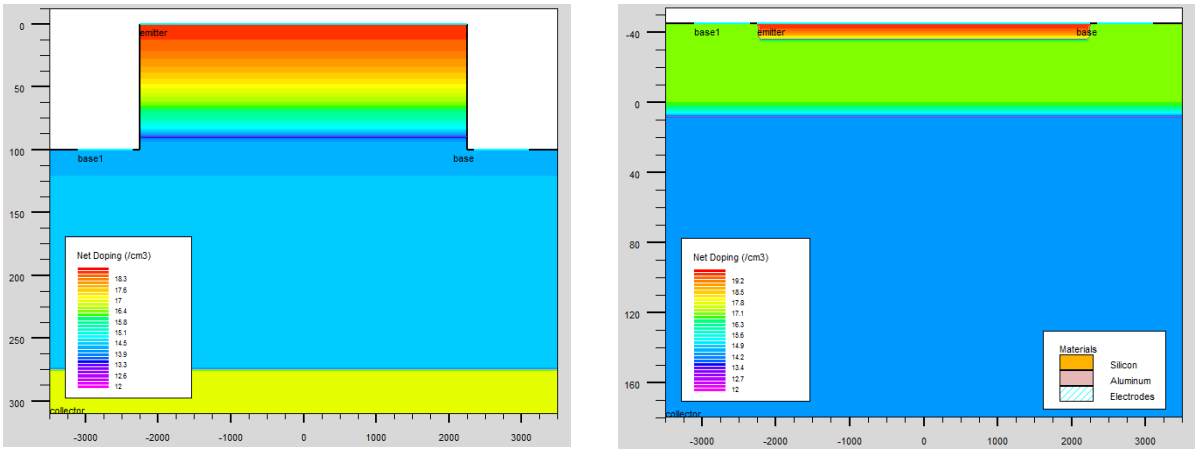
It is emphasized that the resistance R_{nb} accounts for the total resistor effect of the n-base which is the base region of the pnp transistor, so R_{nb} = 0 is used for the SPICE pnp BJT component in the simulation.

3. NPN AND PNP CURRENT GAINS

One of main issues that should be covered well is the study of the DC current gains (dc alphas) and the small-signal current gains (ac alphas). These alphas play an important role in the modeling of the thyristor considering the two-transistor model. Although many contributions are found in literature considering the measurements and simulation of various thyristor structures [13], the phenomenon of alpha behavior according to the injection level is not covered well.

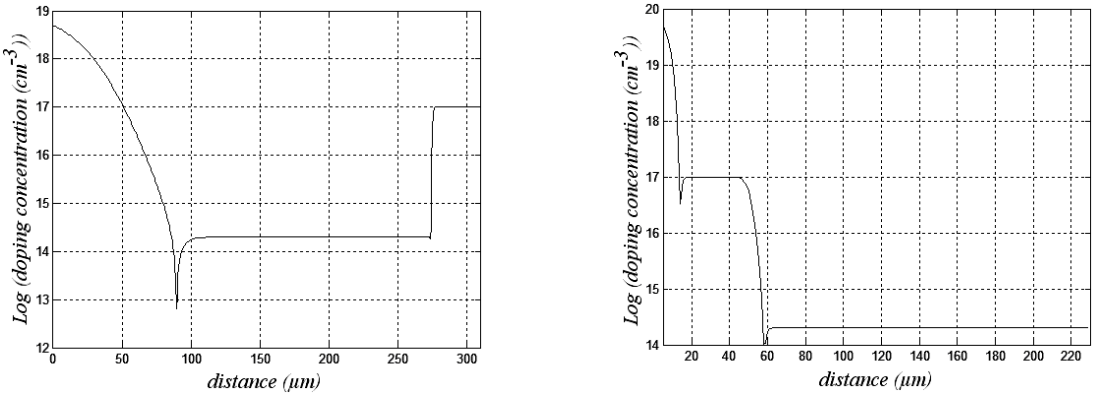
It is important to study this effect because the proposed model depends on some parameters which is very important to be modeled well or the results will deviate noticeably from measurements. Some of the vital model parameters are the SPICE parameters I_{KF} and I_{KR}. These parameters could be determined falsely leading to simulation errors. When injection levels are not taken into consideration, there will be errors in evaluating the current gains that couldn't be ignored.

To study this effect in details, a thyristor structure whose fabrication details are given in [14] and [15] is simulated. A process simulator Athena Silvaco [16] is used for simulation of the fabrication processes and a device simulator Atlas Silvaco [17] is used for simulation of the terminal characteristics. First the thyristor is decomposed of its two constitute two transistors. Each transistor is virtually fabricated and simulated separately. Then the alphas of the each component are determined. The comparison with measurements is done whenever possible.



(a) (b)

Fig 2 Transistors components of the thyristor: (a) pnp and (b) npn



(a) (b)

Fig 3 Doping profiles of the thyristor components: (a) pnp and (b) npn

The simulated thyristor structure is presented in [14]. The n-base width is about 180 µm with doping of 2×10^{14} cm^{-3}. The p-base is an epitaxial layer whose doping is ranging from 1×10^{16} cm^{-3} to about 1×10^{18} cm^{-3}. Now considering this thyristor structure and dividing it to its two transistor equivalence following the measurement technique by Gerlach [15] as shown in Fig. 2. The corresponding doping profiles are shown in Fig. 3.

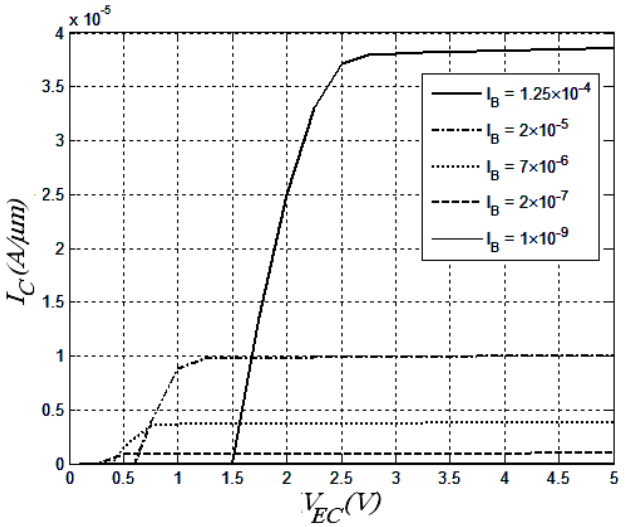


Fig 4 **The transfer characteristics of the pnp; all currents are given per width**

In order to obtain the alphas of each transistor, DC simulations are carried out, using Silvaco, in which the base current is varied in fine steps (such as to prevent simulation convergence) for different values of V_{CE}. A family of I_C-V_{CE} curves results. For instance, in the case of the pnp transistor, Fig. 4 shows these family of curves. All important physical semiconductor parameters are taken into account like the carrier-carrier scattering, band gap narrowing, and doping-dependent lifetime and mobility. Using the resulting *I-V* characteristics, the alphas are easily extracted.

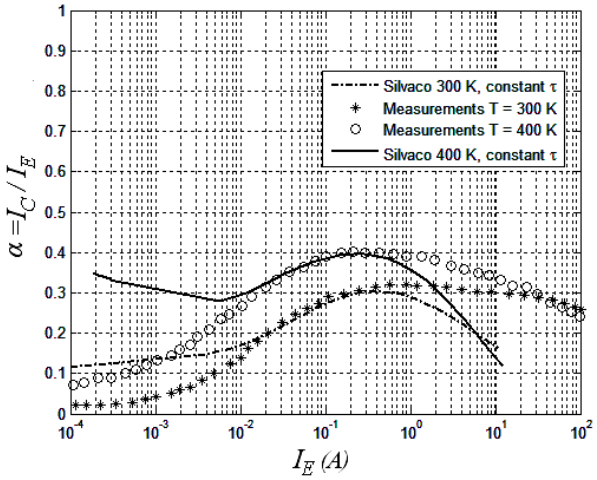


Fig 5 DC current gain of the pnp considering constant lifetime

Fig. 5 shows the corresponding alpha of the pnp transistor for a lifetime of τ_{HL} = 10 µs. As can be deduced from the figure, there are disagreements between the simulation and measurements. This is mainly accounted for by the constant lifetime model taken in the simulation. The disagreement increases at low level injection for high temperature because of increasing of lifetime with temperature.

The discrepancy between simulation and measurements could be reduced if the variation of the lifetime with injection level is taken. So, the lifetime is varied with the emitter current I_E. To reach the best fit with the measured data, the high-level lifetime is varied starting by 5 µs at low injection, reaching 8 µs to 10 µs at medium injection, and ending with 15 µs at high injection. As expected, the agreement becomes evident between measurements and simulations as shown in Fig. 6. To reach a good fit between simulation and measurements, a behavioral model is applied for the injection-dependent lifetime. Unfortunately, there is no such model in Silvaco. So, the lifetime is changed manually by incrementing it with current.

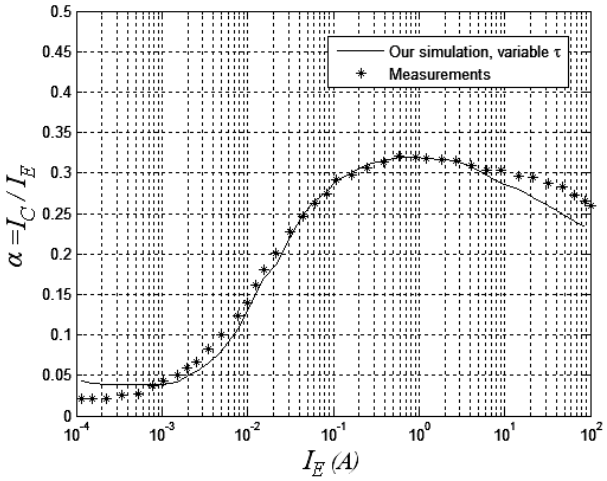


Fig 6 The DC current gain of the pnp considering variable lifetime

The conclusion is that the value of I_{KF} expected by regular simulation is far from reality. The actual value is considerably larger than the value obtained by direct extraction. The problem when using a small value of I_{KF} is that the summation of alphas may be below unity. In such case, the thyristor will be OFF while it should be ON. So, in the presented circuit model of the thyristor, I_{KF} is chosen to take a higher value than extracted.

4. IDENTIFICATION OF DESIGN PARAMETERS

First a quick review of the main design and circuit parameters of the thyristor model used is provided. Then the relations between these parameters are provided. The main design and technological parameters for the power thyristor are:

1) Active die area, A

2) n-base width, W_{nB}

3) n-base concentration, N_{DB}

4) Effective minority-carrier, and high-level lifetimes in the wide n-base, τ_p, and τ_{HL}

5) p-base width, W_{pB}

6) p-base concentration, N_{AB}

The parameter extraction approach relies on how to relate these physical parameters to the circuit parameters. The main circuit and device parameters are:

1) Breakdown voltage between A-K (this is related to V_{RRM} as in the case of power diodes), $V_{BR(AK)}$

2) Breakdown voltage between G-K, $V_{BR(GK)}$

3) DC forward current, I_F

4) The fall time, t_f

5) Device off time, t_q,

6) Forward voltage drop, V_F.

4.1 Active Die Area

An estimated value of the active die area A can be obtained from the forward current I_F (which should be indicated in the device datasheet). The current density J for most power thyristors is ranging from 100 A/cm^2 to 500 A/cm^2. Then, similar to power diodes [18], the initial value of A can be estimated as:

$$A = \frac{I_F}{J} \tag{10}$$

4.2 Minority-Carrier Lifetime

The minority-carrier lifetime in the n-base could be related approximately to either the turn-off time or the fall time of the thyristor. The turn-off time t_q (which is usually found in datasheets) is related to τ_p via the following relation [19]:

$$t_q \approx 4.6 \text{ to } 6.9\tau_p \tag{11}$$

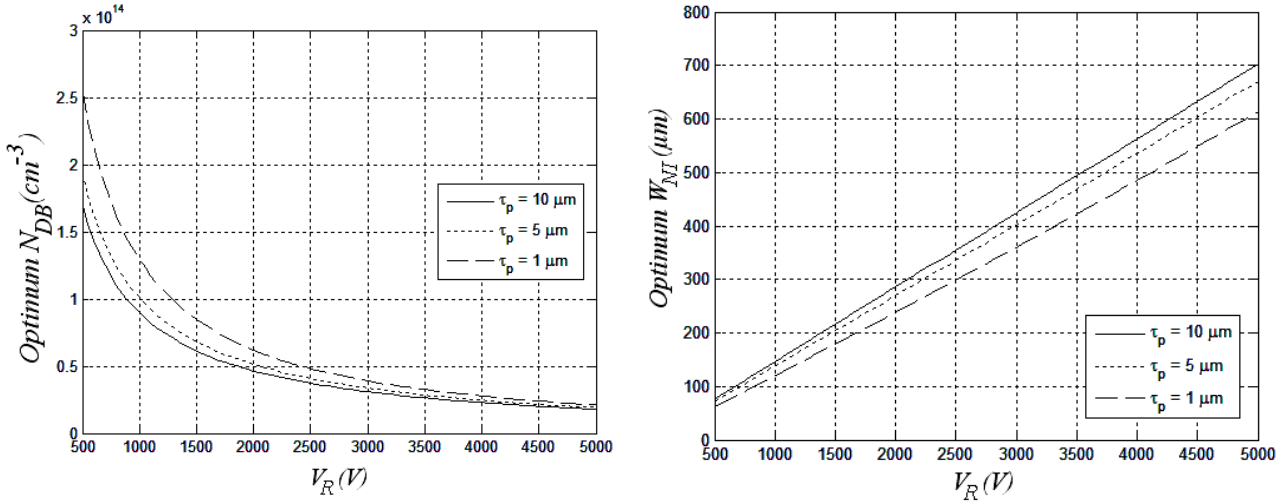
When the thyristor is commutated from a forward current I_F to a reverse current I_R, the fall time t_f of the reverse recovery current I_R (which is the time required for I_R to be reduced from 90% to 10% of its initial value at the storage delay time) is also directly related to the lifetime τ_p, and it is given by [12]:

$$t_f \approx 2.3\tau_p \tag{12}$$

4.3 n-base Width and Doping

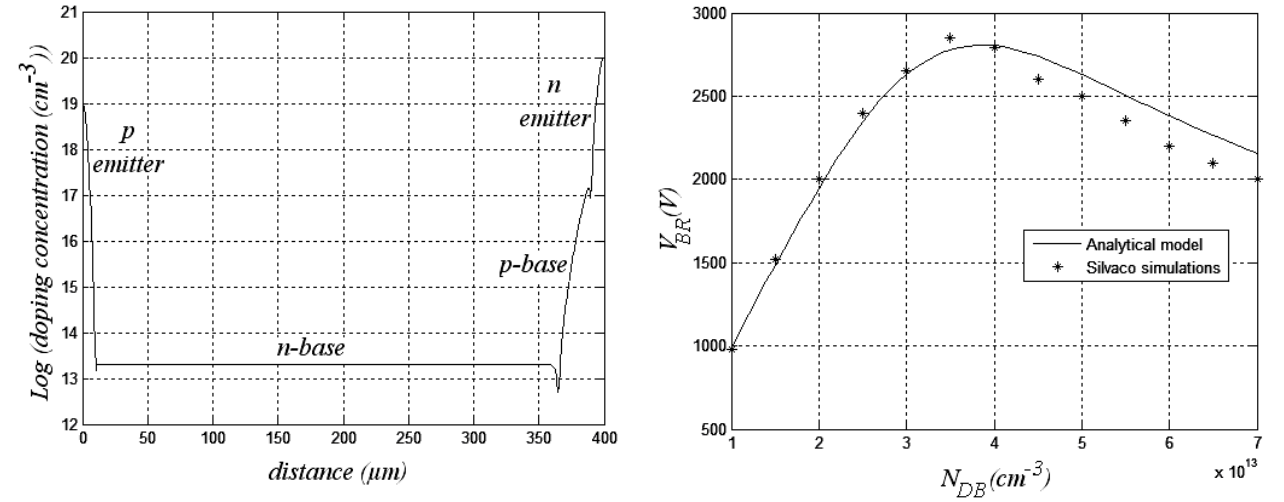
The actual breakdown voltage for the thyristor in the reverse-blocking mode is governed by the open-base transistor (P1N1P2) breakdown phenomenon. The optimization of the n-base width and doping is studied such that to obtain a specific value for the breakdown V_R (which is also called $V_{BR(AK)}$). Following the approach given by Baliga [20], V_R is varied for some selected different values of τ_p (= 1, 5, and 10 µs). The optimum base width and doping theoretically calculated are shown in Fig. 7 for different values of V_R.

To validate this theoretical approach, a typical thyristor structure is examined whose profile is shown in Fig. 8(a) with a wide n-base width of 360 µm and n-base doping of 2.1×10^{13} cm^{-3} [20]. The n-base doping is varied from 1×10^{13} to 7×10^{13} cm^{-3} and the breakdown voltage is calculated for each case. The lifetimes are fixed at $\tau_n = \tau_p$ = 3 µs. The comparison between the analytical model with Silvaco simulations is shown in Fig. 8(b). This comparison indicates good agreement and proves the usefulness of the analytical model used.



(a) (b)

Fig 7 Optimum base width and base doping for τ_p = 1, 5, and 10 µs



(a) (b)

Fig 8 (a) Doping profile of a thyristor, (b) Comparison between analytical model and Silvaco simulations for breakdown calculations

4.4 p-base Width and Doping

The p-base doping could be related to the breakdown voltage between the gate and cathode $V_{BR(GK)}$. A simple analytical expression is used considering the critical electrical field concept:

$$V_B = \frac{\varepsilon_r \varepsilon_o E_{Max}^2}{2qN_{AB}} \quad (13)$$

where E_{Max} is the maximum electric field in the junction which is given by [21]:

$$E_{Max} = 4010 N_B^{1/8} \quad (14)$$

Then, knowing V_{BR} of the gate-to-cathode junction, Eq. 13 and Eq. 14 are solved to find the p-base doping N_{AB}. This doping should practically in the range of 1×10^{16}-1×10^{17} cm^{-3} to obtain a reasonable gain for the internal npn BJT component of the thyristor [20].

The base width W_{pB} (or equivalently W_{P2}) may be found based upon the constraint about the forward voltage drop or the average ON-state voltage. The method relies on assuming a PIN diode behavior for the thyristor and calculating the forward characteristics [22]. This is practically accepted for cases when high injection prevails. In this case, the equivalent base diode width is W_{N1} + W_{P2} (where W_{N1} is the N-base width).

5. SIMULATION AND RESULTS

The BT151 is taken as a study case to validate the proposed model. Some selected design specifications from its datasheet are shown in Table 1. The main DC constraints are repetitive maximum voltage V_{RRM}, the peak reverse gate voltage V_{RGM}, and the forward current I_F. The main dynamic constraint is the turn-off time t_q at a certain condition.

Table 1 Main design specifications of BT151 thyristor

V_{RRM}	800 V
V_{RGM}	5 V
I_F (average)	7.5 A
V_F (typical) at I_F = 23 A	1.4 V
t_q (maximum) at di_F/dt = 30 µA/s and 125ºC	70 µs

5.1 Evaluation of Design Parameters

Following the methodology presented in the previous section, a try to extract the design parameters of this Thyristor is followed. The die active area could be found by assuming a forward current density of 200 A/cm^2 as an average value for a small thyristor. This gives an area of A = 0.0375 cm^2.

To extract the minority-carrier lifetime τ_p, the value of t_q specified in the datasheet is used. From Eq. 11, a maximum possible τ_p is required. Noting that t_q is given at a temperature of 125 ºC, the value of τ_p = 15.2 µs obtained should be corrected to get it at room temperature. Using the temperature dependence of the lifetime given in [23], τ_p could be calculated at room temperature which is about 10 µs.

Next, consider the breakdown voltage from anode-to-cathode. Assuming a margin of about 400 V (50% safety factor is assumed), then the breakdown voltage $V_{BR(AK)} \approx$ 1200 V. From Fig. 7 the n-base width and doping are obtained. The values are N_{DB} = 7.6×10^{13} cm^{-3} and W_{nB} = 175 µm. For the breakdown voltage from gate-to-cathode, consider the datasheet constraint V_{RGM}. Then $V_{BR(GK)} \approx$ 5 V. Using Eq. 13 and Eq. 14: N_{AB} = 2.18×10^{17} cm^{-3}.

Now, for p-base width W_{pB}, consider the forward voltage drop at a certain condition as given in the datasheet. Applying a DC model of the power PIN diode [22], and taking $\tau_{HL} \approx$ 20 µs, a suitable W_{pB} is found such that V_F (forward voltage) doesn't exceed 1.4 V at a current of 23 A. A value of $W_{pB} \approx$ 70 µm was found from these calculations. To check that the values are all in the correct range, the DC *I-V* characteristics are simulated and compared with that given in the datasheet. Fig. 9 shows the difference between simulation and datasheet typical values for temperature of 125 ºC. A good match is seen, assuming *h*-parameters of 3×10^{-14} cm^4/s on the average which is a suitable typical value.

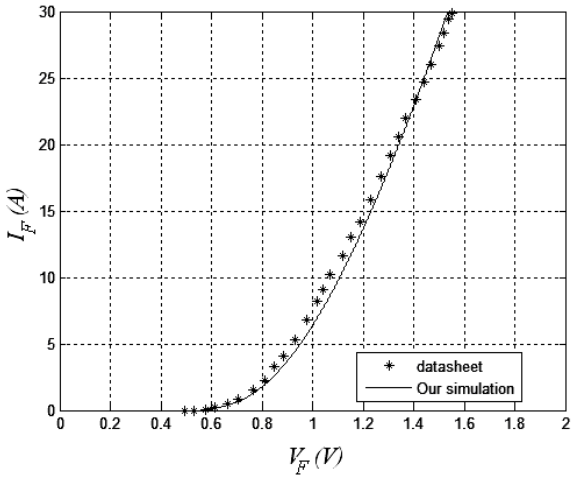


Fig 9 Comparison between simulation and datasheet DC characteristics

5.2 Design Parameters Trimming Using Measurements

First, the breakdown voltages were measured by a curve tracer and found to be $V_{BR(Ak)}$ = 1200, and $V_{BR(GK)}$ = 5.2 V. So, the doping levels and base widths will not be modified. The dynamic performance was measured and t_f was found to be 24 µs. Using Eq. 13, τ_p = 10.4 µs is calculated which is very close to the value obtained concerning t_q constraint.

Next, a check for the area *A* is done. *C-V* measurements were taken between the gate-anode junction. It was shown that [10]:

$$\frac{1}{C_m^2} = \frac{1}{C_{j_o}^2}\left[1+\left(1+\frac{V}{\varphi}\right)^{0.5}\right]^2 \quad (15)$$

where C_m is the measured capacitance between the gate and the anode. C_{jo} is the junction capacitance at zero bias which is given by:

$$C_{j_o} = A\sqrt{\frac{q\varepsilon_r\varepsilon_o N_{DB}}{2\varphi}} \quad (16)$$

From capacitance measurement: C_j = 85.4 pF and φ = 0.75 V. Then the area *A* could be obtained from Eq. 16: A = 0.03 cm^2 which is not far from the value obtained shortly. The difference may occur due to the uncertainty in determining the doping levels.

To complete the thyristor model one has to take into consideration the emitter shorts. A simplified model was proposed in [10]. From the model, the emitter short resistance was estimated to be $R_{sh} \approx$ 300 Ω. Table 2 shows a summary of the design parameters that that will be used in simulation.

Table 2 Design parameters used for simulations

Physical parameter	Symbol	Value
n-base doping concentration of the pnp transistor	N_{DB}	7.6×10^{13} cm^{-3}
p-base doping concentration of the npn transistor	N_{AB}	2.18×10^{17} cm^{-3}
n-base width of pnp transistor	W_{nB}	175 µm
p- base width of npn transistor	W_{pB}	70 µm
Area of the junction	A	0.0375 cm^2
Lifetime of minority carriers	τ_p	10 µs
The emitter short resistance	R_{sh}	300 Ω

Once these values for the technological parameters of the thyristor are extracted, Athena is used to fabricate virtually the two transistors. Then a built-in simulator in Silvaco called QUICKBIP is used to extract the Gummel-Poon SPICE parameters [24]. QUICKBIP is fully automated and takes all important bipolar semiconductor parameters into consideration. The extracted SPICE parameters for the pnp transistor and npn transistor are shown in Table 3. The values of *IKF* and *IKR* are not reliable for simulation as stated previously. Instead, suitable high values are used for SPICE simulation.

Table 3 Extracted SPICE parameters for the pnp and npn transistors

SPICE parameter	Symbol	npn	pnp
Saturation current	*IS*	5.6×10^{-14} A	1×10^{-12} A
Base-emitter saturation current	*ISE*	2×10^{-14} A	4.7×10^{-11} A
Base-collector saturation current	*ISC*	7.3×10^{-14} A	6×10^{-11} A
Forward knee current	*IKF*	125 mA	190 mA
Reverse knee current	*IKR*	0	61 mA
Maximum forward current gain	*BF*	4.5	2.5
Maximum reverse current gain	*BR*	1.2	2
Base-emitter built-in potential	*VJE*	0.88 V	0.3 V
Base-collector built-in potential	*VJC*	0.3 V	0.3 V
Emitter-base junction capacitance	*CJE*	2000 pF	60 pF
Collector-base junction capacitance	*CJC*	54 pF	52 pF
Emitter-base capacitance gradient factor	*MJE*	0.34	0.5
Collector-base capacitance gradient factor	*MJC*	0.5	0.5
Ideal forward transit time	*TF*	0.3 μs	6 μs
Ideal reverse transit time	*TR*	1.5 μs	5 μs
Forward current emission coefficient	*NF*	0.95	1
Reverse current emission coefficient	*NR*	1	1
Low-current base-emitter emission coefficient	*NE*	1.7	1.2
Low-current base-collector emission coefficient	*NC*	1	1.2

5.3 Simulation Results

In this section, using the thyristor model parameters determined in the previous section, the static and dynamic characteristics of the thyristor under study are simulated.

In order to turn-ON the thyristor, the gate current I_G must be increased to a certain value. This value is found to be about 2.45 mA from measurements. The *I-V* characteristics in this case are a full thyristor curve having the conventional S-shape as shown in Fig. 10. Also, Fig. 11 shows the measured and simulated *I-V* curves for the diode mode of operation of the thyristor for different anode ranges. The results show good agreement between the simulation and measurements which indicates the usefulness of the model used for static characteristics.

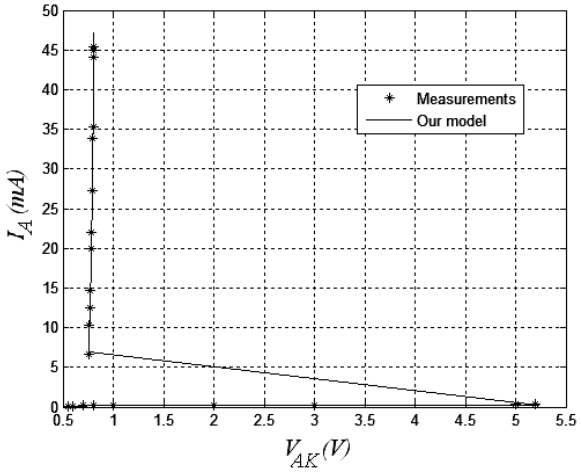


Fig 10 Measured and simulated I-V characteristics of the thyristor at the turn-ON point (I_G = 2.45 mA)

(a)

(b)

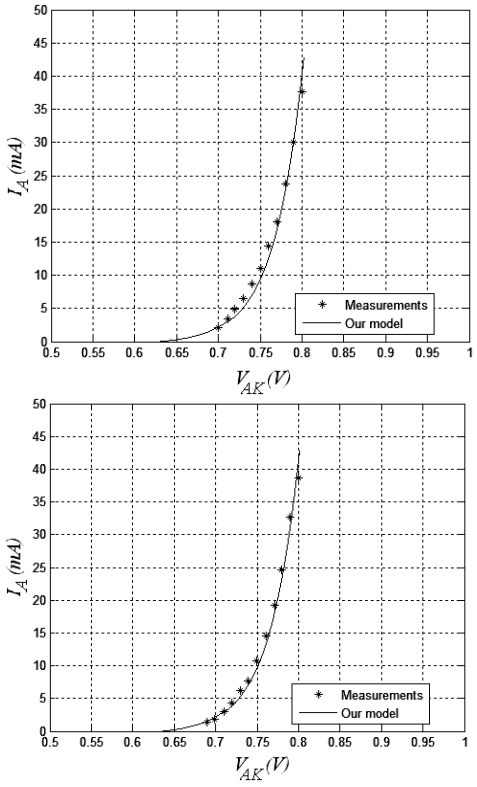


Fig 11 Measured and simulated I-V characteristics in the diode mode for (a) I_G = 8 mA, and (b) I_G = 9.5 mA

For the dynamic characteristics, the circuit shown in Fig. 12 is used for measurements and SPICE simulation. Fig. 13 shows the measured [9] and simulated switching waveforms at the same applied signals (square waveform of amplitude =16 V p-p, and frequency = 10 kHz). The waveforms are similar in shape and there is a good quantitative agreement between measured and simulated waveforms. This proves the validity of the model in tracing the dynamic behavior as well as the static one.

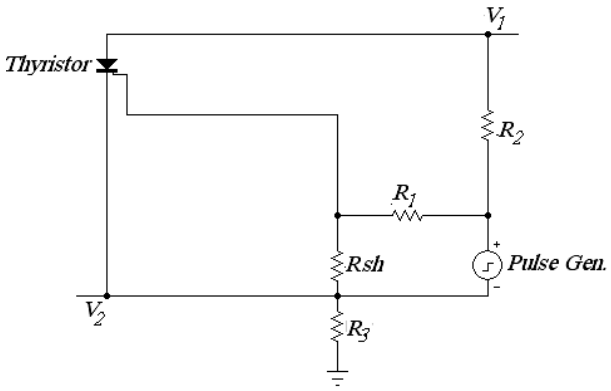


Fig 12 Circuit used for dynamic characteristics simulation

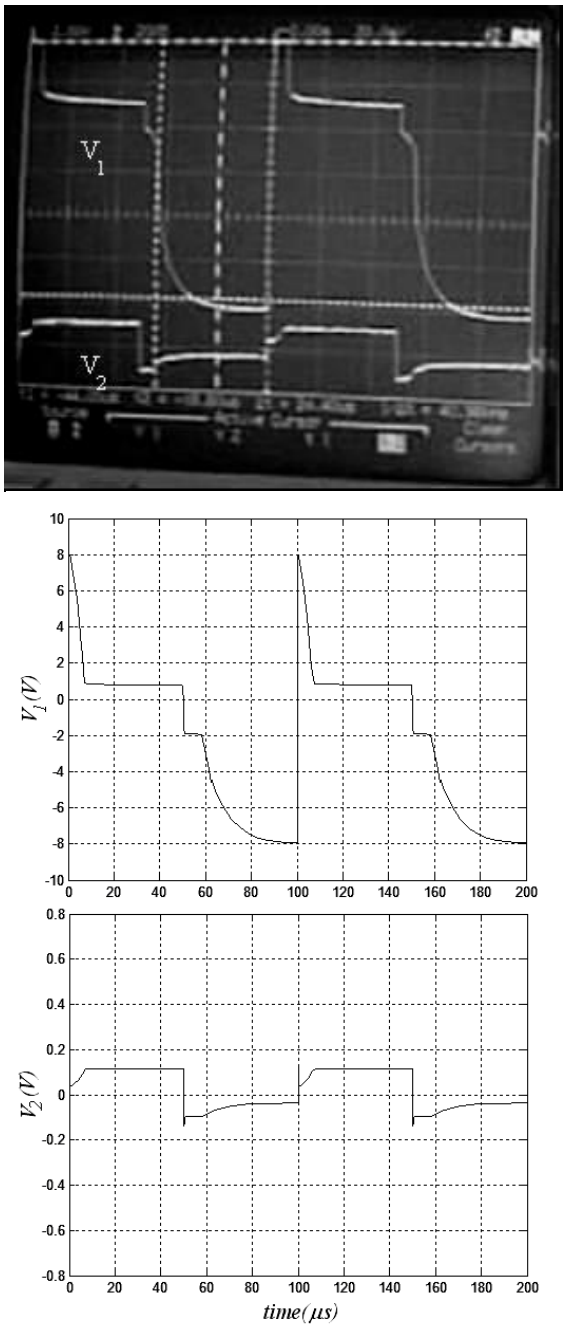


Fig 13 Measured and simulated switching waveforms of the anode to cathode voltage
$V_{AK} = V_1$ and the anode current $I_A \approx V_2 / R_3$

6. CONCLUSIONS

In this paper, an improved modeling approach for the power thyristor is presented. The model is based on the two-transistor configuration considering the Gummel-Poon model. It is demonstrated how to obtain the design parameters of the thyristor using simple analytical expressions. According to the design parameters, a SPICE parameters extraction using QUICKPIB simulator in Silvaco environment is accomplished. A case study was presented in details. The design and SPICE parameters were extracted. Static and dynamic behaviors were simulated using the SPICE model of the thyristor and compared to measurements. Very good agreement between simulations and measurements is observed showing the availability of the proposed model in tracing the various conditions of operation.

7. REFERENCES

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